HIERARCHICAL SIZING AND BIASING OF ANALOGUE FIRM INTELLECTUAL PROPERTIES

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CHAMS Project

Project **CHAMS** is developped by LIP6-SOC-CIAN-AMS group:

Team:

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- Jean-Paul CHAPUT (Research Engineer)

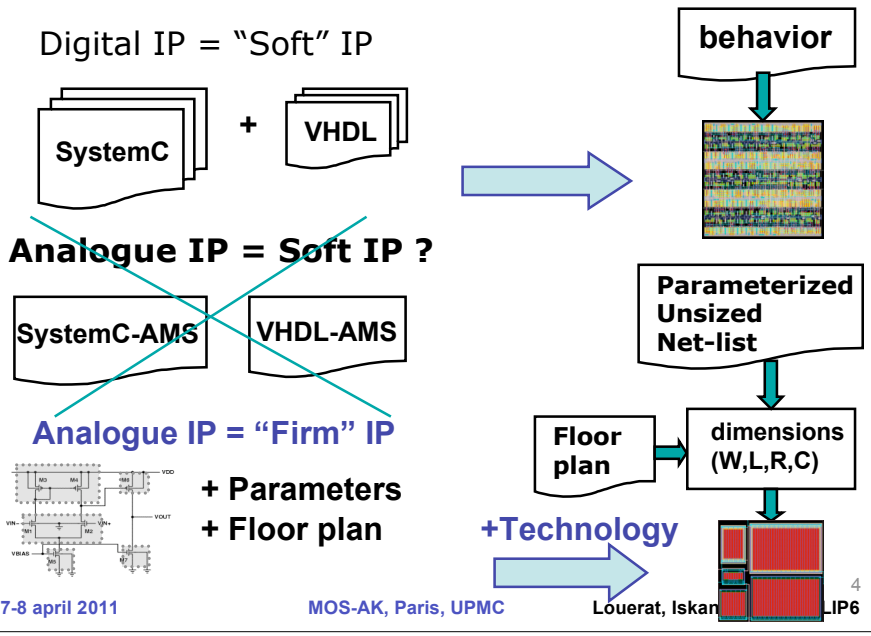
Collaboration:

- Prof. Andreas KAISER (ISEN-IEMN)

Presentation Outline

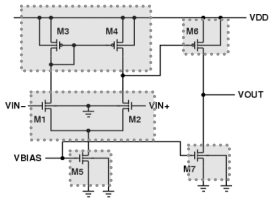
- Background and Motivations
- Problem Definition
- MOS Transistor-Model-Based Sizing and Biasing
  - From Transistor to Circuit
  - Circuit Sizing and Biasing : Dependency Graph
  - Application: Knowledge-Aware Synthesis
  - Results
- CHAMS Project : 2 posters
- Conclusions

Motivation : Parameterized Analogue Circuit



Motivation : analogue IP features

the **Sizing Procedure** : A systematic approach to parameterize an Analogue Circuit



Netlist : known topology
+Input parameters
+**Sizing Procedure**
(Dependency Graph)

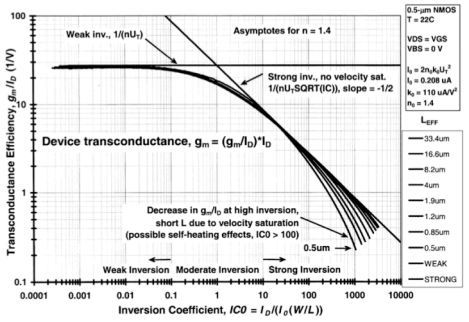
- Migration : Technology and Performance
- Reuse : Hierarchy (leaf cells : library of devices)
- Knowledge : stored and used for sizing
- As accurate as electrical simulator (Compact Transistor model)
- Layout aware sizing (layout template)

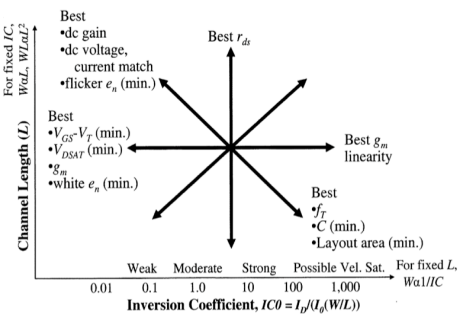
Motivation : Knowledge Aware Sizing

GOAL: Optimize design tradeoffs ! Control all MOS electrical performances !

Design Inputs: Saturation Current I_D, Inversion Coefficient IC_0, Length L

$$W = I_D \,.\, L \,/\, (\, I_0 \,.\, IC_0 \,)$$



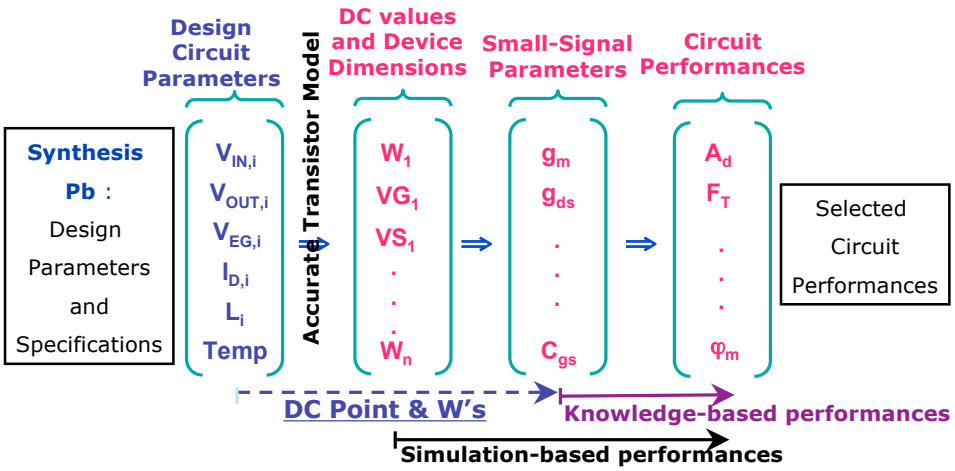


Silveira, Flandres, Jespers, " A gm/ID based Methodology for the Design of CMOS Analog Circuits and Its Application to the Silicon-on-Insulatror Micropower OTA", IEEE JSSC, SEPT 1996

Binkley, Hopper, Tucker, et al, "A CAD methodology for optimizing transistor current and sizing in analog CMOS design", IEEE TCAD of Integrated Circuits and Systems, 2003.

Problem Definition : V_{EG}, L, I_{DS} input

Knowledge : Design Parameters, gm/I_D ==> $V_{EG} = V_{GS}-V_{th}$



Sizing Procedure : the DC Operating Point & W's Calculation

Transistor Sizing and Biasing

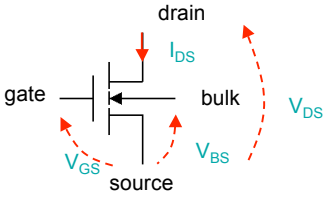
Transistor in Saturation

$$I_{DS} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$$= \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)(V_{EG})^2(1 + \lambda V_{DS})$$

$$V_{th} = V_{th0} + \gamma_n\left(\sqrt{2\,\phi_F - V_{BS}} - \sqrt{2\,\phi_F}\right)$$

$$\phi_F = \frac{k \cdot Temp}{q} \ln \frac{N_A}{n_i}$$



$V_{EG} = V_{GS} - V_{th}$

Overdrive voltage

where μ, C_{OX}, λ, V_{th0}, γ_n, N_A and n_i are technology parameters

For every transistor, we are interested in the following electrical parameters:

I_{DS}, W, L, V_G, V_S, V_D, V_{GS} or V_{EG}, V_B, Temp and V_{th}

This choice is independent on the used transistor model.

Models that are not threshold-voltage-based, do not have V_{th} (e.g. PSP)

Transistor Sizing and Biasing

How to Compute : Temp, L, V_{GS} or V_{EG}, W, I_{DS}, V_{th}, V_B, V_G, V_S and V_D ?

Parameter	Input/output	Knowledge
temp	input	Application dependant
L	input	Noise, matching, gain
IDS	input	Power budget
VB	input	Netlist
VEG/VGS	input	Inversion coefficient
VG, VS	output	?
VD	output	?
W	output	?

What about W, V_G, V_S and V_D ?

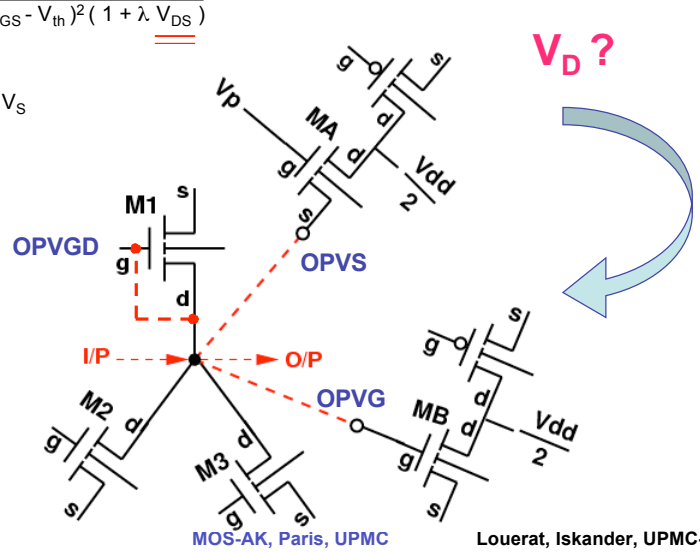
Transistor Sizing and Biasing

How to compute W, V_G, V_S & V_D ?

+MOS Transistor Model

$$W = \frac{2 \cdot L \cdot I_{DS}}{\mu C_{OX} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})}$$

$V_{DS} = V_D - V_S$



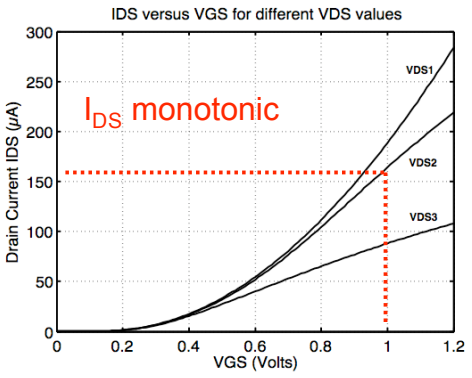
Transistor Sizing and Biasing

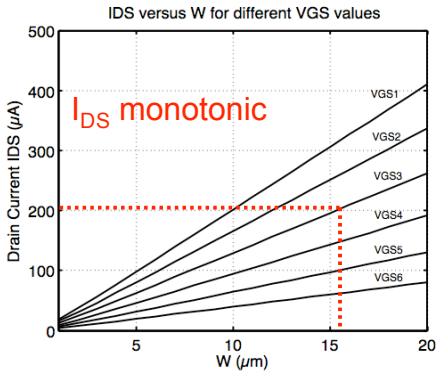
We developed 46 sizing and biasing operators. These are divided into 5 classes.

Operator Name	Input	Output
OPVS	**Temp**, I_{DS}, L, V_{EG}, V_D, V_G , V_B	V_S,V_{th},**W**
OPVG	**Temp**, I_{DS}, L, V_{EG}, V_D,V_S	V_G,V_B,V_{th},**W**
OPVGD	**Temp**, I_{DS}, L, V_{EG}, V_S	V_G, (=V_D),V_B,V_{th},**W**
OPW	**Temp**, I_{DS}, L, V_D, V_G, V_S	**W**,V_B,V_{th}
OPIDS	**Temp**,W,L,V_{EG},V_D,V_G,V_S	I_{DS},V_B,V_{th}

Transistor Sizing and Biasing

Each sizing and biasing operator solves only one of the numerical problems below.





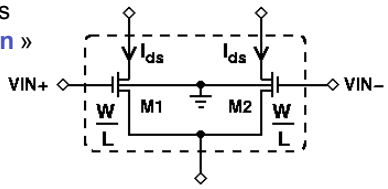
$$V_{GS}^{k+1} = V_{GS}^{k} - \frac{I_{DS}(V_{GS}^{k}) - I_{DS,desired}}{g_m(V_{GS}^{k})} \quad \text{(A)}$$

$$W^{k+1} = W^{k} - \frac{I_{DS}(W^{k}) - I_{DS,desired}}{I'_{DS}(W^{k})} \quad \text{(B)}$$

Device Sizing and Biasing

Definition of a Device

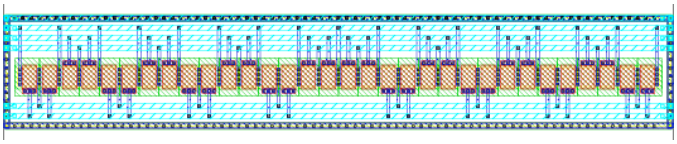
« A device is a **set of transistors** that constitutes an **elementary and standard electrical function** »



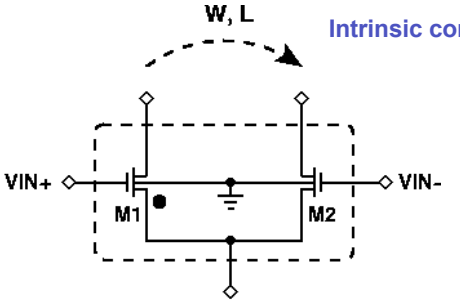
Transistor Packing

« Transistors are **packed in a device** if:

- They realize, together, a **known electrical function**
- They have common electrical parameters like (W, L, or V_{GS}), ==> have **dedicated layout** (common physical parameters) to reduce mismatch error »



Device Sizing and Biasing



Intrinsic constraint

- Every device has only **one reference transistor** (marked with a dot)
- The **reference transistor** is **chosen** by the designer of the device
- The reference transistor is the **only transistor that is sized** in a device
- Electrical parameters are **propagated** from the reference transistor to secondary ones

Example: W and L of the differential pair are propagated from M_1 to M_2

Device Sizing Procedure : Dependency Graph

A **node** represents a parameter : I_{DS}, W, L, V_G, V_S, V_D, V_{GS}, V_{EG}, V_B or Temp

Each node has some attributes:

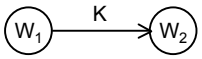
- Type of node : voltage, current, width, ...
- List of multiple aliases :

$W_1 = W_2 \Rightarrow$

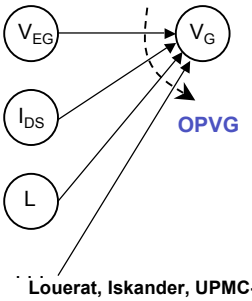
- A **dependency rule** having some attributes:
  - ❑ Type of rule : **Constraint**, **Operator**, …
  - ❑ List of affected nodes (LVALUE)
  - ❑ List of affecting nodes (RVALUE)
  - ❑ Operator : Name of a procedure to execute

Constraint

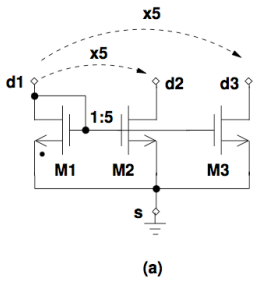
$W_2 = K \cdot W_1$



Operator

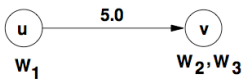


Device Sizing and Biasing Procedure

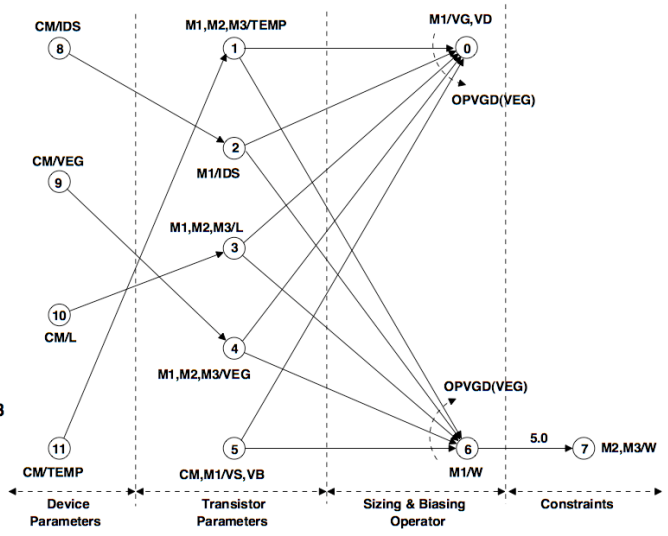


(a)

Current Mirror CM

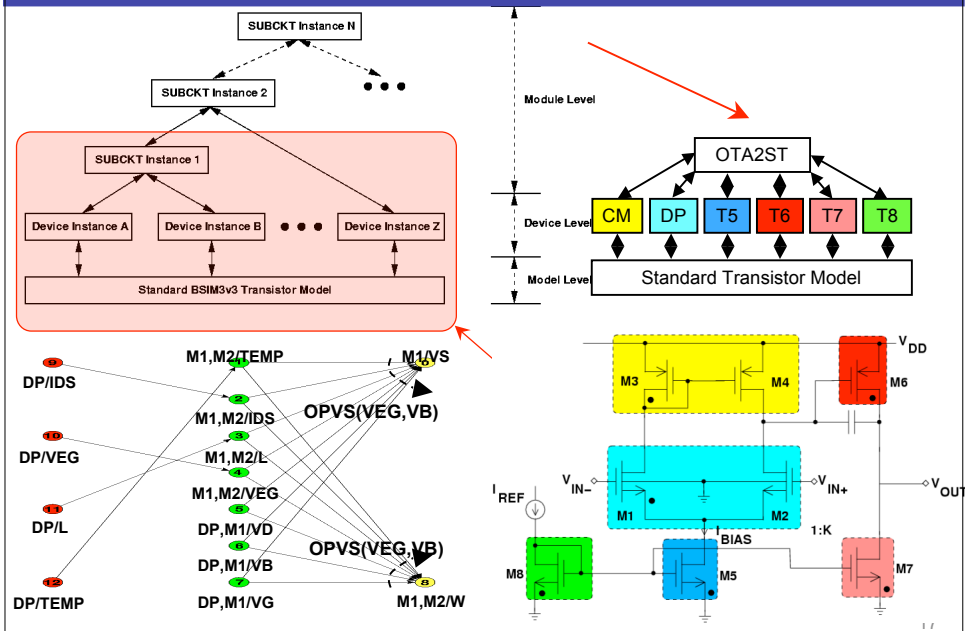


Intrinsic constraint



Sizing Procedure : Device (Current Mirror) Dependency Graph

Circuit Hierarchy Sizing and Biasing Procedure



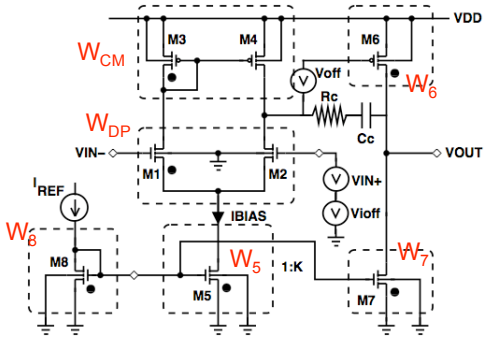
Differential Pair DP

Analog IP: Single-Ended Two Stage Amplifier

Hypotheses

Assuming Minimum Systematic Offset

- $V_{off} = 0 \Rightarrow V_{D,M3} = V_{D,M4} = V_{G,M6}$
- $L_{M8} = L_{M5} = L_{M7}$
- $L_{CM} = L_{M6}$
- $W_{M8} = W_{M5}$

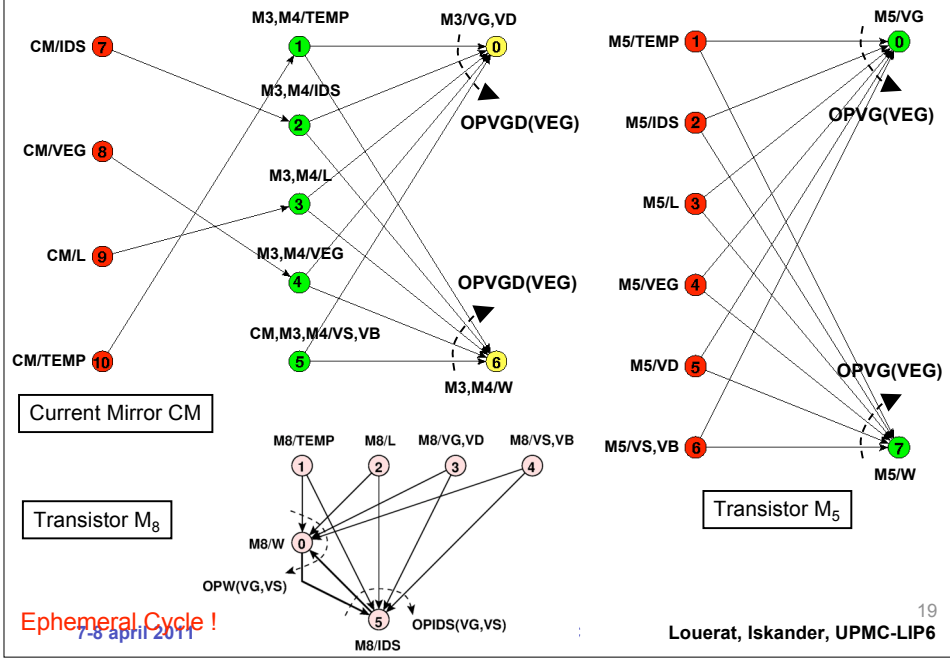


Input Parameter	Parameter Value	Input Parameter	Parameter Value
Temp (Kelvin)	300.15	V_{DD} (V)	1.2
V_{SS} (V)	0.0	I_{BIAS} (µA)	30.0
$V_{EG,M5}$ (V)	0.1	$L_{M5,M7,M8}$ (µm)	0.34
$V_{EG,CM}$ (V)	-0.12	L_{DP} (µm)	0.34
$V_{EG,DP}$ (V)	0.12	$L_{CM,M6}$ (µm)	0.34
V_{INCM} (V)	0.6	V_{OUTCM} (V)	0.6
$K = I_{M6} / I_{BIAS}$	5.0		

Compute the sizes:

W_{DP}, W_{CM}, W_5, W_6, W_7, W_8 ?

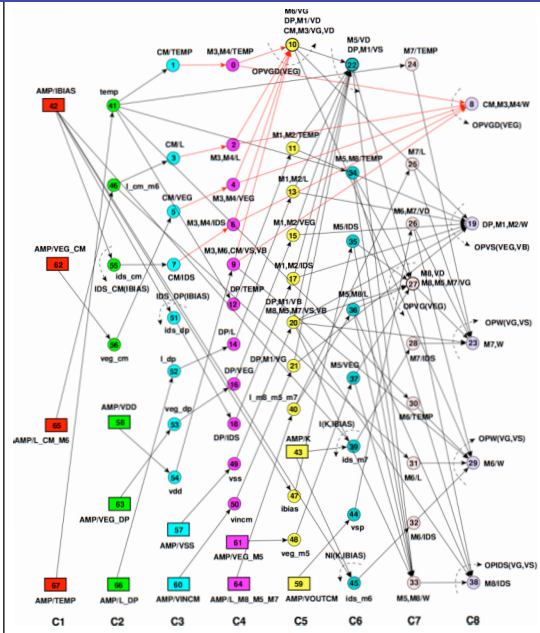
Sizing & Biasing of Amplifier Devices



Ephemeral Cycle !

Dependency Graph of the Amplifier

- Directed Acyclique Graph (DAG)
- Input Parameters → Rectangles
- Propagation Variables → Fine Circles
- Device Parameters → Fine Circles
- Sizing & Biasing Operators → Bold Circles with Arrows
- Widths Computed in C8
- $W_{M8} = W_{M5}$ in (C7,33)
- Designer-Defined Procedure in (C2,55)
- Minimum Systematic Offset in (C5,10)
- Sizing & Biasing Procedure:
  1. Node 10: $V_{G/D,M3}$
  2. Node 22: $V_{D,M1}$
  3. Node 27: $V_{G,M5}$
  4. Node 23: W_{M7}
  5. Node 33: W_{M8} W_{M5}
  6. Node 38: I_{DS}
- Fully Reusable and Technology Independent



Sizing & Biasing Results of the Amplifier

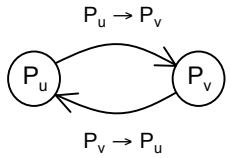
DC Operating Point and Sizes for the Technology CMOS 0.13µ et V_{DD} = 1.2V
For Minimum Systematic Offset

Parameter	Synthesis (Design Mode)		Spice Simulation		
	M_1,M_2	M_6	M_1	M_2	M_6
I_{DS} (µA)	15.0	-150.0	15.0	15.0	-149.9
V_{GS} (V)	0.481	-0.474	0.481	0.481	-0.474
V_{DS} (V)	0.608	-0.6	0.608	0.608	-0.6
V_{BS} (V)	-0.118	0.0	-0.118	-0.119	0.0
V_{th} (V)	0.362	-0.354	0.362	0.362	-0.354
V_{EG} (V)	0.12	Not Given	0.120	0.120	-0.120
V_{dsat} (V)	0.119	-0.119	0.119	0.119	-0.119
g_m (mA/V)	0.191	1.90	0.191	0.191	1.90
g_{ds} (µA/V)	2.27	17.8	2.27	2.27	17.7
g_{mb} (mA/V)	0.0356	0.369	0.0357	0.0357	0.369
C_{gd} (fF)	1.04	24.6	1.04	1.04	24.6
C_{gs} (fF)	5.31	152	5.32	5.32	152

$(W/M)_{DP}$	$(W/M)_{CM}$	$(W/M)_{M5}$	$(W/M)_{M6}$	$(W/M)_{M7}$	$(W/M)_{M8}$	$I_{DS,M8}$
2.08 µm/4	6.32 µm/2	6.64 µm/4	62.2 µm/20	27.6 µm/16	6.64 µm/4	35.29 µA

Inconsistencies in Dependency Graphs

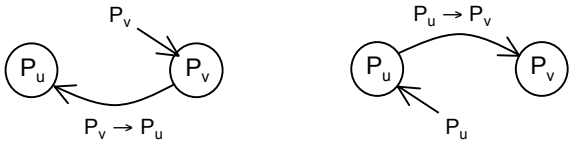
Our objective is to automatically generate **REUSABLE**, **PORTABLE** and **CONSISTENT** sizing procedures in the form of ***Dependency Graphs***.
Therefore, dependency graphs should be **Directed Acyclic Graphs (DAG).**



Directed Cycle = An Unknown to Determine !!!

- Different types of cycles appear in the following cases:
  1. **Ephemeral directed cycles** (Device re-ordering problem)
  2. **Under-specified** problems have **directed cycles** (insufficient degrees of freedom)
  3. **Undirected cycles** appear in **Negative feedback** circuits

Solution : **Cut The Cycles !**



- Conflicting Hypotheses (Excess degrees of freedom in **Over-specified** problems).

Designing the Amplifier with Conflicting Hypotheses

Reformulating Hypotheses

Assuming Nonzero Systematic Offset

- $V_{off} \neq 0 \Rightarrow V_{D,M3} = V_{D,M4} \neq V_{G,M6}$
- $L_{CM} \neq L_{M6}$
- $L_{M8} = L_{M5} = L_{M7}$
- $W_{M8} = W_{M5}$

Input Parameter	Parameter Value	Input Parameter	Parameter Value
Temp (Kelvin)	300.15	V_{DD} (V)	1.2
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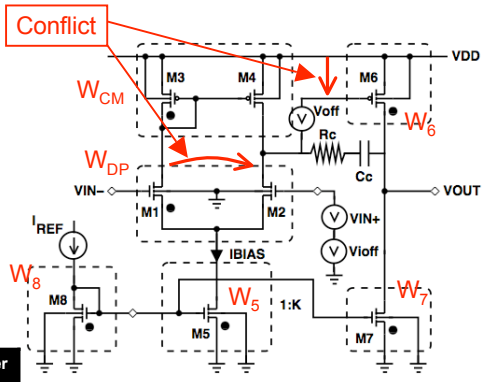
$V_{eg,M5}$ (V)	0.1	$L_{M5,M7,M8}$ (µm)	0.34
$V_{EG,CM}$ (V)	-0.12	L_{DP} (µm)	0.34
$V_{EG,DP}$ (V)	0.12	L_{CM} (µm)	0.34
$V_{EG,M6}$ (V)	-0.1	L_{M6} (µm)	0.34
V_{INCM} (V)	0.6	V_{OUTCM} (V)	0.6
$K = I_{M6} / I_{BIAS}$	5.0		

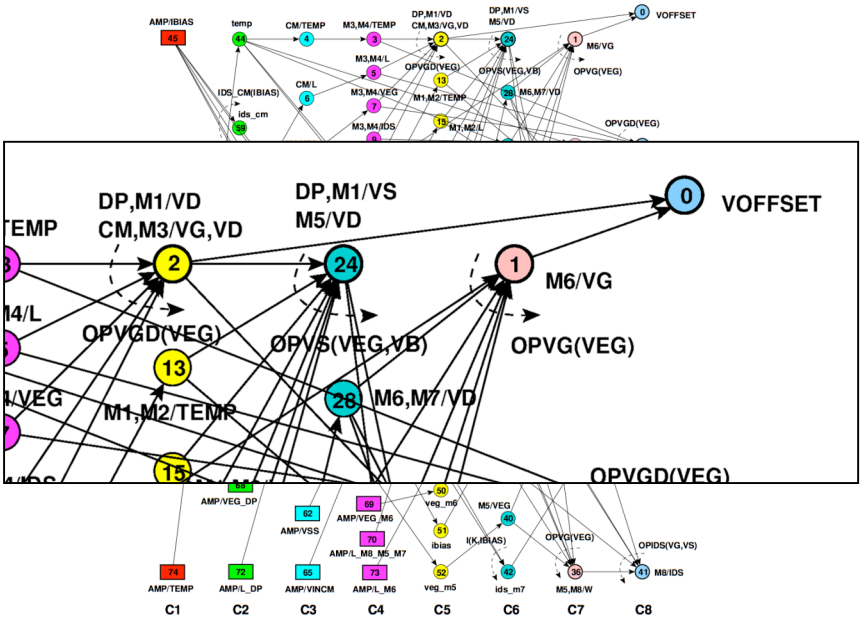


Conflict is resolved by introducing systematic offset as one degree of freedom

SI: $$g_{m,M6} \simeq \frac{2\, I_{M6}}{V_{GS,M6} - V_{th,M6}}$$

$$V_{i,off} \simeq (V_{D,M4} - V_{G,M6}) \frac{g_{ds,M2} + g_{ds,M4}}{g_{m,M1}}$$

Dependency Graphs with Systematic Offset



Results of Sizing the Amplifier with Systematic Offset

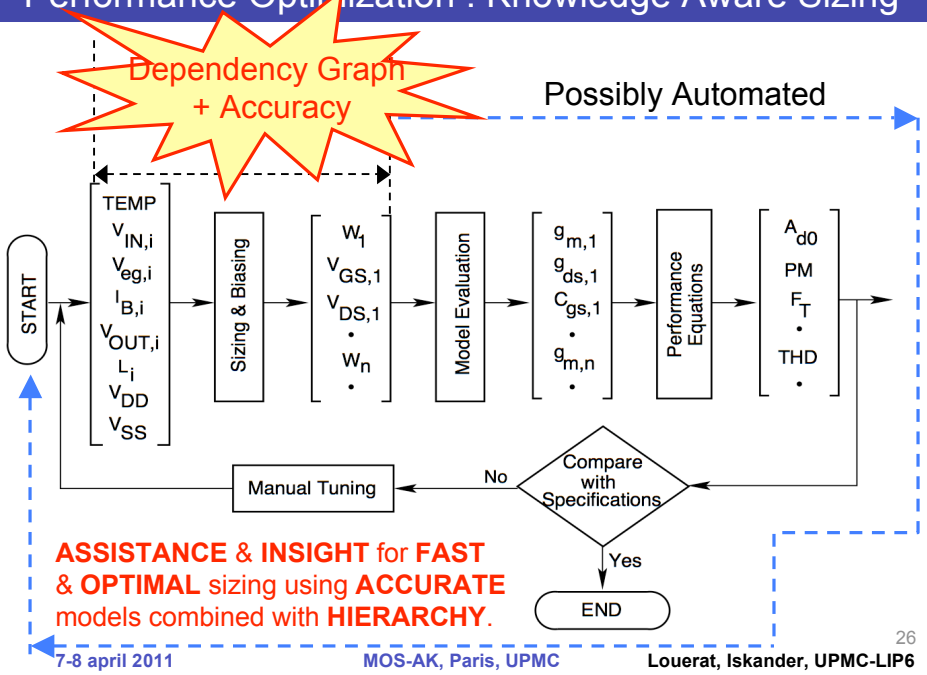
Operating Point For The Technology CMOS 0.13µ and V_{DD} = 1.2
With Nonzero Systematic Offset

Parameters	Synthesis		Spice Simulation		
	M_1,M_2	M_3,M_4	M_1	M_2	M_4
I_{DS} (µA)	15.0	-15.0	15.0	15.0	-15.0
V_{GS} (V)	0.481	-0.474	0.481	0.481	-0.474
V_{DS} (V)	0.608	-0.474	0.608	0.627	-0.454
V_{th} (V)	0.362	-0.354	0.362	0.362	-0.354
V_{EG} (V)	0.12	-0.12	0.120	0.120	-0.120
g_m (mA/V)	0.191	0.190	0.191	0.191	0.190
g_{ds} (µA/V)	2.272	2.227	2.28	2.24	2.33
	M_6		M_6		
I_{DS} (µA)	-150.0		-150.0		
V_{GS} (V)	-0.454		-0.454		
V_{DS} (V)	-0.6		-0.6		
V_{th} (V)	-0.354		-0.354		
V_{eg} (V)	-0.1		-0.100		
g_m (mA/V)	2.10		2.10		
$V_{i,off}$ (mV)	-0.468[1]		Not used for simulation		
$V_{i,off}$ (mV)	-0.471[2]		-0.471		

1. Using approximate equations.
2. Using accurate equations.

$(W/M)_{M6}$	80.63 µm / 22

Performance Optimization : Knowledge Aware Sizing



ASSISTANCE & **INSIGHT** for **FAST** & **OPTIMAL** sizing using **ACCURATE** models combined with **HIERARCHY**.

Results for Knowlegde-Aware Synthesis

Optim. Parameters	Range	Synthesis
$L_{M5} = L_{M7} = L_{M8}$ (µm)	0.2:3.0:0.1	0.6
L_{CM} (µm)	0.2:3.0:0.1	0.6
L_{M6} (µm)	0.2:3.0:0.1	0.2
L_{DP} (µm)	0.2:3.0:0.1	0.8
$V_{EG,M5}$ (V)	0.01:0.2:0.01	0.1
$V_{EG,DP}$ (V)	0.01:0.2:0.01	0.08
$V_{EG,CM}$ (V)	-0.2:-0.01:0.01	-0.15
$V_{eg,\ M6}$ (V)	-0.2:-0.01:0.01	-0.04
I_{BIAS} (µA)	10.0:30.0:1.0	25
K	1.0:5.0:0.5	4.5
C_C (pf)	1.0:5.0:0.1	2.9

Circuit Performances	Target	Syn.	Sim.
A_{d0} (dB)	> 65	71.22	70.83
A_{c0} (dB)	< 17	5.59	8.82
F_T (MHz)	> 6	10.79	10.66
ϕ_m (degrees)	> 76	76.69	76.9
Input Offset Voltage (mV)	< 2	-1.03	-1.07
Input Noise @1Hz (µV/Hz)	< 20	10.86	10.14
Input Noise @F_T (µV/Hz)	< 0.02	0.014	0.015
SR (V/µS)	> 6	8.25	9.16
Transistors in Saturation	= 8	8	8
Power Consumption (mW)	< 1	0.176	0.176
CMRR	-	65.63	62.01
Min Common-Mode Inp. (V)	-	0.53	0.53
Max Common-Mode Inp. (V)	-	1.04	1.04
Max Output Voltage (V)	-	1.12	1.12
Min Output Voltage (V)	-	0.1	0.1
Area (µm²)	-	69	69
Average Runtime over 10 runs		76 secs	

Computation time :
Interactive Process

Results for Technology Migration Through ReSizing

Variable	Domaine	Synthèse
$L_{M5} = L_{M7} = L_{M8}$ (µm)	0.2:3.0:0.1	0.3
L_{CM} (µm)	0.2:3.0:0.1	0.9
L_{M6} (µm)	0.2:3.0:0.1	0.3
L_{DP} (µm)	0.2:3.0:0.1	1.8
$V_{eg,M5}$ (V)	0.01:0.2:0.01	0.07
$V_{eg,DP}$ (V)	0.01:0.2:0.01	0.17
$V_{eg,CM}$ (V)	-0.2:-0.01:0.01	-0.17
$V_{eg,\ M6}$ (V)	-0.2:-0.01:0.01	-0.09
I_{BIAS} (µA)	10.0:60.0:1.0	56
K	1.0:5.0:0.5	5
C_C (pf)	1.0:5.0:0.1	2.6

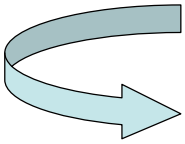
Performance	Cible	Syn.	Sim.
A_{d0} (dB)	> 65	72.04	71.49
A_{c0} (dB)	< 17	15.91	18.13
F_T (MHz)	> 12	17.2	17.09
ϕ_m (degrees)	> 76	76.44	76.59
Input Offset Voltage (mV)	< 2	-0.67	-0.6882
Input Noise @1Hz (µV/Hz)	< 20	8.31	7.02
Input Noise @F_T (µV/Hz)	< 0.02	0.0125	0.0127
SR (V/µS)	> 6	18.61	20.0
Transistors in Saturation	= 8	8	8
Power Consumption (mW)	< 1	0.432	0.432
CMRR	-	56.13	53.36
Min Common-Mode Inp. (V)	-	0.58	0.58
Max Common-Mode Inp. (V)	-	1.03	1.03
Max Output Voltage (V)	-	1.1	1.1
Min Output Voltage (V)	-	0.09	0.09
Area (µm²)	-	155	155
Average Runtime over 10 runs		87 secs	

Since the unity-gain frequency F_T is doubled, the biasing current I_{BIAS} has also doubled !

Simulation-Based Hierarchical Sizing and Biasing

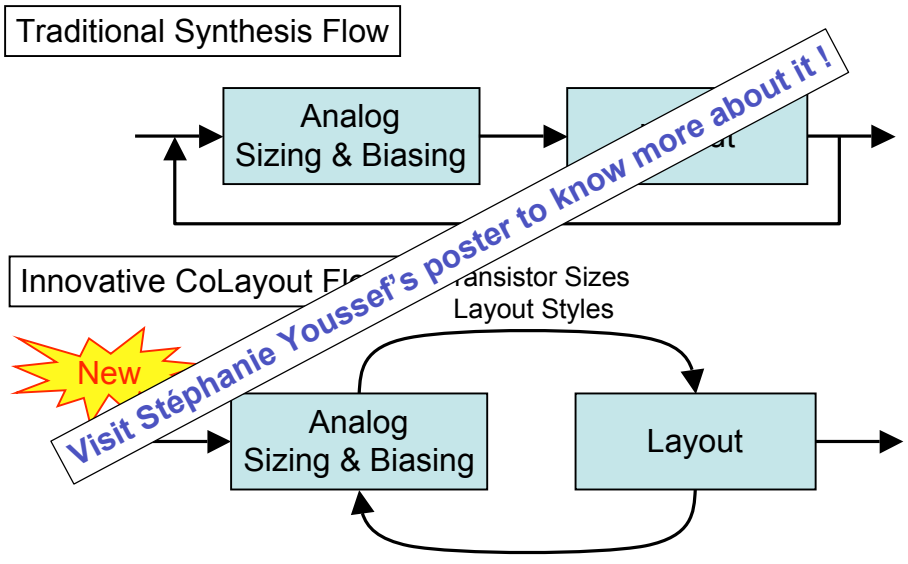
Built-in Model for Sizing & Biasing requires Huge Investement !

Therefore, we provide a **Simulation-Based** Version



Please visit
Farakh Javid's Poster
To know more about it !

Handling Stress Effects For Nanotechnology



Stress Effects Parameters: SA, SB, SA_{REF}, SB_{REF}, …
W, NF, AS, AD, PS, PD, …

Conclusions

- A *Parameterized* Analogue Circuit in introduced.
- *A Hierarchical Sizing & Biasing Methodology* is proposed to size this circuit.
- A *structured* approach is proposed providing designers with *full control* and *sufficient insight*.
- Knowledge documentation, reuse and portability are achieved.
- A need for *analogue structured analyses types.*
- *Layout is taken into account*

Thank you for your kind attention. Questions ?