Lecture 4: STRUCTURED ASIC's

CSE690
Jennifer Wong

Taken from: Dan Lander, Haru Yamamoto, Shane Erickson

Contents

- Introduction
- Overview
- Architectures
- Advantages / Disadvantages
- Design Methodology
  - Case study: clock signal aware design
- Conclusions

Introduction

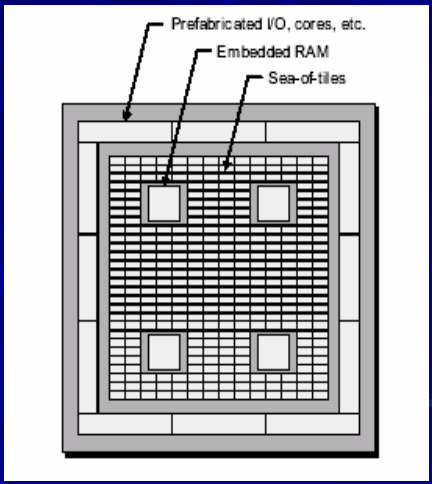
- A Structured ASIC falls between an FPGA and a Standard Cell-based ASIC
- Structured ASIC's are used mainly for mid-volume level designs
- The design task for structured ASIC's is to map the circuit into a fixed arrangement of known cells

Properties

- Low NRE cost
  - Implementation engineering effort
  - Mask tooling charges
- High performance
- Low power consumption
- Less Complex
  - Fewer layers to fabricate
- Small marketing time
  - Pre-made cell blocks available for placing

Architecture

- Two Main Levels
  - Structured Elements
    - Combinational and sequential function blocks
    - Can be a logical or storage element
  - Array of Structured Elements
    - Uniform or non-uniform array styles
    - A fixed arrangement of structured elements



Main Implementation Steps

1. RTL Design
   - Register transfer level design
2. Logical synthesis
   - Maps RTL into structured elements
3. Design for Test insertion
   - Improves testability and fault coverage
4. Placement
   - Maps each structured element onto array elements
   - Places each element into a fixed arrangement

Main Implementation Steps

5. Physical synthesis
   - Improves the timing of the layout
   - Optimizes the placement of each element
6. Clock synthesis
   - Distributes the clock network
   - Minimizes the clock skew and delay
7. Routing
   - Inserts the wiring between the elements

Implementation Issues

- Logical synthesis, placement and routing all depend on the target structure element architecture and hence add more complexity to the design process.
- The completeness of the target structured ASIC library also affects what specifically can be implemented from the design.

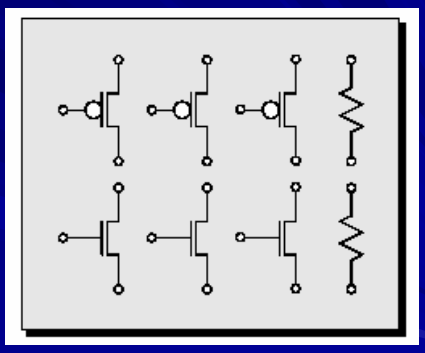
FPGA Vs. Standard Cell ASIC

Easy to Design	Difficult to Design
Short Development Time	Long Development Time
Low NRE Costs	High NRE Costs
Design Size Limited	Support Large Designs
Design Complexity Limited	Support Complex Designs
Performance Limited	High Performance
High Power Consumption	Low Power Consumption
High Per-Unit Cost	Low Per-Unit Cost (at high volume)

Structured ASIC's Combine the Best of Both Worlds

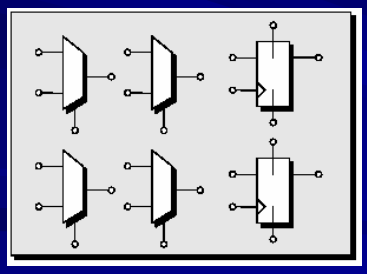
Structured ASIC Architectures
Fine-Grained

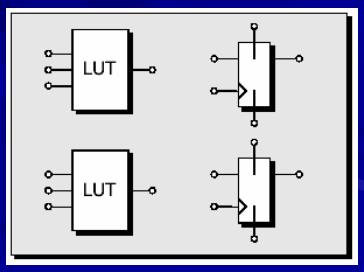
- Structured elements contain unconnected discrete components
- Could include transistors, resistors, and others



Structured ASIC Architectures
Medium-Grained

- Structured elements contain generic logic
- Could include gates, MUX's, LUT's or flip-flops





Structured ASIC Architectures
Hierarchical

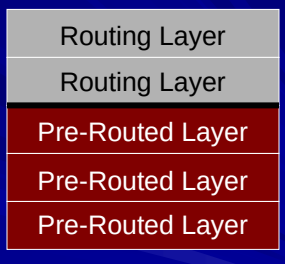
- Use mini structured elements that contain only gates, MUX's, and LUT's
- It does not contain storage elements like flip-flops
- This mini element is then combined with registers or flip-flops

Architecture Comparison

- Fine-grained requires many connections in and out of a structured element
- Higher granularities reduce connections to the structured element but decreases the functionality it can support
- Clearly, each individual design will benefit differently at varying granularities

Structured ASIC Advantages

- Largely Prefabricated
  - Components are “almost” connected in a variety of predefined configurations
  - Only a few metal layers are needed for fabrication
  - Drastically reduces turnaround time



Structured ASIC Advantages

- Easier and faster to design than standard cell ASIC's
  - Multiple global and local clocks are prefabricated
  - No skew problems that need to be addressed
  - Signal integrity and timing issues are inherently addressed

Structured ASIC Advantages

- Capacity, performance, and power consumption closer to that of a standard cell ASIC
- Faster design time, reduced NRE costs, and quicker turnaround
- Therefore, the per-unit cost is reasonable for several hundreds to 100k unit production runs

Structured ASIC Disadvantages

- Lack of adequate design tools
  - Expensive
  - Altered from traditional ASIC tools
- These new architectures have not yet been subject to formal evaluation and comparative analysis
  - Tradeoffs between 3-, 4-, and 5-input LUT's
  - Tradeoffs between sizes of distributed RAM

Technology Comparison

- Generally speaking
  - 100:33:1 ratio between the number of gates in a given area for standard cell ASIC's, structured ASIC's, and FPGA's, respectively
  - 100:75:15 ratio for performance (based on clock frequency)
  - 1:3:12 ratio for power

Design Tools

- Many companies are using existing standard cell-based CAD tools
  - They add product specific placement tools
  - To maximize benefits, we need CAD tools designed specifically for structured ASIC's
  - Need updated algorithms to exploit the modularity of structured ASIC's
  - Clock aware design
- Need architectural evaluation and analysis tools

Case Study: NEC ISSP

Problem Formulation

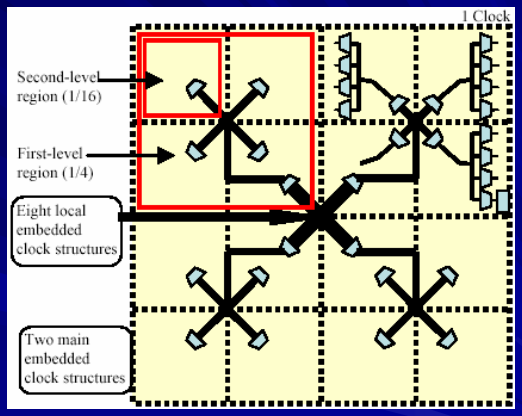
- Prefabricated
  - Standard Cells, Flip-Flops, DSP, Memory and other IP (Intellectual Properties)
  - Interconnects for modules, DFT circuit, and clocks
- Physical Design (Placement) Problems
  - Modules are already embedded
  - Mapping problem

After Logical Synthesis

- Different clock signals for different groups of modules (FFs)
- Multiple clock signals in one chip
- Must perform clock-aware placement

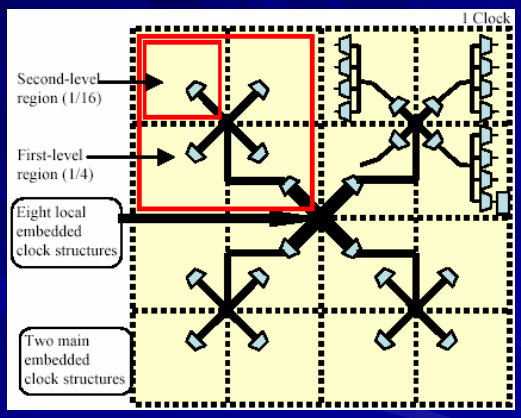
Embedded Clocks

- 2 main clocks
  - Accessible from anywhere



Embedded Clocks

- 8 local clocks
  - Chip divided into 4 regions
  - 4 local clocks can be assigned to each region
  - Region divided into 4 sub regions



  - Each subregion assigned 2 local clocks

More Clock Signals Needed?

- Use a custom layer to implement an additional clock signal
- Custom layer is limited, so it many not be feasible
- Try to avoid this as much as possible

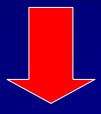
Assigning Clock Signal

- Main/local clock assignment
  - Which clock should be the main clock?
  - Which clock should be the local clock?
- Region clock assignment
  - Which local clock should be assigned to each region?
- Do we need a custom clock?
  - We generally do not want it
- 3 methods to solve this

Number Based Heuristics

Method 1

- Assign 2 most used clocks as main clocks
- Other clocks are local clocks
- Assign local clocks to subregions based on I/O positions
- Perform placement



Problems

- May not be possible
- What about delay optimization?

Placement Based Clock Optimization
Method 2

1. Perform placement without clock constrains
   - Based on interconnect delays
2. Clock assignment as result of step 1
   - Which clock should be the main clock?
   - Which local clock should be assigned to each region?
3. Move violating FFs to other regions
4. Map FFs to embedded positions

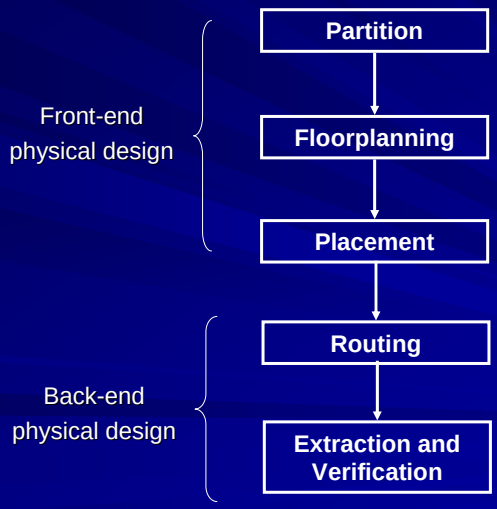
Placement Based Clock Optimization
Method 2

Problems

- Moving FFs to different regions will drastically increase interconnect delays
- Huge performance loss

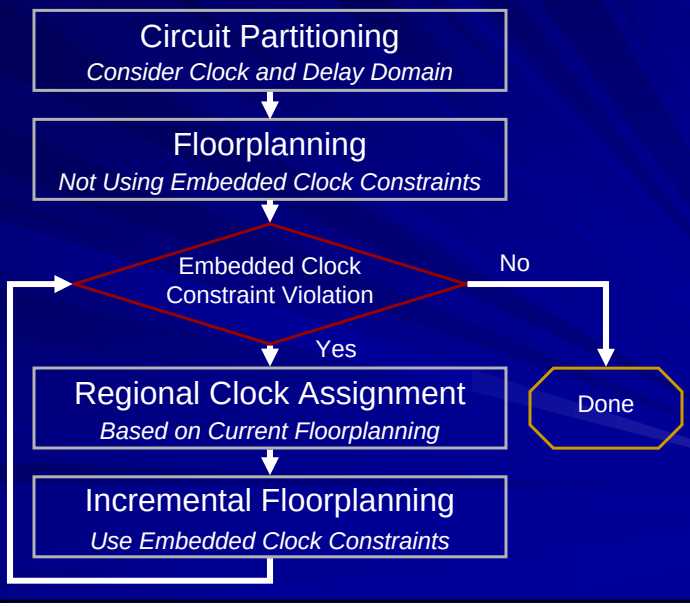
How do we solve this?

Design Flow from 1st day



Floorplanning Based Clock Optimization

Method 3



In Structured ASIC's

- Partitioning
  - Create clusters of cells and FFs based on clock, delay, and other constraints
- Floorplanning
  - Assigning the clusters to each region
- Incremental Floorplanning
  - Move violating FFs to other regions

With Partitioning and Floorplanning

- Less FFs moved
  - Less damage to performance

Method 1: Number-based heuristics
Method 2: Placement-based embedded clock optimization
Method 3: Floorplan-based embedded clock optimization

	# F/Fs moved in incremental placement
Method 2	1821
Method 3	0

Conclusions

- Enhancements should be made to existing EDA tools to achieve a better performance result on structured ASIC architectures
- The structured ASIC is a revolution to businesses, but another evolution of ASIC implementation
- The structured ASIC was developed to bridge the gap between the FPGA and the Standard Cell-based ASIC

References

- T. Okamoto, T. Kimoto, N. Maeda, “Design Methodology and Tools for NEC Electronics - Structured ASIC ISSP", [p. 90] Proceeding of the 2004 international symposium on Physical design.
- B. Zahiri, “Structured ASICs: Opportunities and Challenges,” Proceedings of the 21st International Conference on Computer Design (ICCD’03).
- K. Wu, Y. Tsai, “Structured ASIC, Evolution or Revolution?,” Faraday Technology Corporation, Proceedings of the 2004 International Symposium on Physical Design.