Forward Error Correction in Sensor Networks

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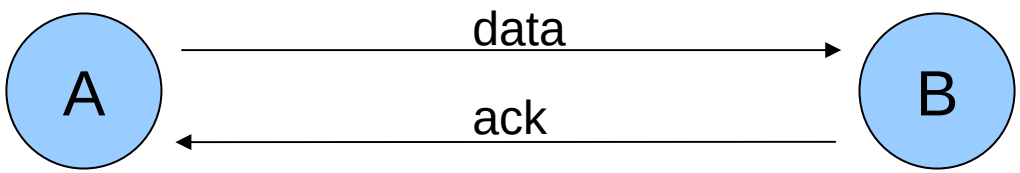
Motivation

- **Packet errors occur in WSN.**
  - Error recovery is required for correct delivery.
- **Questions.**
  - What kinds of error recovery method?
  - What level of error recovery capability?

Two methods for error recovery

- **ARQ (Automatic Repeat reQuest)**
  - A sends, and B acks.



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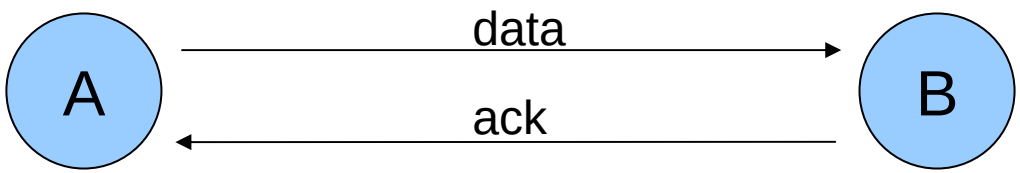

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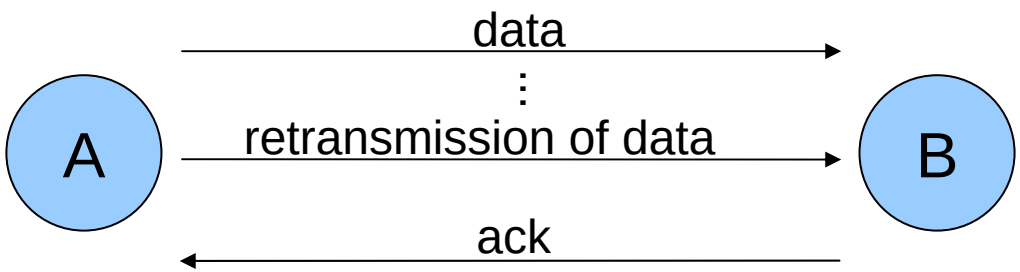

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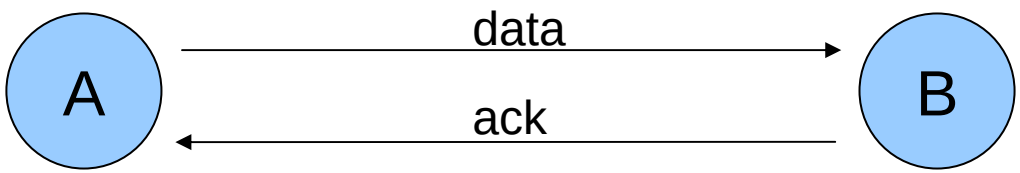

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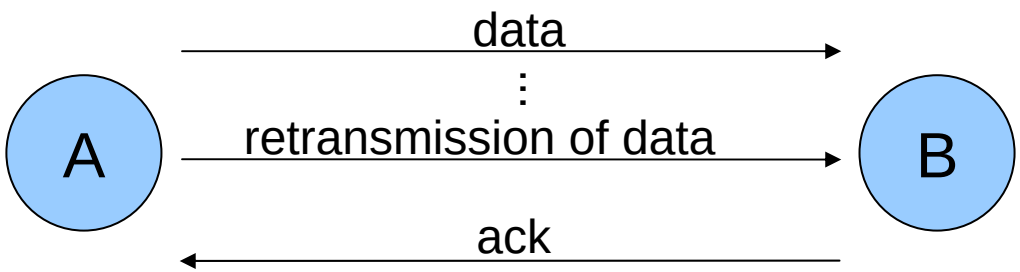

  - TX cost increases with (#-nodes, #-TX).

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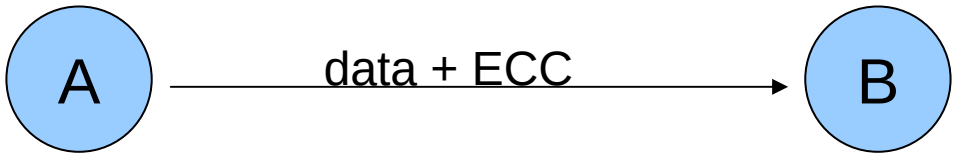

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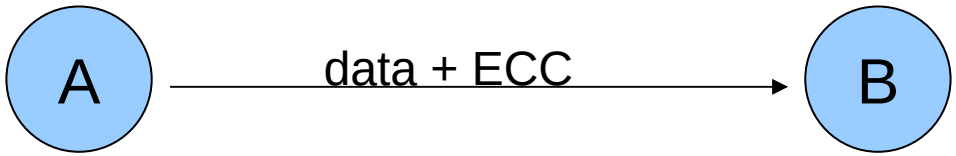

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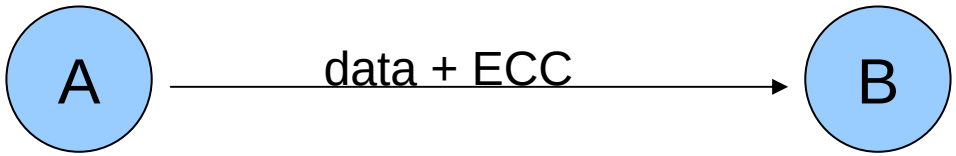
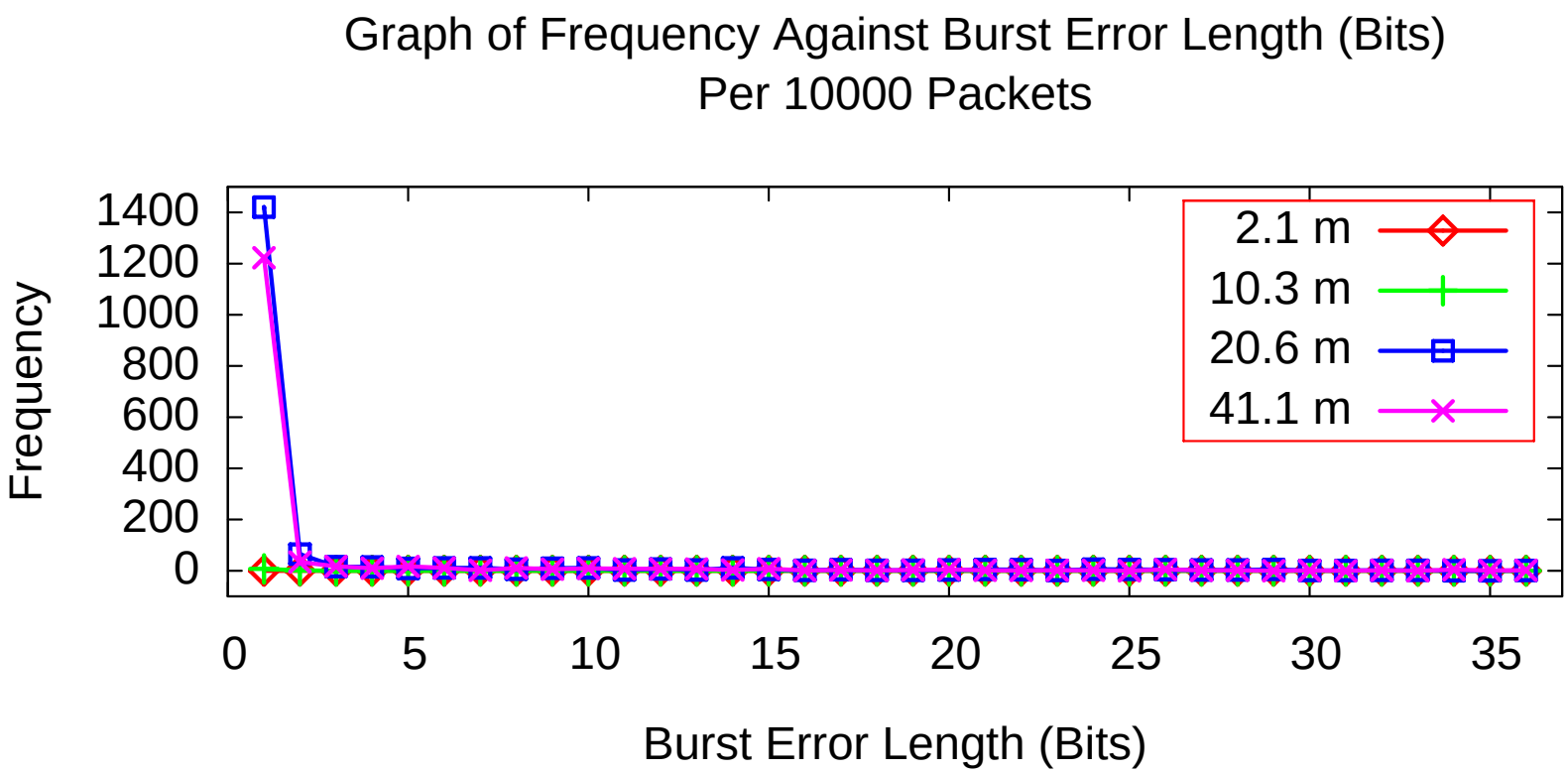


  - Preferable in broadcast and multi-hop network.
  - We focus on FEC for WSN.

Choosing Right ECC for WSN

- **Preliminary Experiment**
  - Most packet errors are 1-bit or 2-bit.



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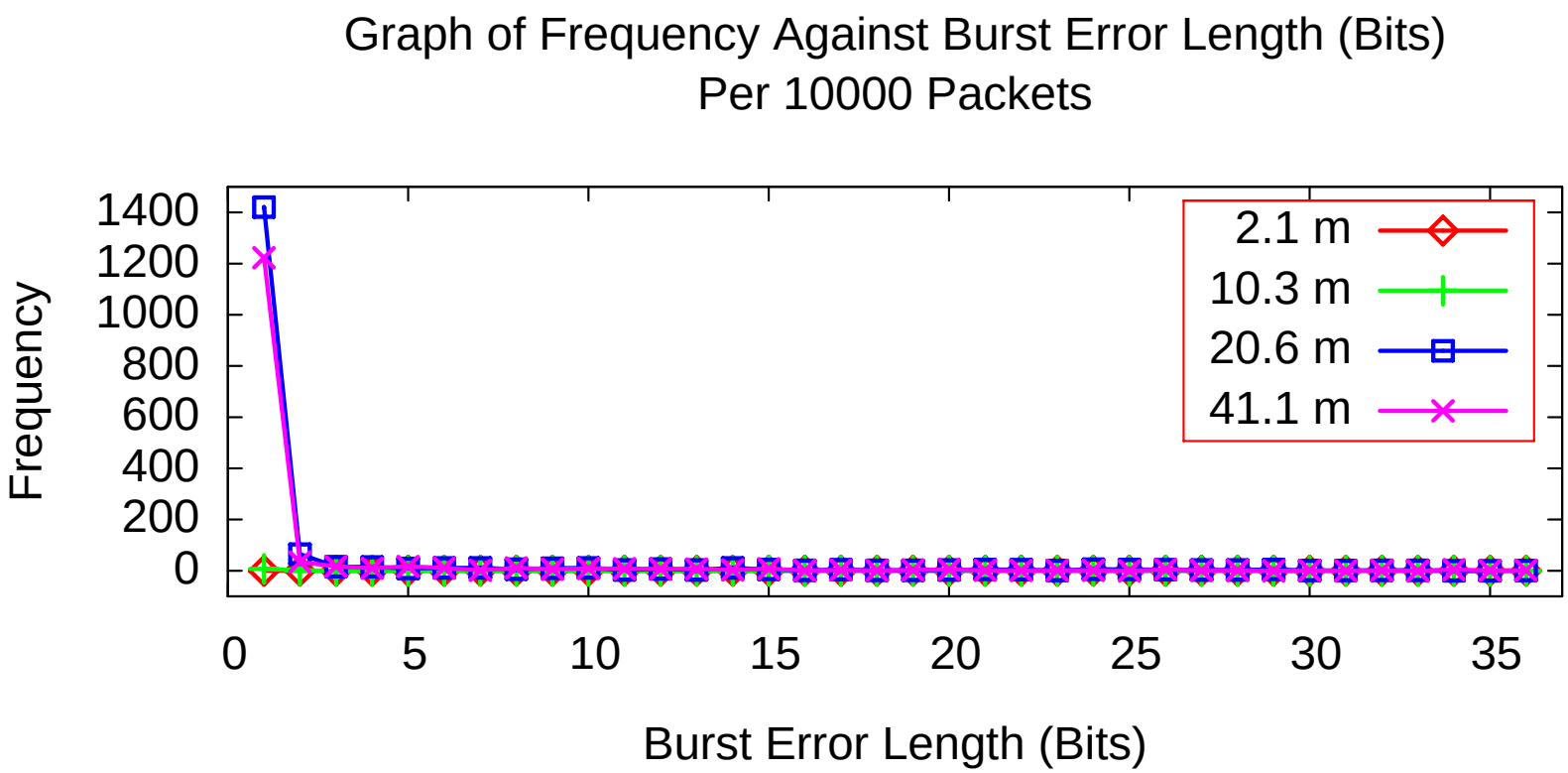

- **Our approach: 1-bit & 2-bit ECC for WSN.**

Organization

- **Background**
- **Theory**
- **Implementation**
- **Experiment**
- **Conclusion**

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  - Outdoor & indoor tests for several ECC.
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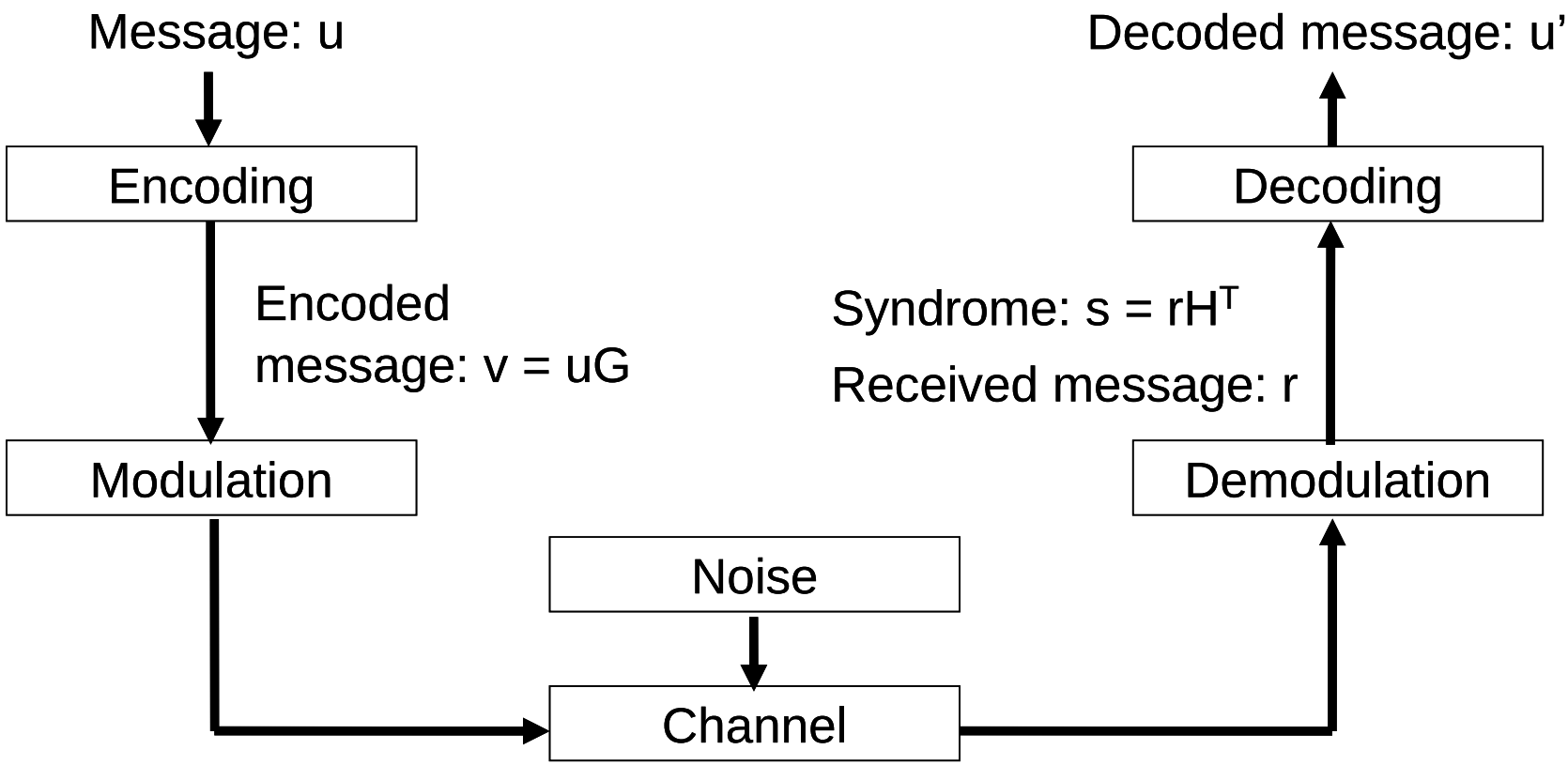
  - Better error-correction capability.
  - Complex computation, larger memory space.
- **1-bit ECC code for Mica (RFM TR1000)**
  - Handles both 1-bit ECC & DC-balancing.
  - Not efficient for radio that already supports DC-balancing (e.g. CC1000).

Theory

- **Based on linear block code over GF(2).**



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- **Decoding:**
  - Decodes (k+r)-bit received data r into k-bit data u'.
  - Calculates syndrome **s** = **r**H^T (r: received msg, H: parity) for locating bit errors.

Theory

- **Locating bit errors:**
  - $s = rH^T = (v+e)H^T = uGH^T + eH^T = eH^T$
  - $GH^T = [I_k : C][C^T : I_r]^T = C + C = 0$
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  - Any non-zero syndrome **s** implies an error.

- **Correcting bit errors:**
  - If **s** matches *i*-th column of H, invert *i*-th bit of **r**.
  - Otherwise, bit error is not correctable.

Odd-weight-column code

- **Odd-weight-column code is SECDED.**
  - Single-Error-Correction & Double-Error-Detection.
- **Ex: odd-weight-column w. k = 8, r = 5.**

$$G = [I_8 : C] = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

$$H = [C^T : I_5] = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

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- **Encoding:** let message $u = [0100 \quad 0010]$
  - Then, codeword $v = uG = [0100 \quad 0010 \quad 10111]$

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  - Received bits $v' = [0000 \quad 0010 \quad 10111]$

$$s = v' H^T = [01011]$$

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- **Detecting error:** $s = v'H^T = [01011]$
  - **s** matches 2nd column of H ➔ 2nd bit of **v** inverted.

$$H = [C^T : I_5] = \begin{bmatrix} & & 1 & 1 & 1 & 1 & 1 & 1 & 1 & & & & \\ & 1 & & & 1 & 1 & 1 & 1 & & 1 & & & \\ 1 & & 1 & 1 & & & 1 & 1 & & & 1 & & \\ 1 & 1 & & 1 & & 1 & & 1 & & & & 1 & \\ 1 & 1 & 1 & & 1 & & & 1 & & & & & 1 \end{bmatrix}$$

Odd-weight-column code

- **Error correction:**
  - Calculating correct codeword.

$$v = v' + [0100 \quad 0000 \quad 00000]$$

$$= [0000 \quad 0010 \quad 10111] + [0100 \quad 0000 \quad 00000]$$

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  - Since first k-columns of G is identity matrix,

$$uG = [0100 \quad 0010 \quad 10111]$$

$$u = [0100 \quad 0010]$$

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  - Can correct 2-bit error and detect 3-bit error (DECTED).
  - Similar to SECDED except decoding.
    - If syndrome **s** matches i^{th} column of H, invert i^{th} bit of r.
    - If **s** matches sum of ith column of H and j^{th} column of H, invert i^{th} and j^{th} bits of **r**.
    - Otherwise, bit error is not correctable.

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- **Detecting error:** $s = v'H^T = [1010 \quad 1111]$

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- **Three versions of ECC (1-bit & 2-bit)**
  - SECDEC (13, 8) : 8-bit data, 13-bit codeword
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- **Implemented within MAC layer providing transparent packet interface.**
- **Lookup table of H for faster decoding.**

Implementation

- **Overhead in bytes to transmit due to ECC.**
  - Assumes 20-byte preamble & 36-byte payload.
  - $r_{ecc} = \dfrac{\text{Bytes to be sent}}{\text{Bytes to be encoded}}$

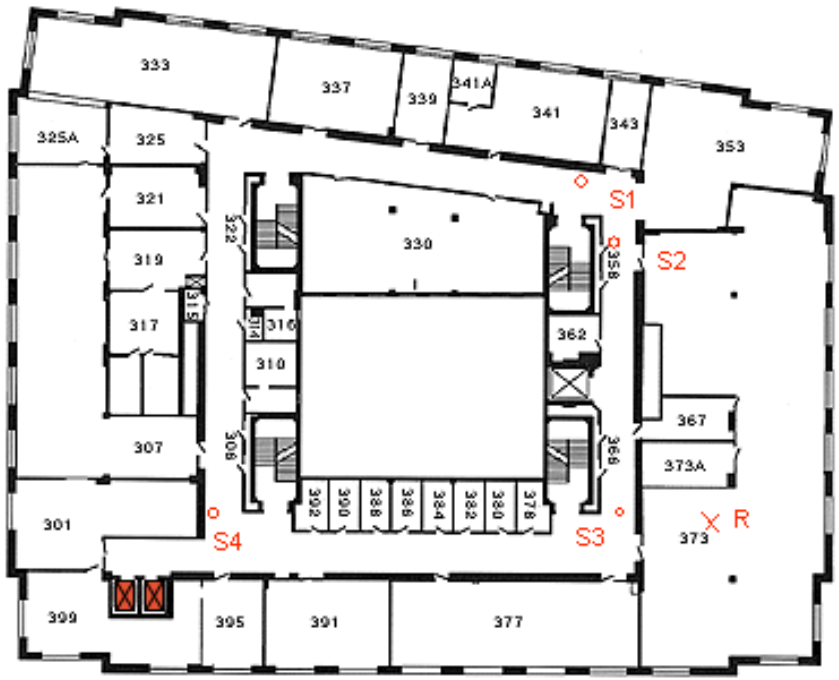
	SECDED (8,13)	SECDED (30,24)	DECTED (16,8)
r_{ecc}	2byte / 1byte	4byte / 3byte	2byte / 1byte
Overhead	64.3%	21.4%	64.3%

Experimental Setup

- **Four versions of ECC MAC were tested**
  - NO FEC
  - SECDED(13,8)
  - SECDED(30,24)
  - DECTED(16,8)
- **TX node sends a packet 5,000 times.**
- **Received data is logged for analysis.**

Experimental Setup

- **Outdoor test**
  - Sender / receiver were 183m apart L.O.S.
- **Indoor test**
  - Four different sender locations in Cory Hall.



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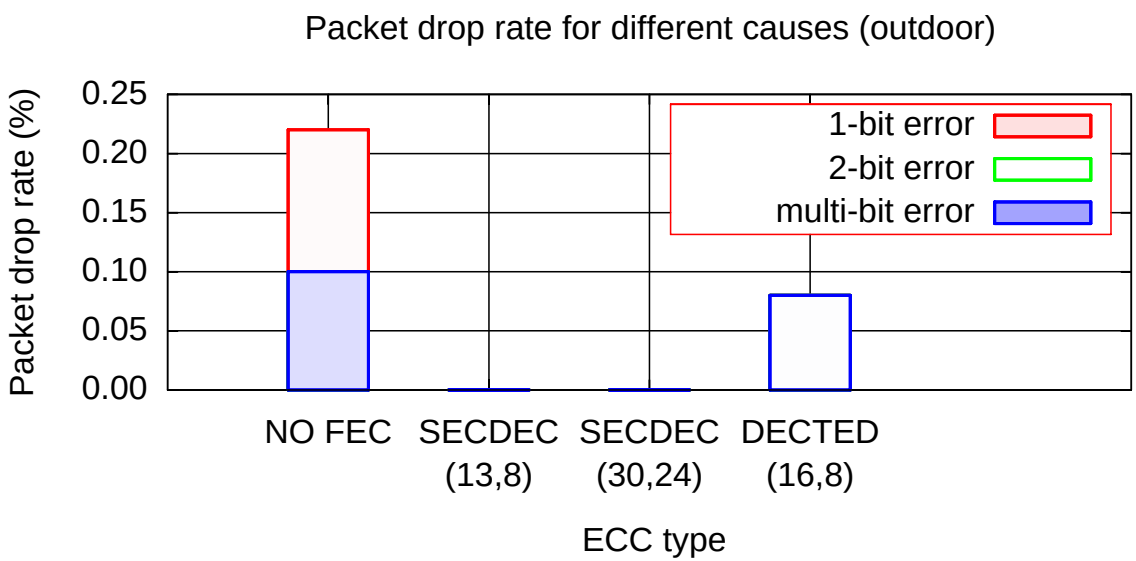
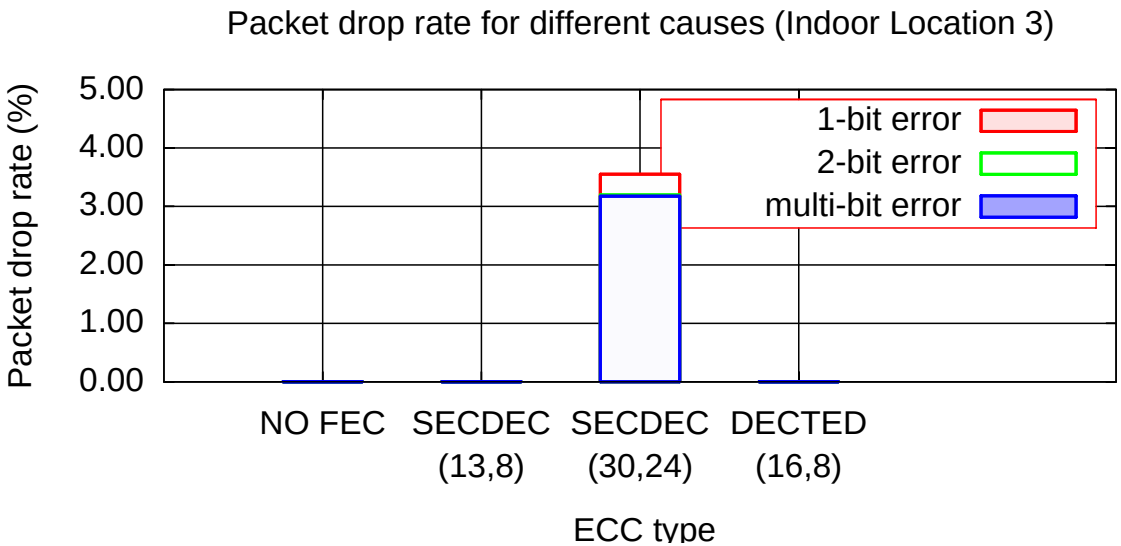
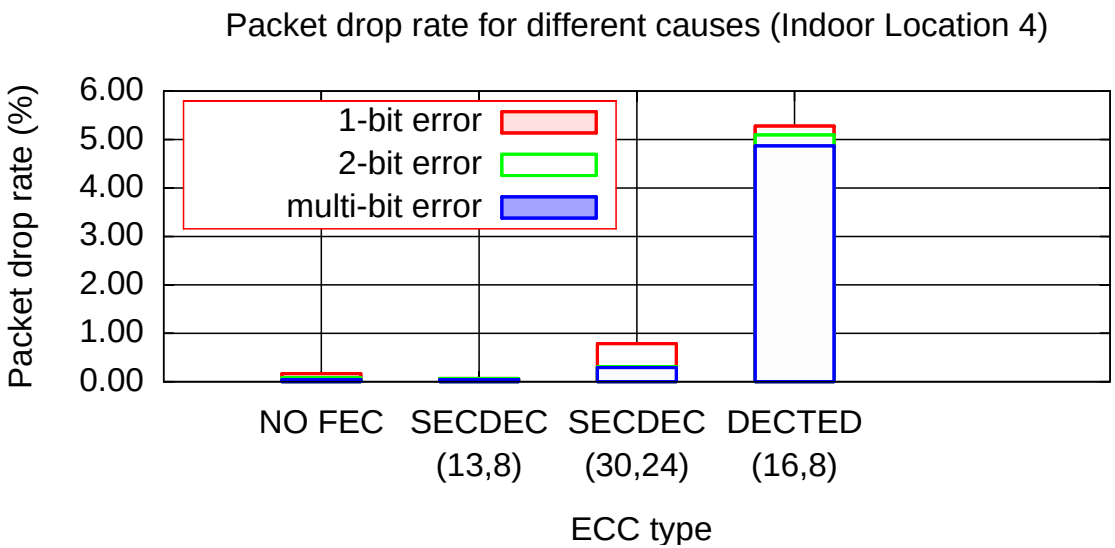
- **Outdoor: ECC reduces PER to zero.**



Result (Packet Drop)

- **Indoor: PER > 0 due to multiple-bit errors.**





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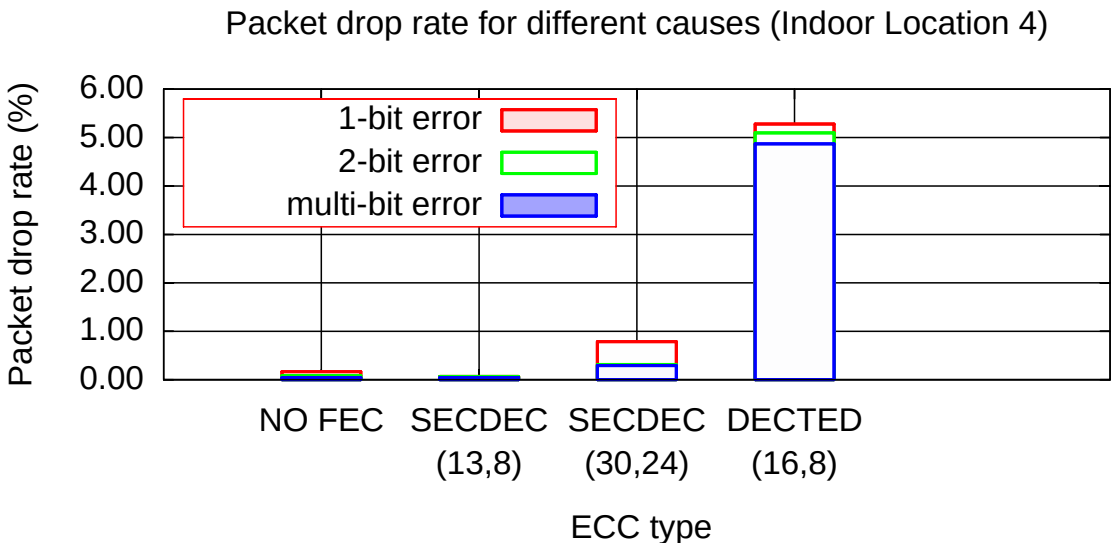

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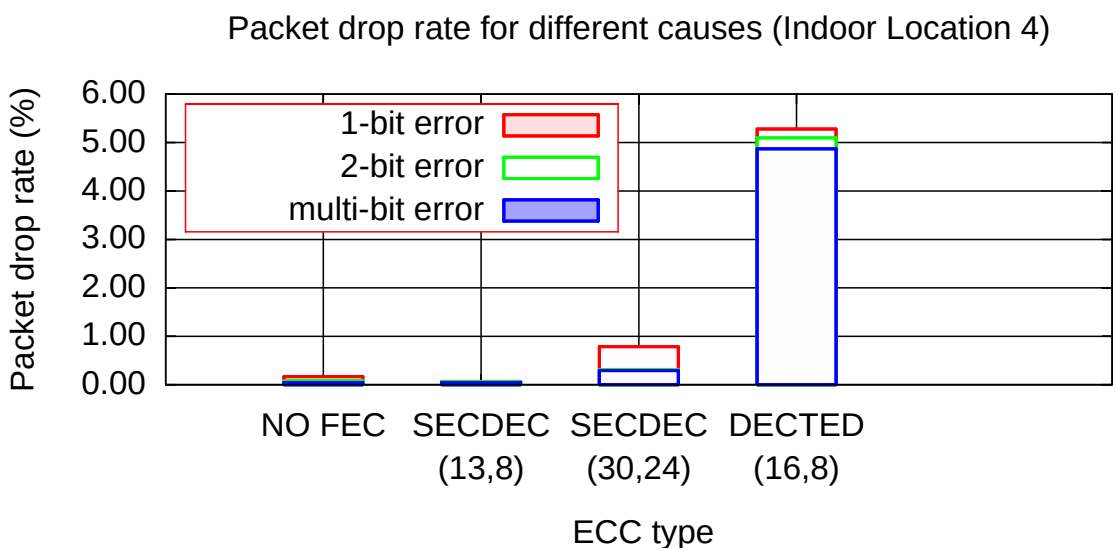

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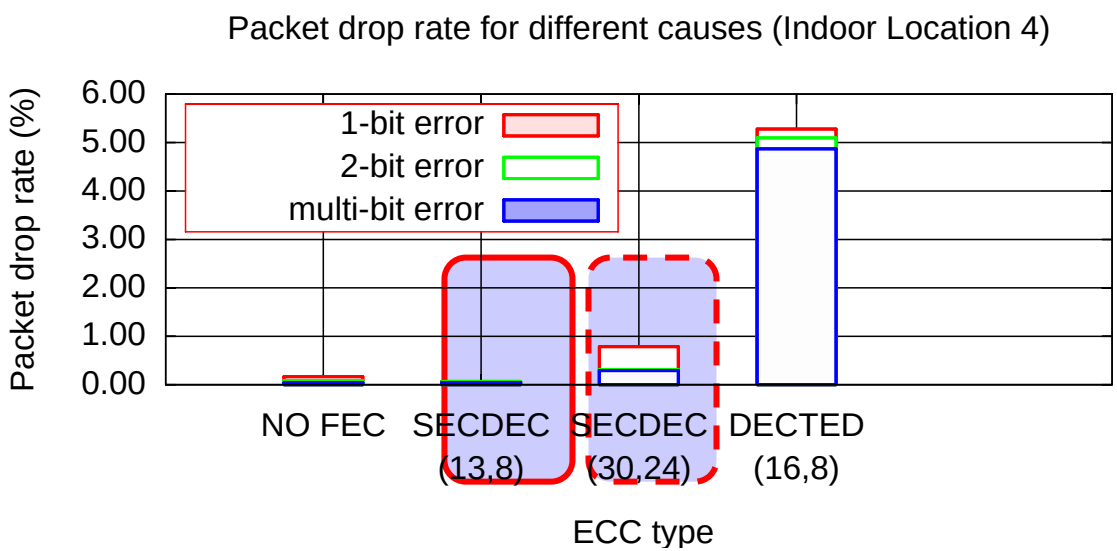

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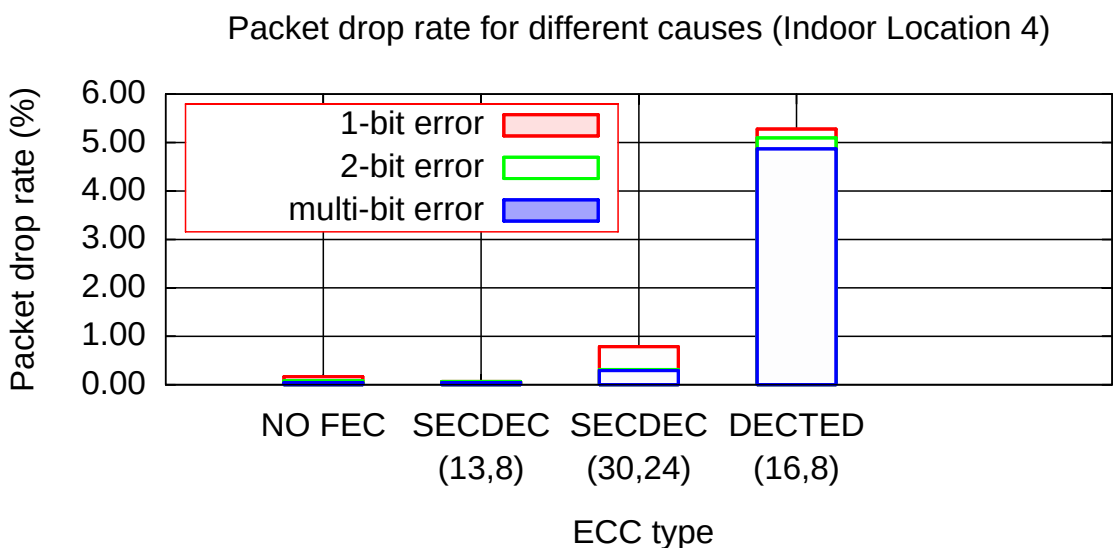

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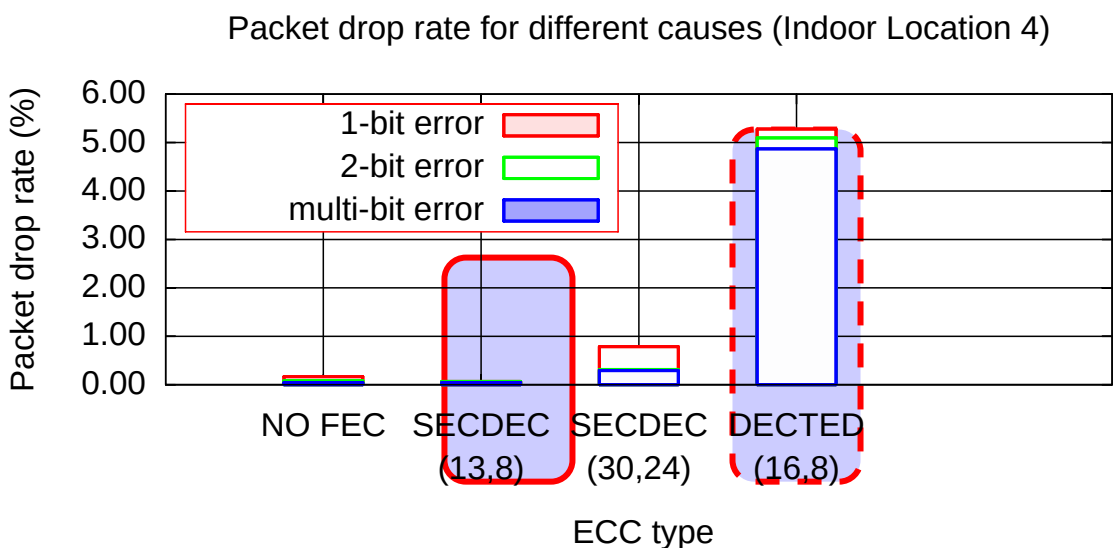
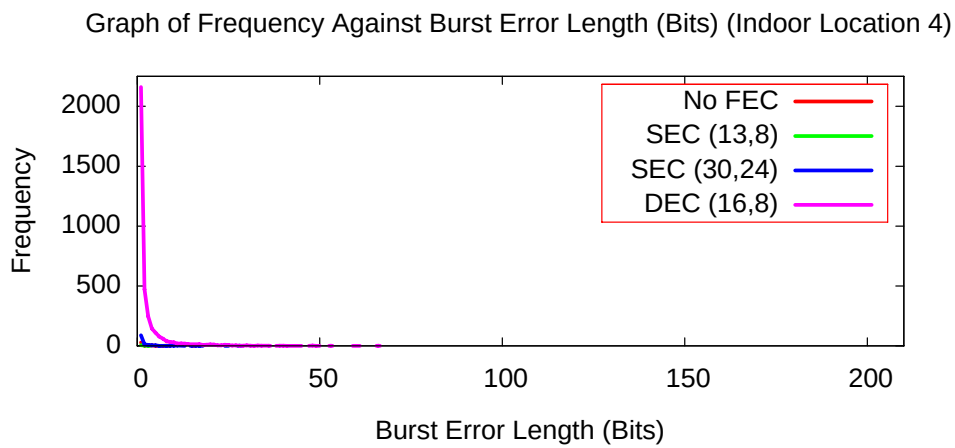
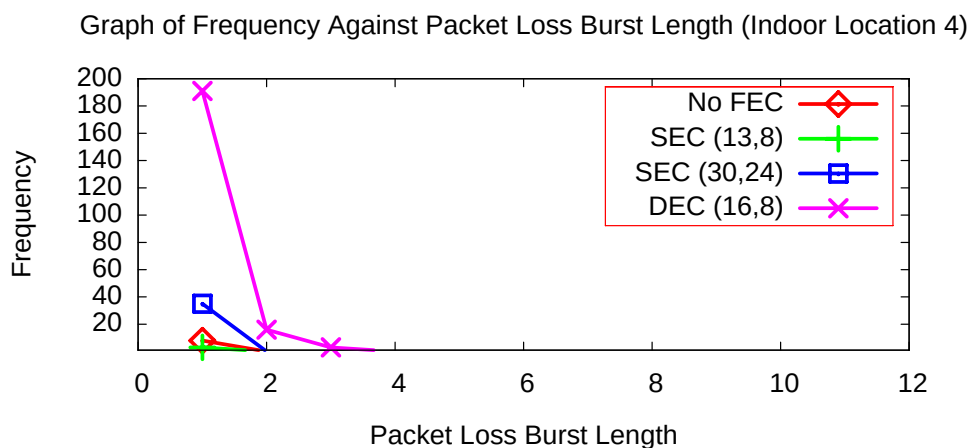


Burst bit errors & packet losses

- **Burst bit errors happen, but frequency of multiple packet drops is low.**
  - A few retransmissions would be enough.





Conclusion

- **A few versions of 1-bit & 2-bit ECC were implemented and tested on CC1000.**
- **ECC reduces packet drop rate, but not effective under burst bit errors.**
- **Under burst bit errors, a few re-TX can be used to further reduce packet drop rate.**