

CS137: Electronic Design Automation

Day 6: October 10, 2005
Static Timing Analysis
and Multi-Level Speedup



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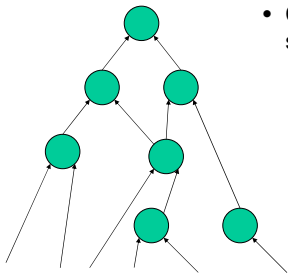
Today

- Topological Worst Case
 - not adequate (too conservative)
- Sensitization Conditions
- Timed Calculus
- Delay-justified paths
 - Timed-PODEM
- Speedup

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Topological Worst-Case Delay

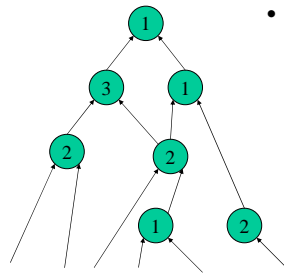


- Compute ASAP schedule
 - Take max of arrival times
 - Apply node Delay

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Topological Worst-Case Delay

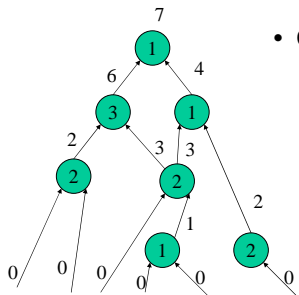


- Node Delays

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Topological Worst-Case Delay



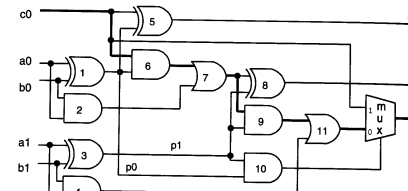
- Compute Delays

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Conservative

- Topological Worst-Case Delay can be conservative

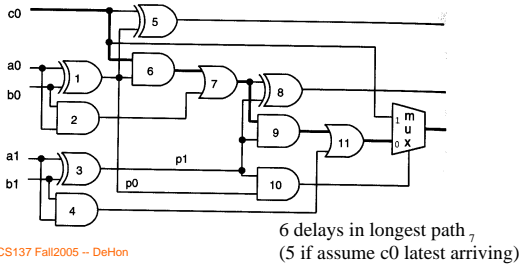


[Fig/Examples from Logic Synthesis by Devadas, Gosh, Keutzer 1994]

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Example

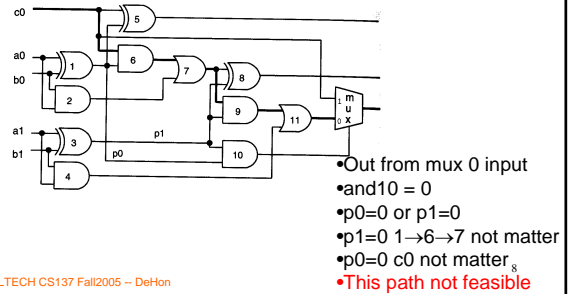
- Assume each gate 1:



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Example

- Is this path possible?



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False Paths

- Once consider logic for nodes
 - There are logical constraints on data values
- There are paths which cannot logically occur
 - Call them **false paths**

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What can we do?

- Need to assess what paths are real
- Brute force
 - for every pair of inputs
 - compute delay in outputs from in1→in2 input transition
 - take worst case
- Expensive:
 - 2^{2n} delay traces

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Alternately

- Look at single vector and determine what controls delay of circuit
 - I.e. look at values on path and determine path *sensitized* to change with input

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Controlled Inputs

- Controlled input to a gate:
 - input whose value will determine gate output
 - e.g.
 - 0 on a AND gate
 - 1 on a OR gate

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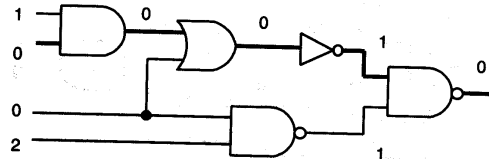
Static Sensitization

- A path is statically sensitized
 - if all the side (non-path) inputs are non-controlling
 - I.e. this path value flips with the input

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Statically Sensitized Path

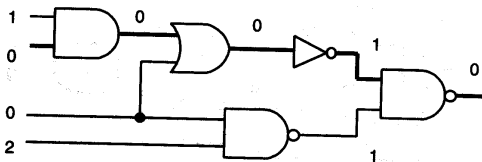


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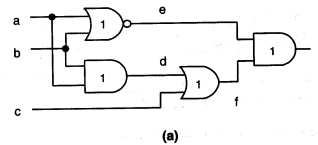
Sufficiency

- Static Sensitization is **sufficient** for a path to be a **true** path in circuit

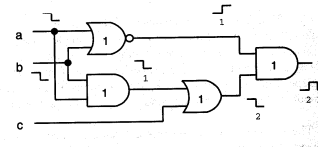


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...but not necessary



Paths of length 3 not statically sensitizable.



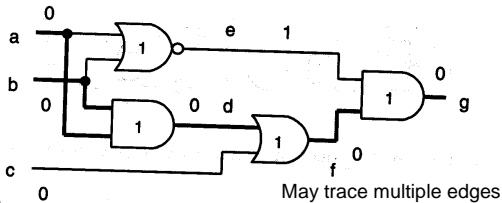
But there is a true path of delay 3.

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Static Co-sensitization

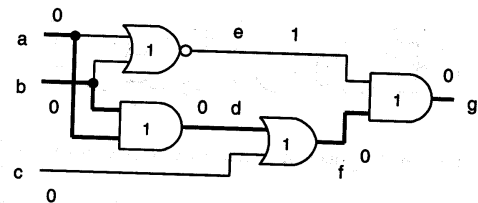
- Each output with a controlled value
 - has a controlling value as input on path
 - (and vice-versa for non-controlled)



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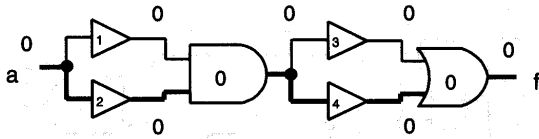
Necessary

- Static Co-sensitization is a **necessary** condition for a path to be true



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...but not sufficient

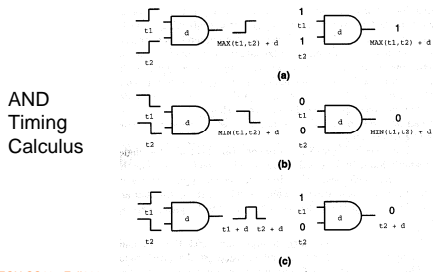


Cosensitize path of length 6.
Real delay is 5.

Combining

- Combine these ideas into a timed-calculus for computing delays for an input vector

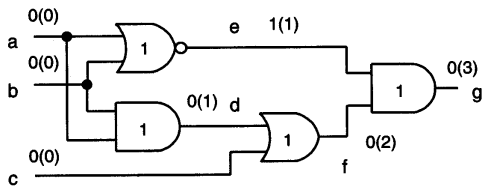
Computing Delays



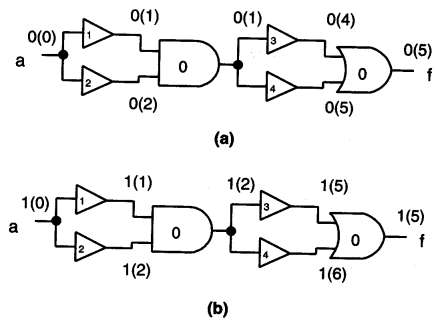
Rules

- If gate output is at a controlling value, pick the minimum input and add gate delay
- If gate output is at a non-controlling value, pick the maximum input and add gate delay

Example (1)



Example (2)



Now...

- We know how to get the delay of a single input condition
- Could:
 - find critical path
 - search for an input vector to sensitize
 - if fail, find next path
 - ...until find longest true path
- May be $O(2^n)$

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Better Approach

- Ask if can justify a delay greater than T
- Search for satisfying vector
 - ...or demonstration that none exists
- Binary search to find tightest delay

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Delay Computation

- Modification of a testing routine
 - used to justify an output value for a circuit
- PODEM
 - backtracking search to find a suitable input vector associated with some target output
 - Simple a branching search with implication pruning
 - Heuristic for smart variable ordering

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Search1

- Takes in list of nodes to satisfy
- If all satisfied \rightarrow done
- Backtrace to set next PI
- if inconsistent PI value
 - try inverting this PI call Search2
- else
 - search to set next PI
 - if fail
 - try inverting and Search2

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Search2

- ;; same idea, but this one not flip bit
- ;; because already tried inverted value
- If no conflict
 - search to set next PI
- otherwise
 - pass back failure

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Backtrace

- Follow back gates w/ unknown values
 - sometimes output dictate input must be
 - (AND needing 1 output; with one input already assigned 1)
 - sometimes have to guess what to follow
 - (OR with 1 output and no inputs set)
 - Uses heuristics to decide what to follow

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Example

Try justify $g=1$

(a)

(b)

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Example

(a)

(b)

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For Timed Justification

- Also want to compute delay
 - on incompletely specified values
- Compute bounds on timing
 - upper bound, lower bound
 - Again, use our timed calculus
 - expanded to unknowns

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Delay Calculation

$i_1 \rightarrow$ $i_2 \downarrow$	0	1	2
0	0 $MIN(l_1, l_2) + d$ $MIN(u_1, u_2) + d$	0 $l_2 + d$ $u_2 + d$	0 $MIN(l_1, l_2) + d$ $u_2 + d$
1	0 $l_1 + d$ $u_1 + d$	1 $MAX(l_1, l_2) + d$ $MAX(u_1, u_2) + d$	2 $l_1 + d$ $MAX(u_1, u_2) + d$
2	0 $MIN(l_1, l_2) + d$ $u_1 + d$	2 $l_2 + d$ $MAX(u_1, u_2) + d$	2 $MIN(l_1, l_2) + d$ $MAX(u_1, u_2) + d$

AND rules

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Timed PODEM

- **Input:** value to justify and delay T
- **Goal:** find input vector which produces value and exceeds delay T
- Algorithm
 - similar
 - implications check timing as well as logic

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Example

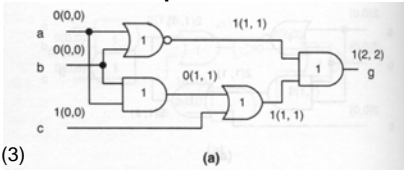
Justify 1(3)

(a)

(b)

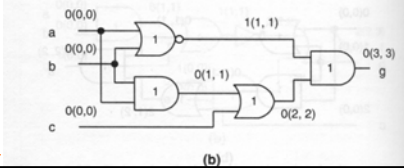
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Example



Fail to justify 1(3)

Justify 0(3)



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Search

- Less than 2^n
 - pruning due to implications
 - here saw a must be 0
 - no need to search 1xx subtree

Speed Up

(sketch flavor)

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Speed Up

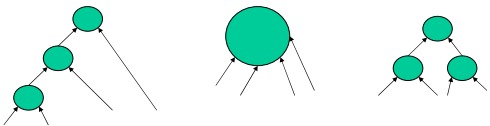
- Start with area optimized network
- Know target arrival times
 - Know delay from static analysis
- Want to reduce delay of node

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Basic Idea

- Improve speed by:
 - Collapsing node(s)
 - Refactoring collapsed subgraph to reduce height



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Speed Up

- While (delay decreasing, timing not met)
 - Compute delay (slack)
 - Static timing analysis
 - Generate network close to critical path
 - Weight nodes in network
 - Compute **mincut** of nodes on weighted network
 - Partial collapse and timing redecompose on cut nodes

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Weighted Cut

- Want to minimize area expansion
- Want to maximize likely benefit
 - Prefer nodes with varying input times
 - Prefer nodes with critical path on longer paths

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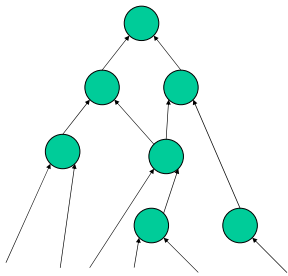
Timing Decomposition

- Extract area saving kernels that do not include critical inputs to node
- When decompose (e.g. into nand2's) similarly balance with critical inputs closest to output

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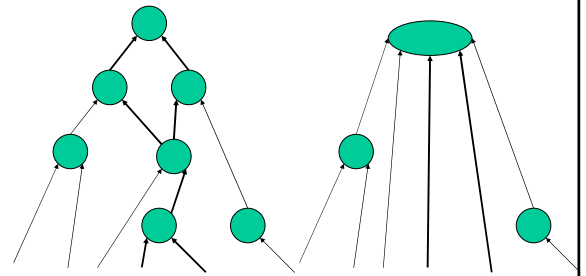
Example



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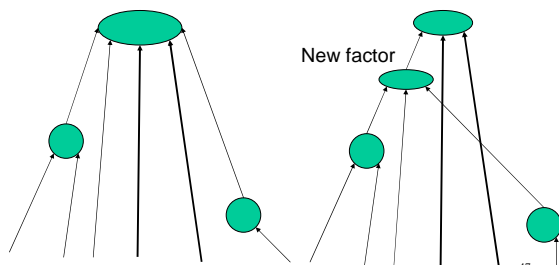
Example



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Example



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Big Ideas

- Topological Worst-case delays are conservative
 - Once consider logical constraints
 - may have false paths
- Necessary and sufficient conditions on true paths
- Search for paths by delay
 - or demonstrate non existence
- Search with implications
- Iterative improvement