Fast Characterization of PBTI and NBTI Induced Frequency Shifts under a Realistic Recovery Bias Using a Ring Oscillator Based Circuit

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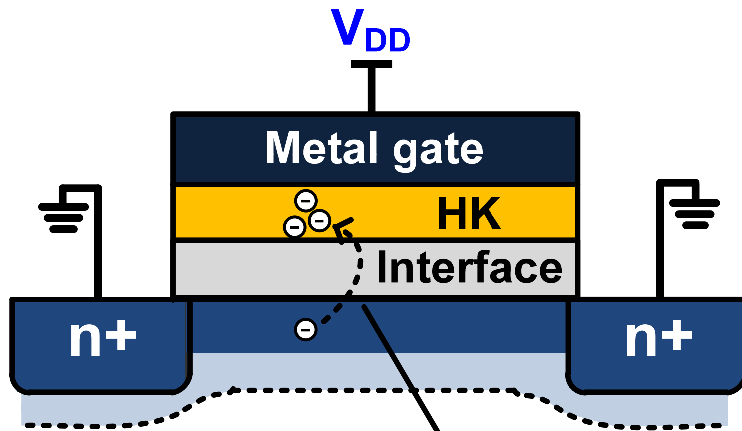
Purpose

- Separately characterize impact of PBTI and NBTI on frequency under DC and AC
- Design an on-chip monitor to support realistic recovery condition and precise and fast measurement

Outline

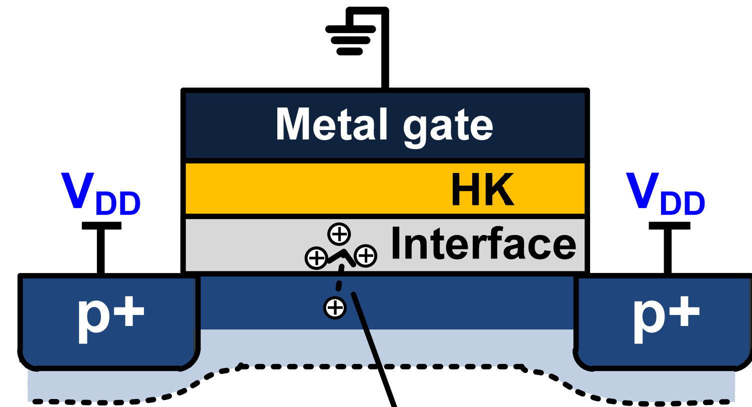
- **NBTI and PBTI Monitoring in HKMG Process and Prior Arts**
- **NBTI and PBTI Aging Monitor Design**
- **Results from HKMG Test Chip**
- **Summary**

PBTI and NBTI in HKMG



Electron trapping mostly in HK layer

PBTI in HKMG stack



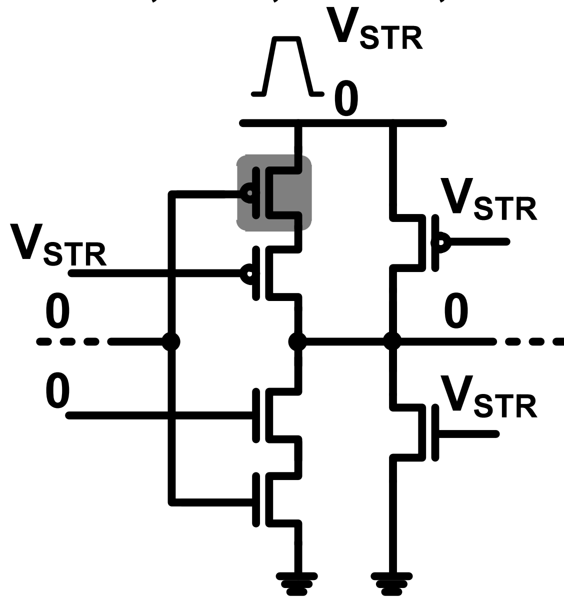
Trap generation, and hole trapping in interface layer

NBTI in HKMG stack

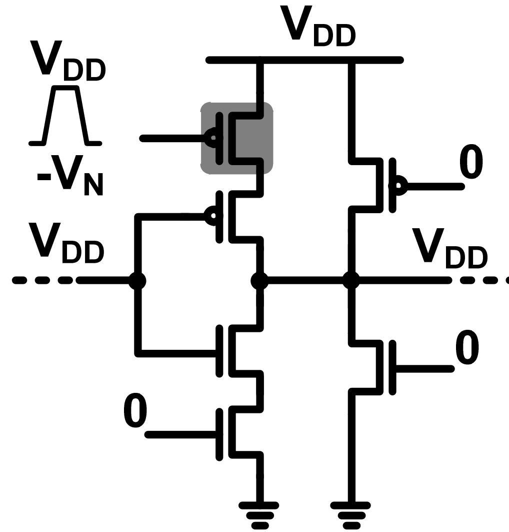
- **NBTI and PBTI have different magnitude and behavior due to different mechanism and trap location**
- **The difference between NBTI and PBTI is highly dependent on the technology**
- **NBTI and PBTI need to be characterized separately**

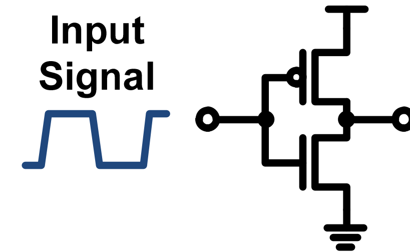
Previous Work on PBTI/NBTI Monitoring

J. Kim, *et al.*, ICICDT, 2008



J. Kim, *et al.*, VLSI, 2011





	PMOS	NMOS
BTI Stress	Gate 0, Source VDD, Drain VDD	Gate VDD, Drain 0, Source 0
Recovery	Gate VDD, Source VDD, Drain 0	Gate 0, Drain VDD, Source 0

For both designs:

In stress: $V_{gs}=-V_{DD}$, $V_{ds}=0$

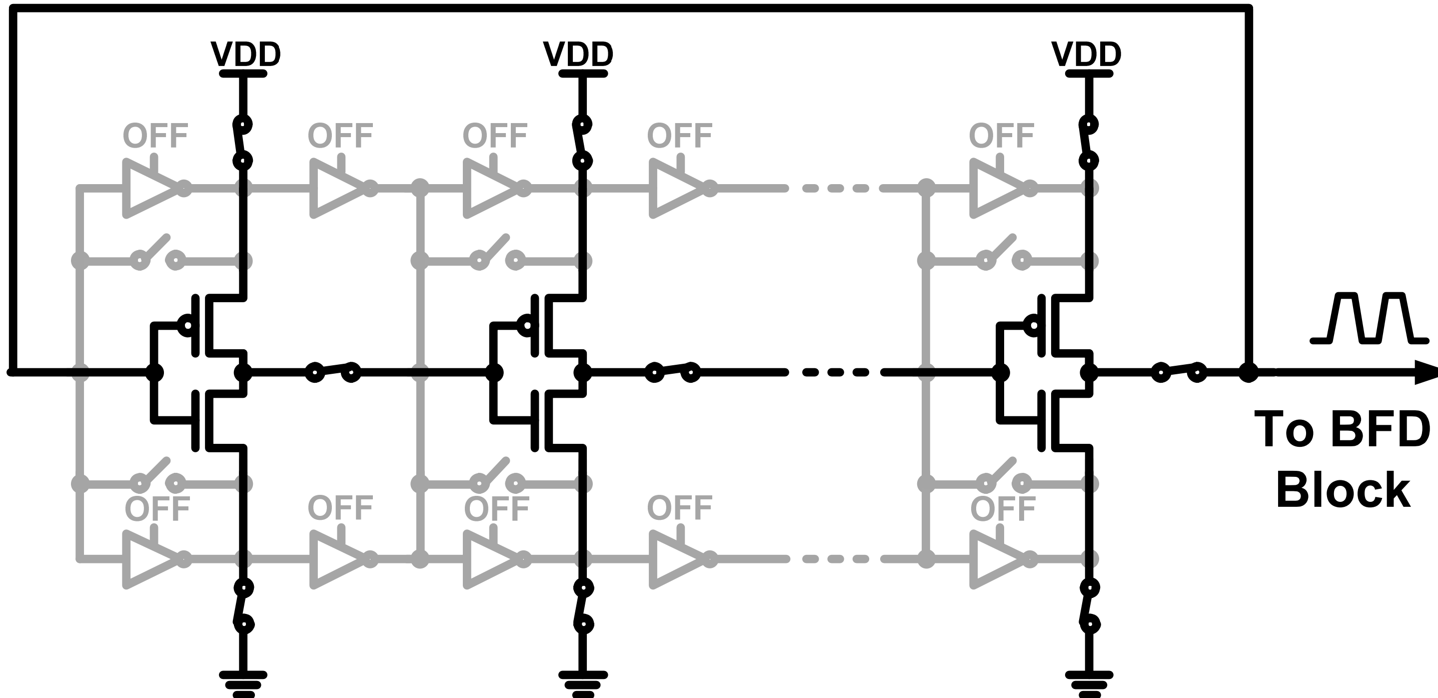
In recovery: $V_{gs}=0$, $V_{ds}=0$

- **During operation, most transistor recovery with $V_{ds}=V_{DD}$**
- **Easy to apply stress bias, but hard to turn the transistor off while keeping V_{ds} at V_{STR}**

Proposed Ring Oscillator in Stress Mode

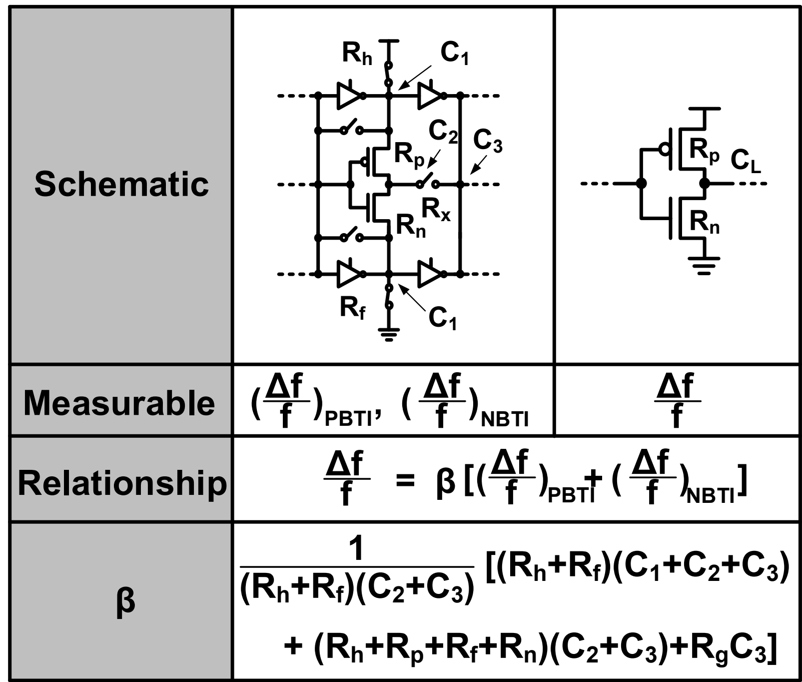
- Use pass gate and tri-state inverter to isolate stress
- During NBTI stress mode, NMOS source and gate are shorted
- Realistic AC stress (i.e. V_{ds}~V_{DD}) can be provided

Proposed Ring Oscillator in Meas. Mode

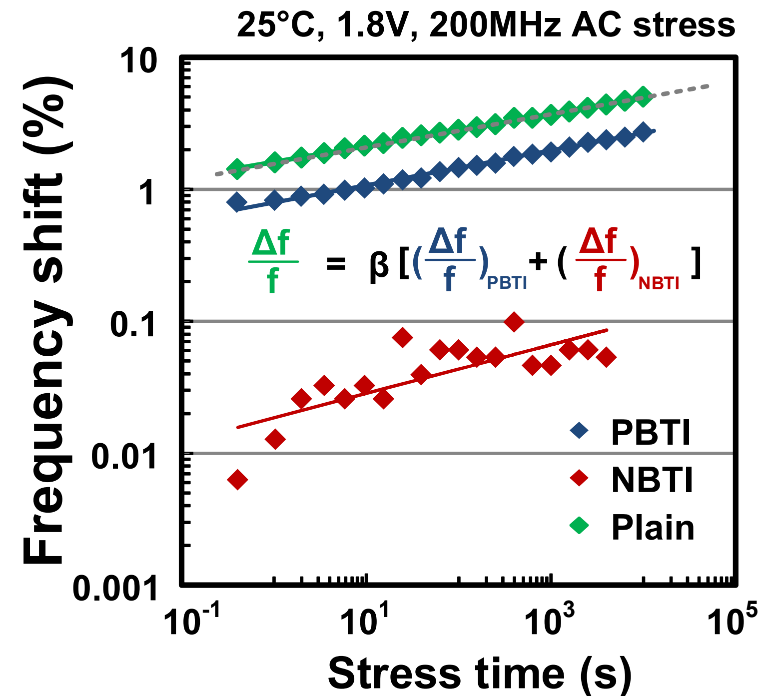


- Additional inverters and pass gates are all turned off, and the loop is closed to initiate the oscillation
- The impact of additional load of the auxiliary circuits on main path delay can be calibrated out

Calibration to Plain ROSC Degradation



Schematic	R_h, C_1, C_2, C_3, R_p, R_x, R_n, R_f, C_1	R_p, C_L, R_n
Measurable	$\left(\frac{\Delta f}{f}\right)_{PBTI}$, $\left(\frac{\Delta f}{f}\right)_{NBTI}$	$\frac{\Delta f}{f}$
Relationship	$\frac{\Delta f}{f} = \beta\left[\left(\frac{\Delta f}{f}\right)_{PBTI} + \left(\frac{\Delta f}{f}\right)_{NBTI}\right]$	
β	$\frac{1}{(R_h+R_f)(C_2+C_3)}\left[(R_h+R_f)(C_1+C_2+C_3) + (R_h+R_p+R_f+R_n)(C_2+C_3)+R_gC_3\right]$	



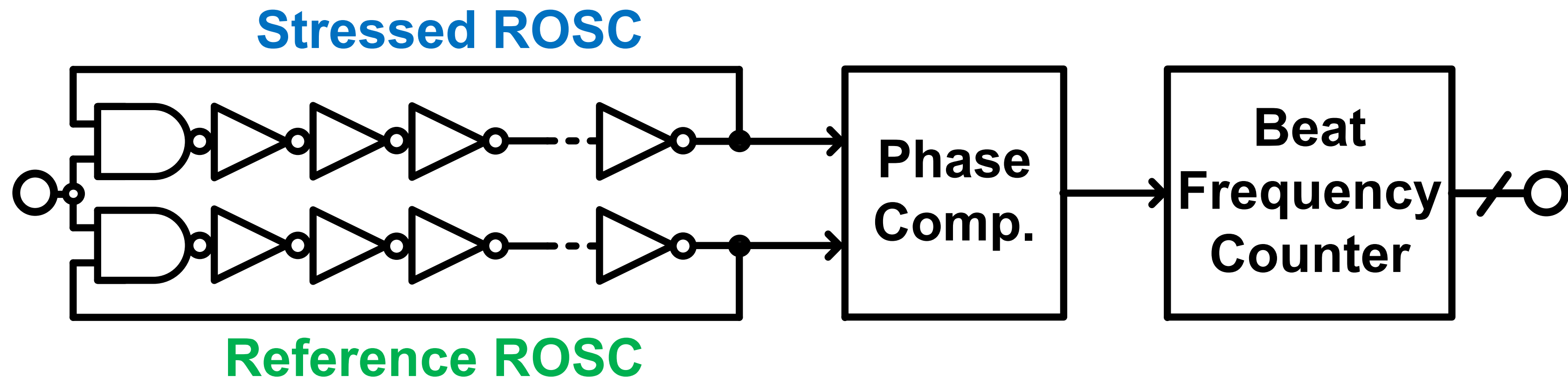
- The delay induced by the additional switches are not dependent on aging, proven by simulation
- Test results can be calibrated using one point calibration

Comparison on PBTI/NBTI Monitoring

	ICICDT 2008	VLSI 2011	This work
ROSC Stage Diagram (NBTI Stress Mode Shown)			
Stress Capability	DC No AC data	DC Unrealistic AC (i.e. V_{ds}=0)	DC Realistic AC (i.e. V_{ds}=~V_{STR})
Meas. Scheme	Simple counter	Simple counter	Beat frequency scheme with phase alignment
*Meas. Time for 0.01% Resolution	10,000 ROSC periods	10,000 ROSC periods	100 ROSC periods (<1μs)

- Neither of the previous designs can provide realistic recovery bias (i.e. V_{ds}=V_{DD})
- Simple counter based scheme results in unwanted recovery

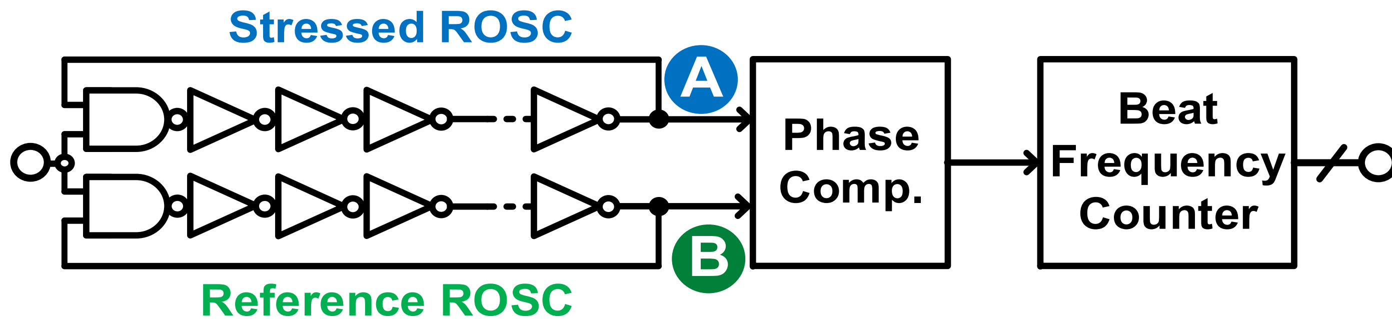
Silicon Odometer Beat Frequency Scheme

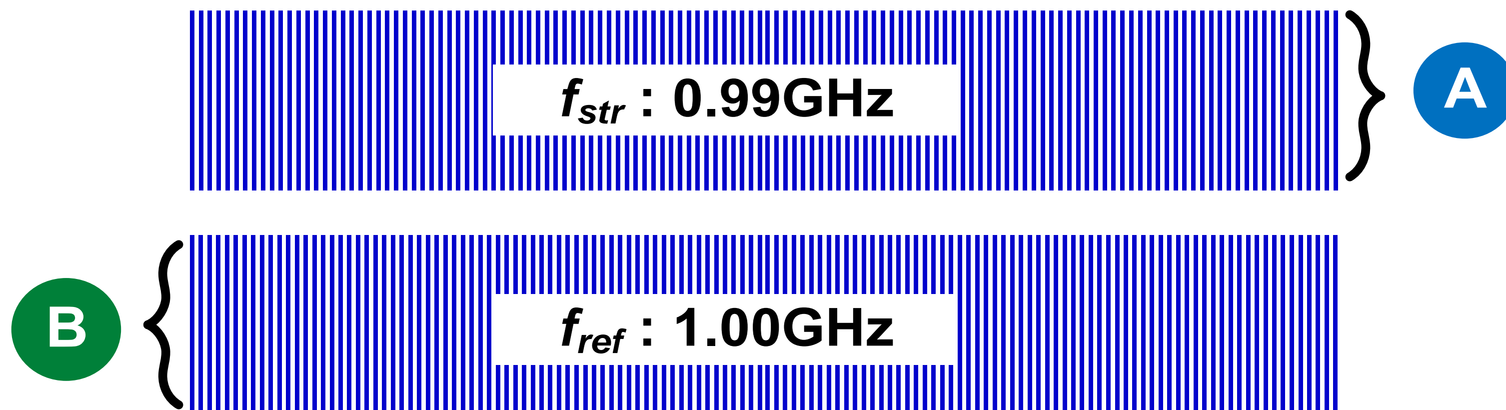


T. Kim, *et al.*, JSSC, 2008

- Beat frequency of two free running ROSCs measured by DFF and edge detector
- Benefits of beat frequency detection system
  - Achieve ps resolution with μs measurement interrupt
  - Insensitive to common mode noise such as temperature drifts
  - Fully digital, scan based interface, easy to implement

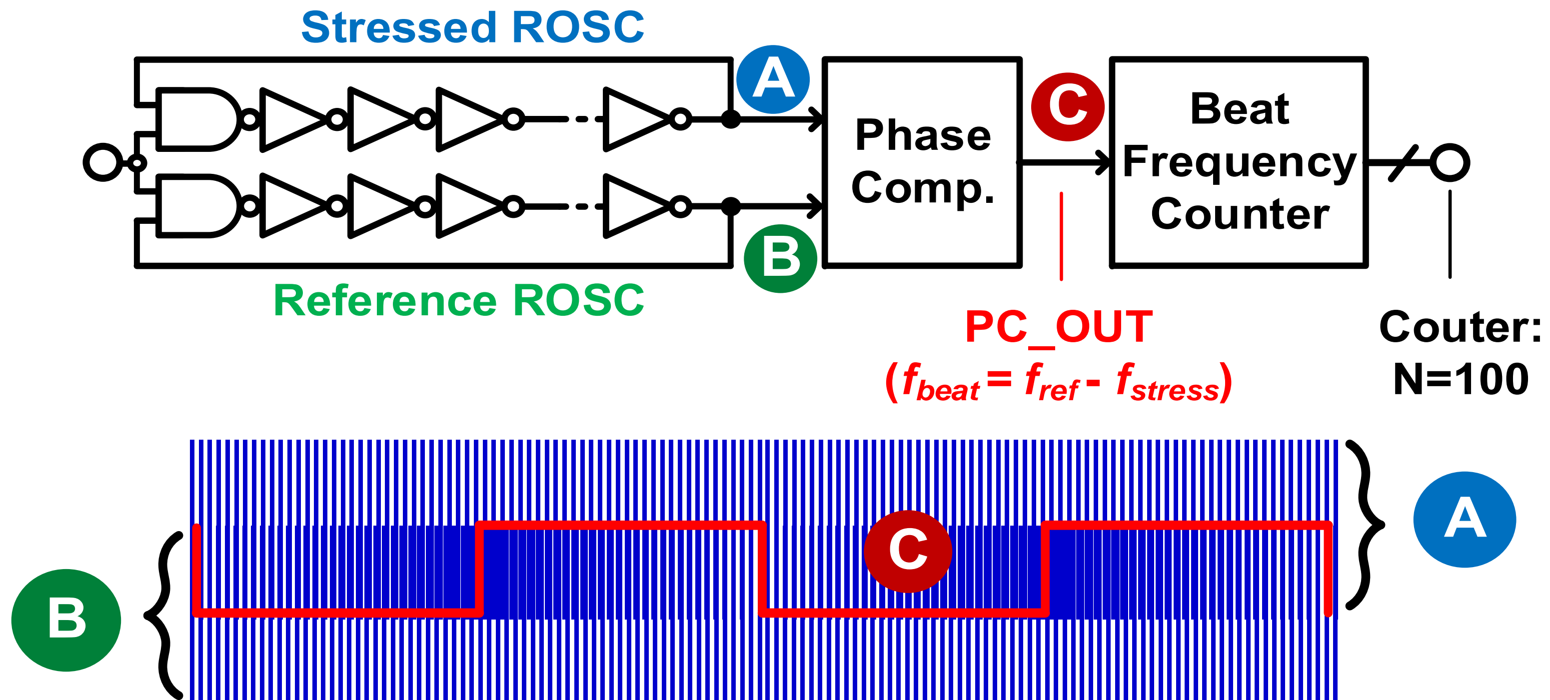
Use Beat Frequency to Detect Aging





- **Phase comparator is used to generate the beat frequency**
- **At time zero the stressed ROSC is trimmed to be slightly slower than the reference ROSC**

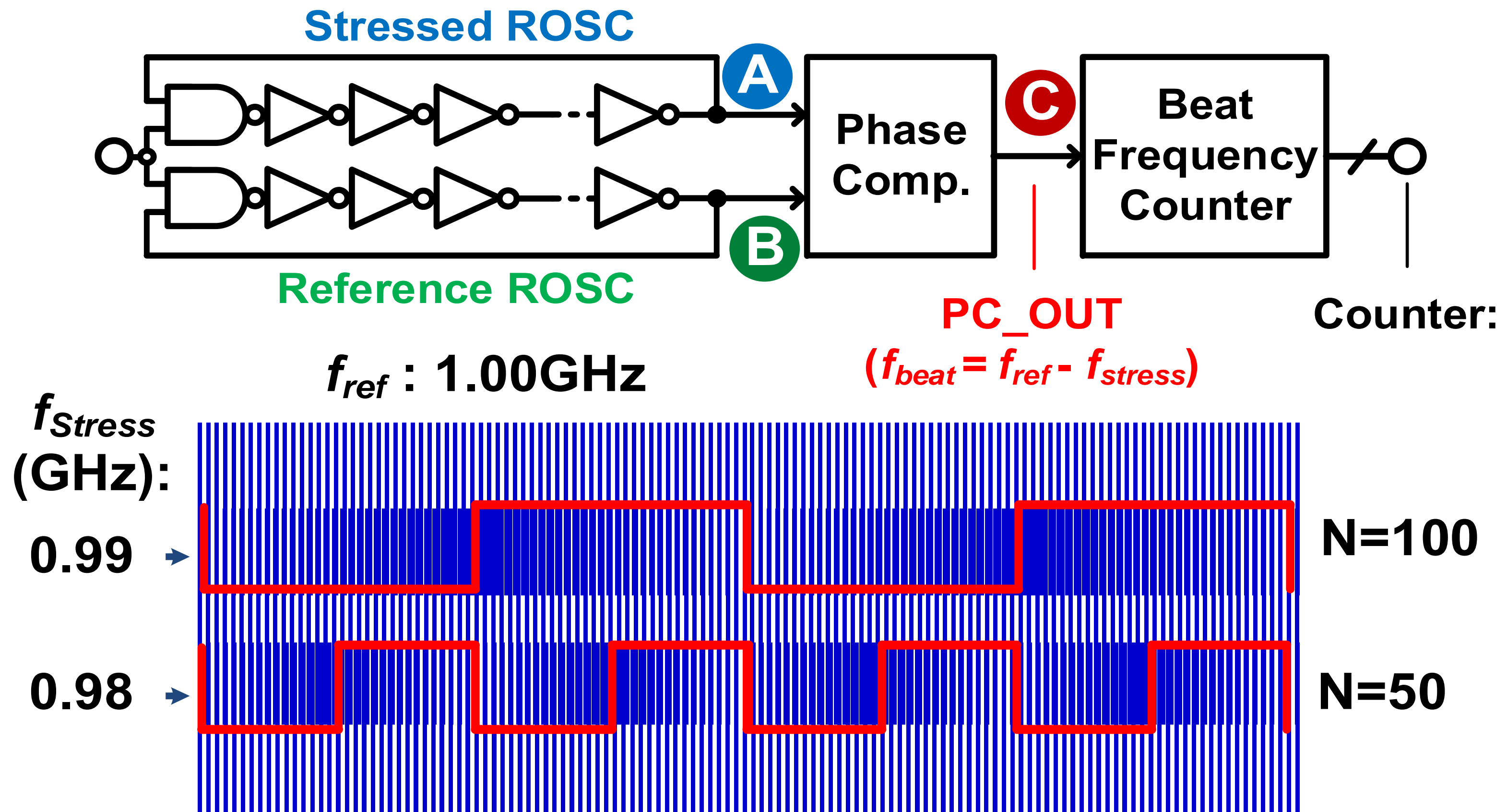
Use Beat Frequency to Detect Aging



- Phase comparator output: $f_{beat} = f_{ref} - f_{stress}$
- The counter counts the number of reference cycle in one period of the beat signal

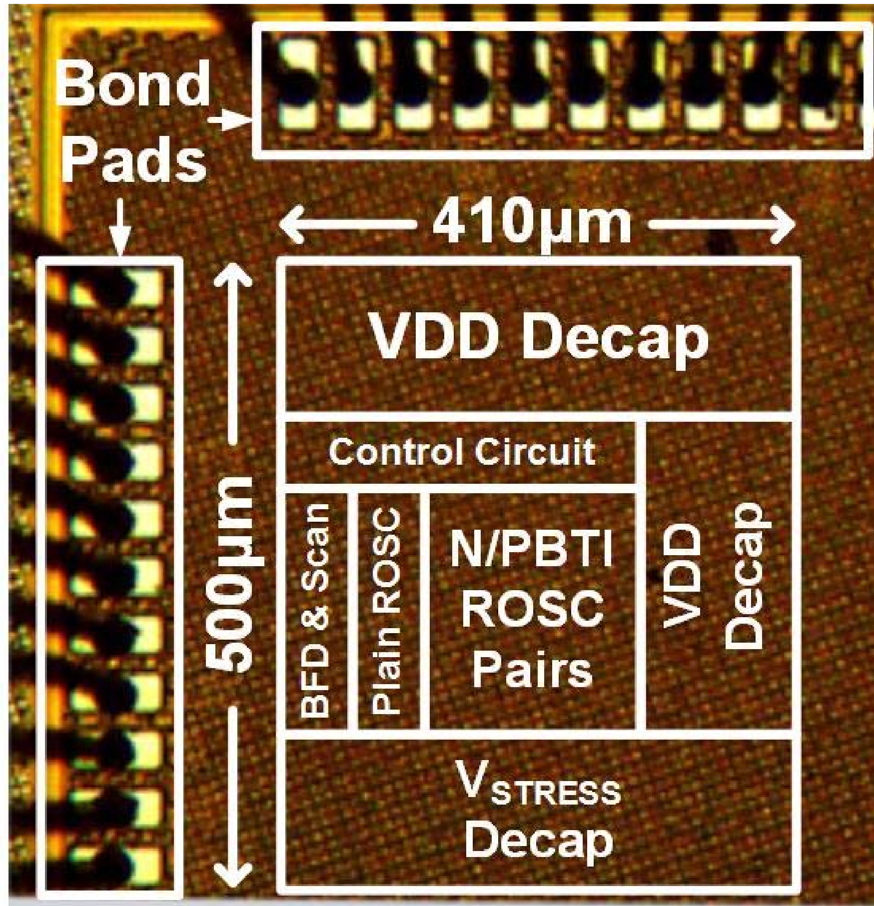
$$N = [(f_{str} - f_{ref})/f_{ref}]$$

Use Beat Frequency to Detect Aging



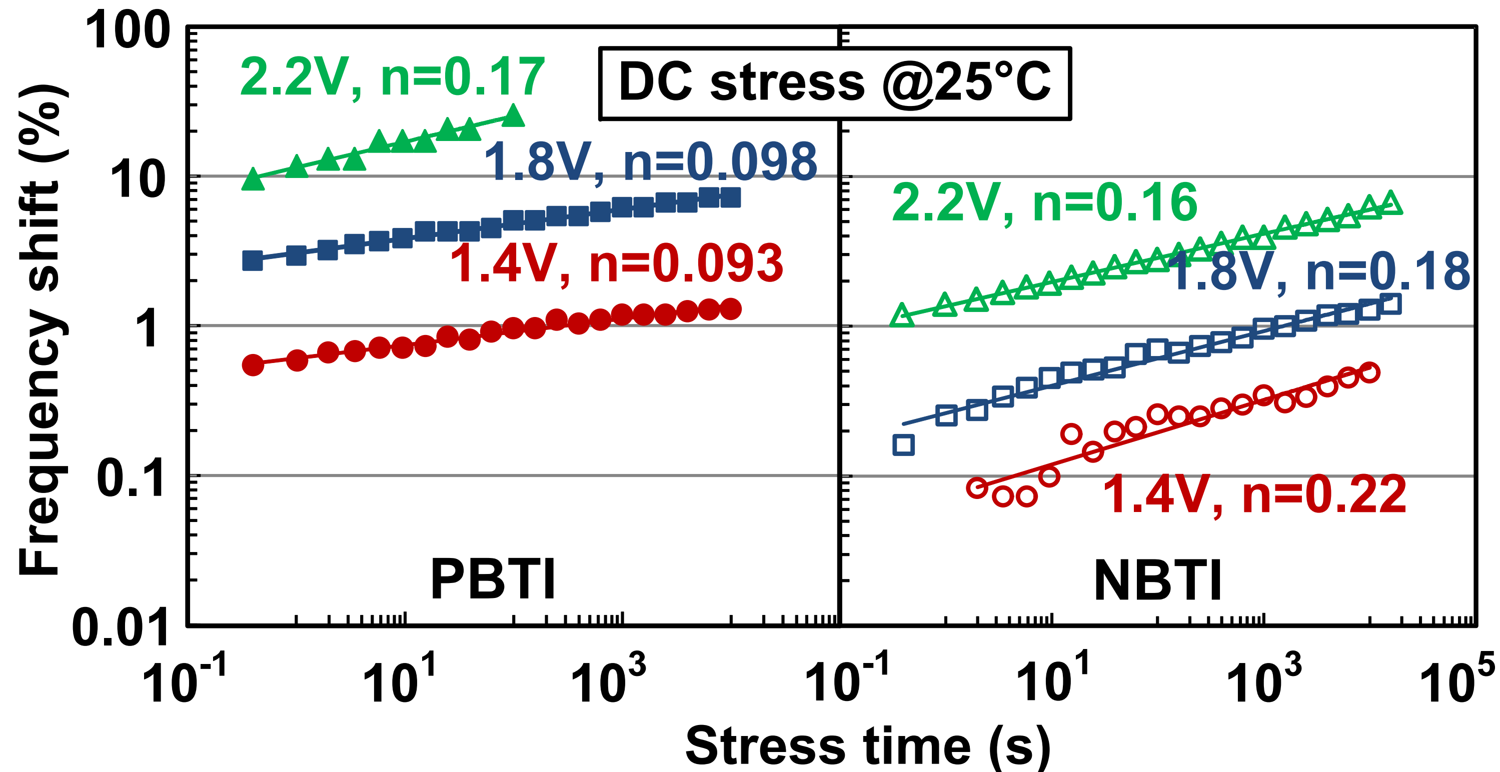
- 1% frequency difference before stress → N=100
- 2% frequency difference after stress → N=50
- Δf or ΔT sensing resolution is 0.01%

HKMG Test Chip Die Photo and Features



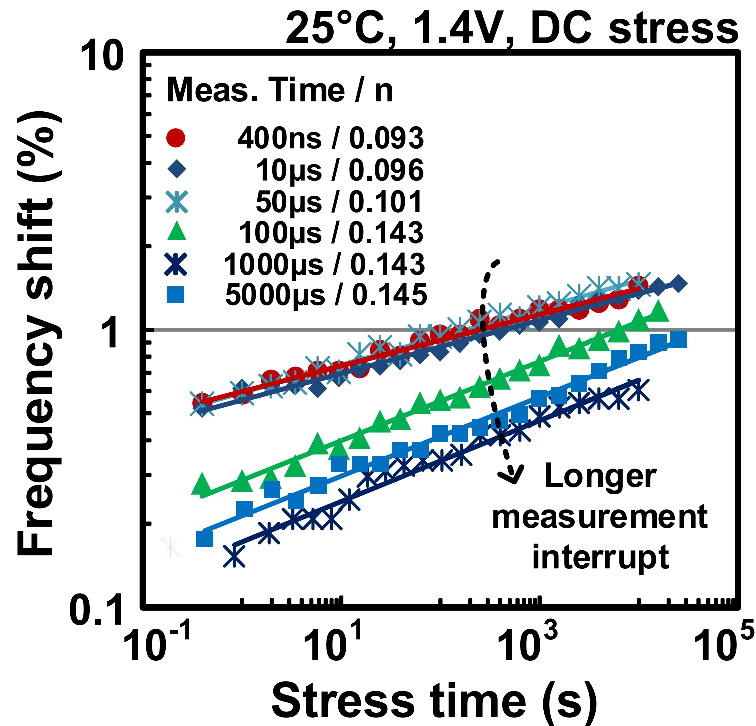
Process	HKMG CMOS
Core / IO Supplies	0.9V / 1.8V
Stress Voltage	0.9V, 1.4V, 1.8V, 2.2V
Measuremt Voltage	0.9V
Area	$500x410\mu m^2$
Δf Resolution	>0.01%
Measuremt Time	>400ns
DUT Type	Core Devices

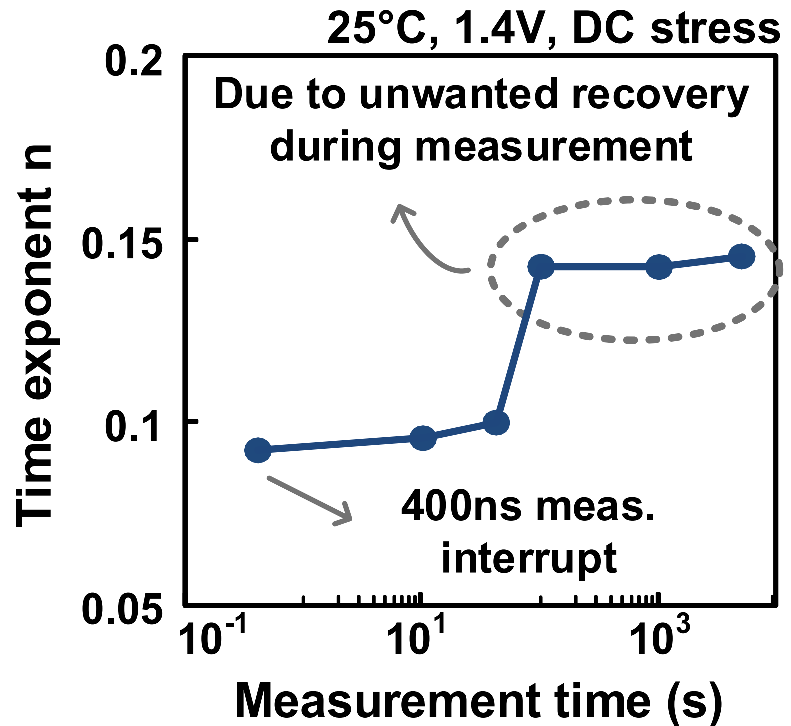
DC Stress Results for PBTI and NBTI



- Both NBTI and PBTI induced frequency shift show power law dependence with stress time
- Magnitude of PBTI is 5X to 10X larger than that of NBTI
- Time exponent n is lower than reported value

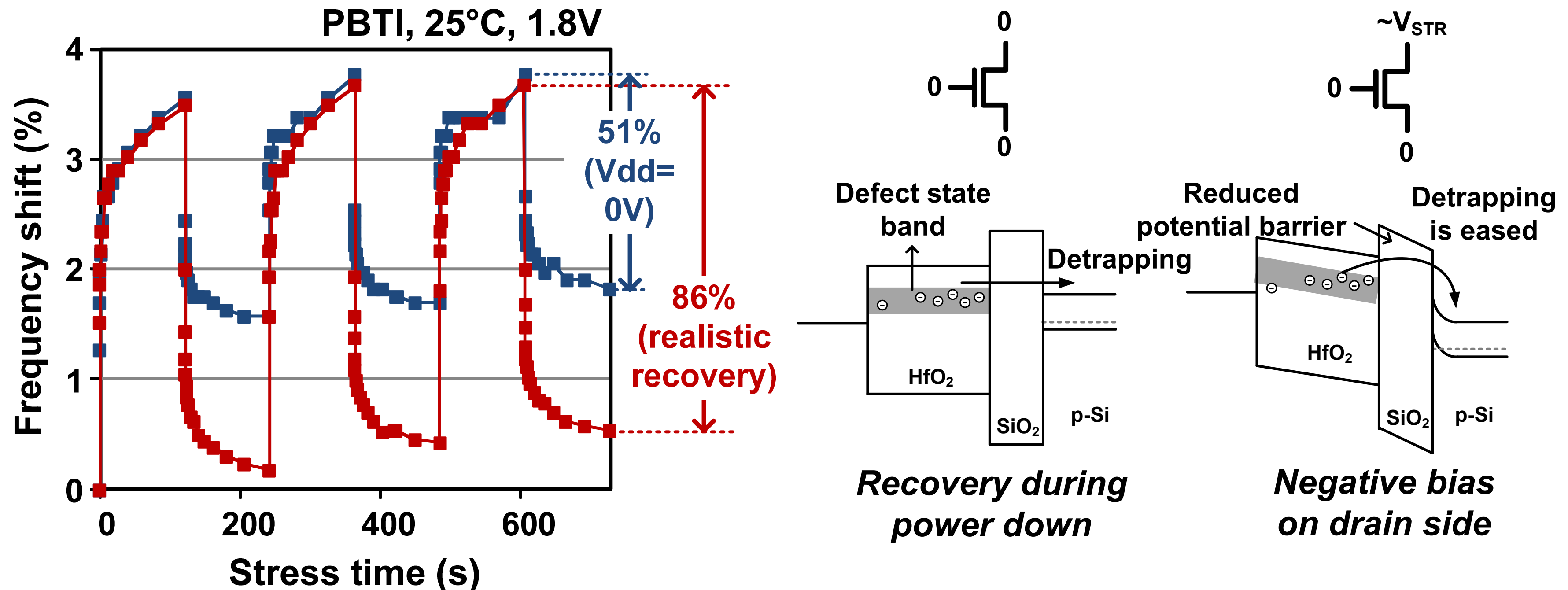
Impact of Measurement Interruption Time





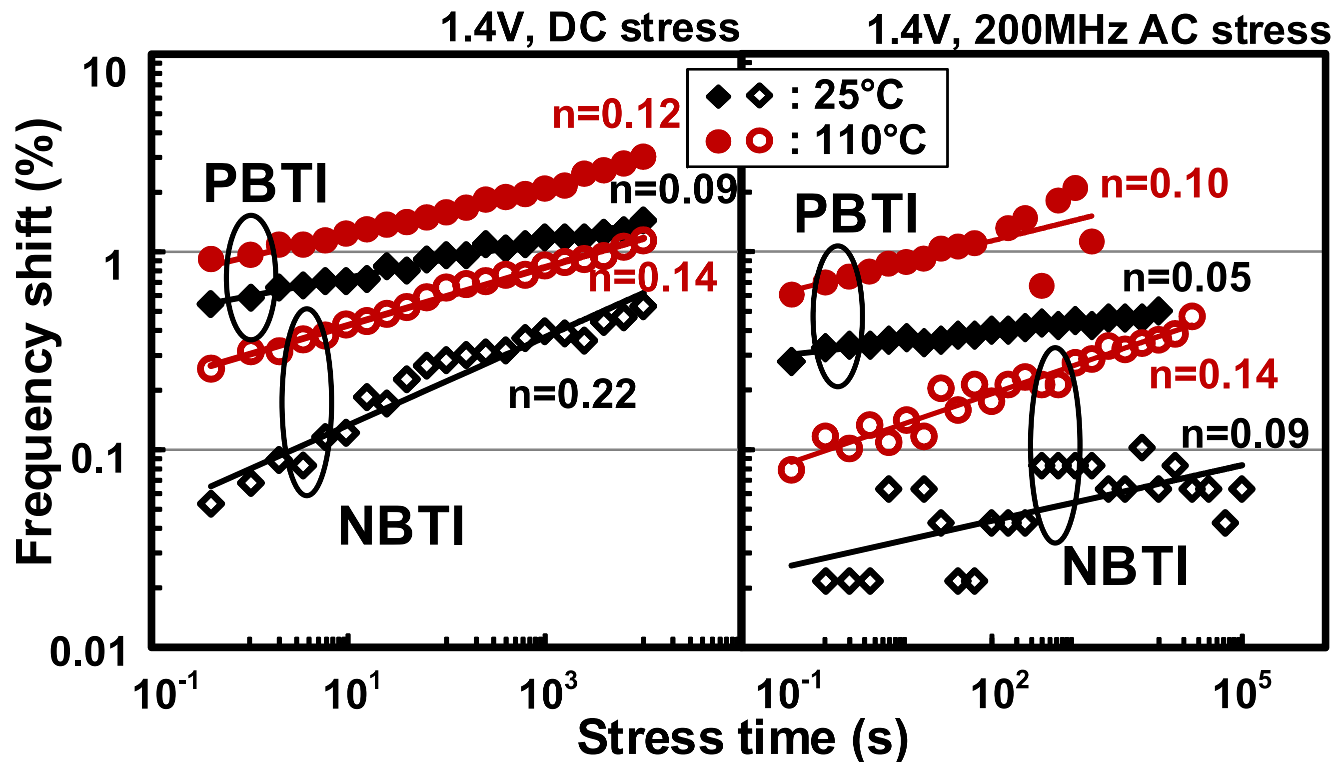
- Degradation decreases with longer measurement time
- Time exponent n increases with longer measurement interruption due to the recovery effect during measurement

Impact of Realistic Recovery Bias



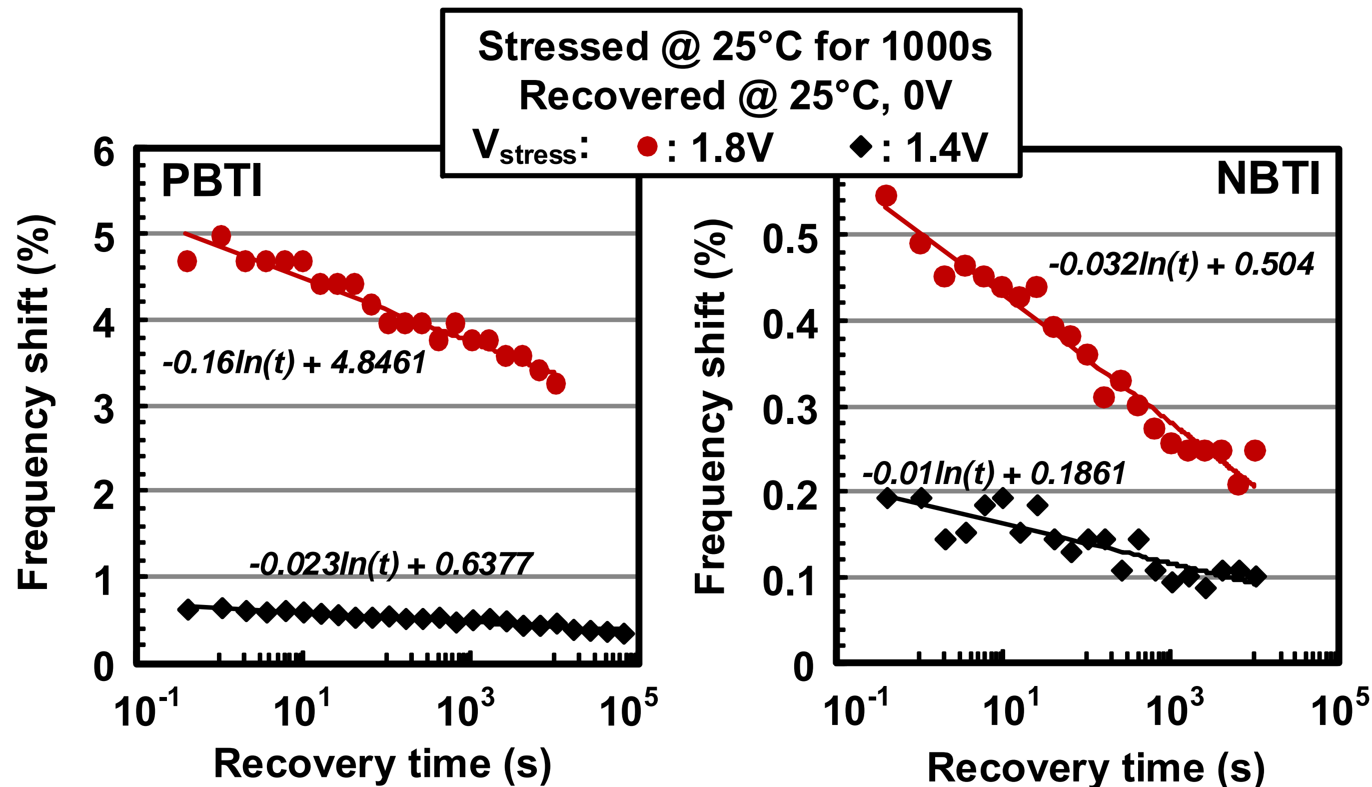
- V_{ds} bias gives stronger recovery rate when the transistor is off compared to zero V_{ds}
- The de-trapping process is accelerated due to the reduced potential barrier

DC and AC Stress at 25°C and 110°C



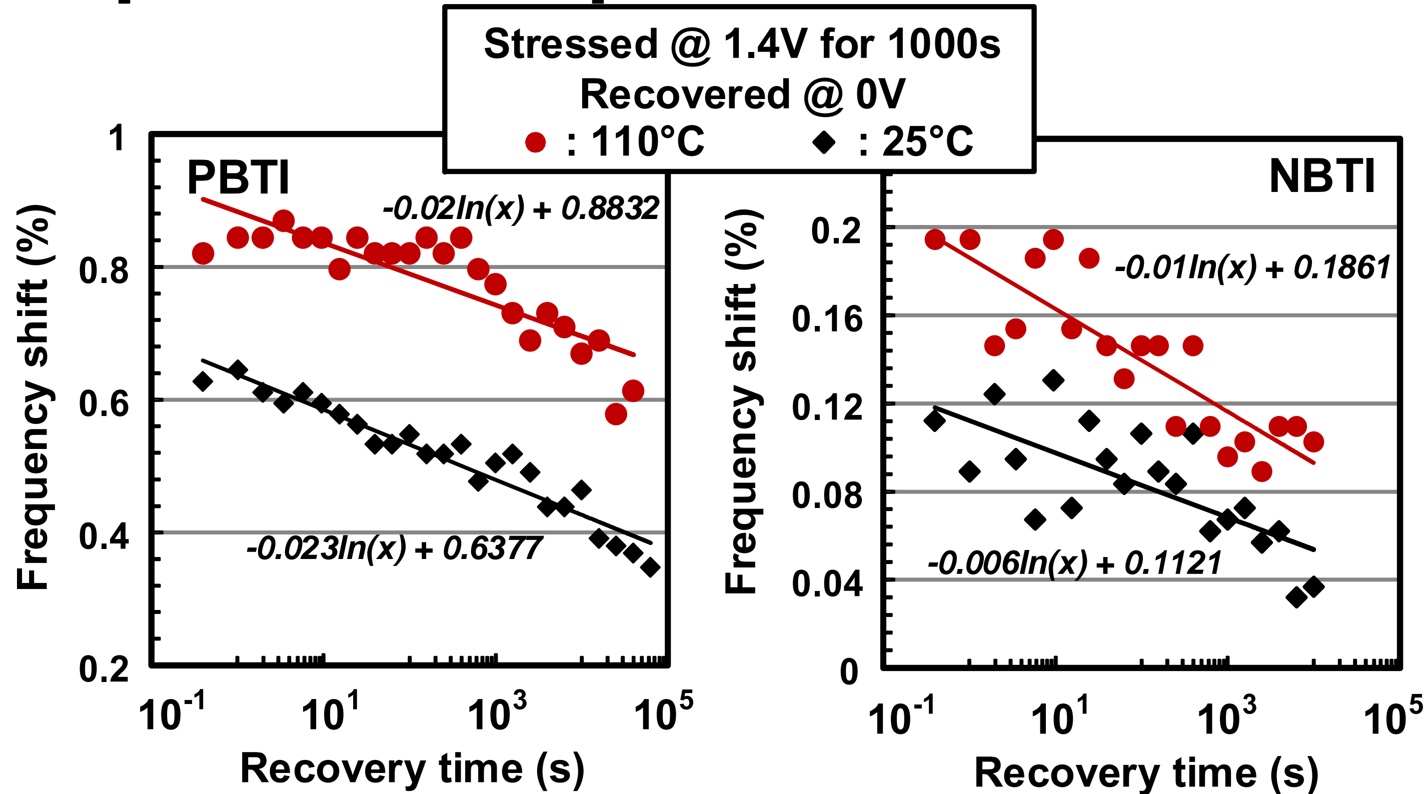
- NBTI is more sensitive to the temperature compared to PBTI
- The time slope dependence is more significant for AC stress

Long-Term Recovery Results versus Stress Voltage



- **Both PBTI and NBTI recovery follows a -log(t) dependency**
- **The magnitude and the log slope increases with stress voltage before recovery**

Temperature Dependence of Recovery



- Recovery magnitude and time slope show small difference at high temp. versus low temp.
- Both PBTI and NBTI recovery shows a weak dependence on temperature

Summary

- A ring oscillator based circuit separately monitor PBTI and NBTI impact on frequency
  - >0.01% resolution with measurement time down to >400ns
  - Supports realistic recovery bias condition
- Realistic power law time exponent measured using fast measurements
- Experimental data confirms that realistic recovery bias (i.e. V_{ds}~V_{DD}) indeed accelerates recovery compared to power down situation (i.e. V_{ds}=0V)