Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout

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Logic Technology Development

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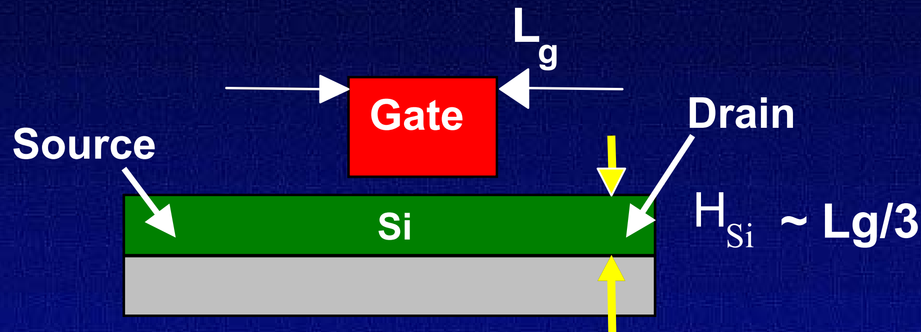
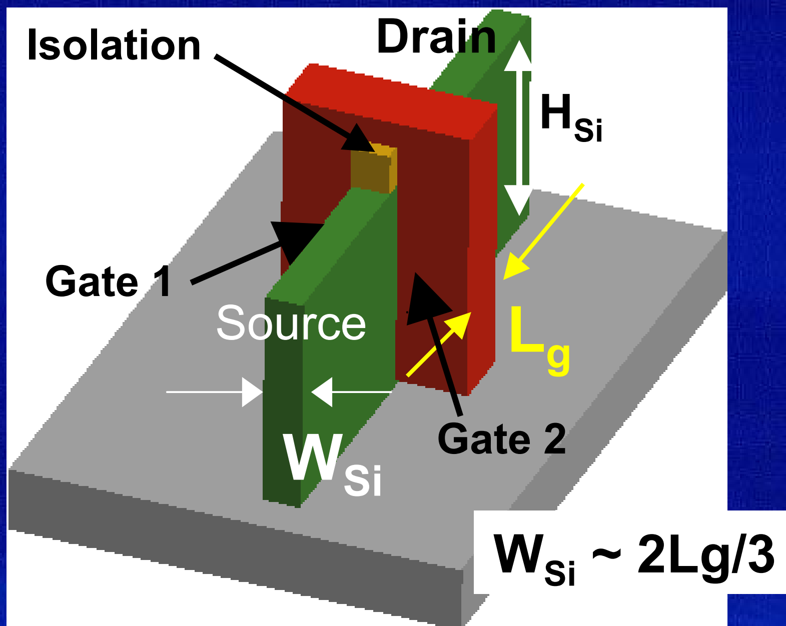
Outline of Presentation

- Introduction
  - Different Depleted Substrate Transistor (DST) Architectures
- Experimental Results
- Computer Simulation Results
  - Dimensional Analysis
  - Importance of Corner Effects
- Tri-Gate Layout Analysis
- Summary

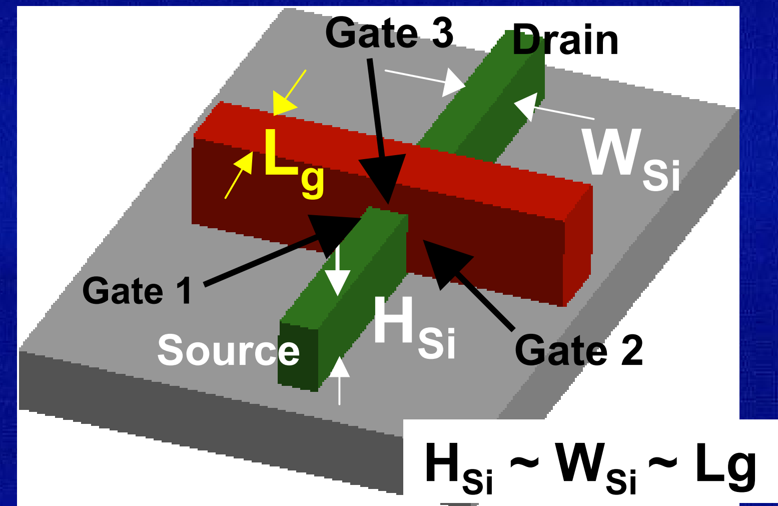
Transistor Architectures



Single-Gate Planar

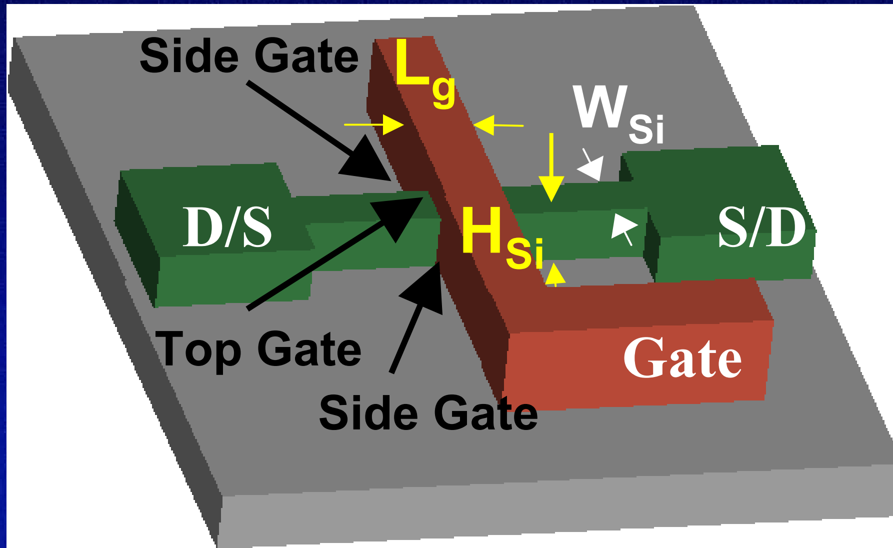


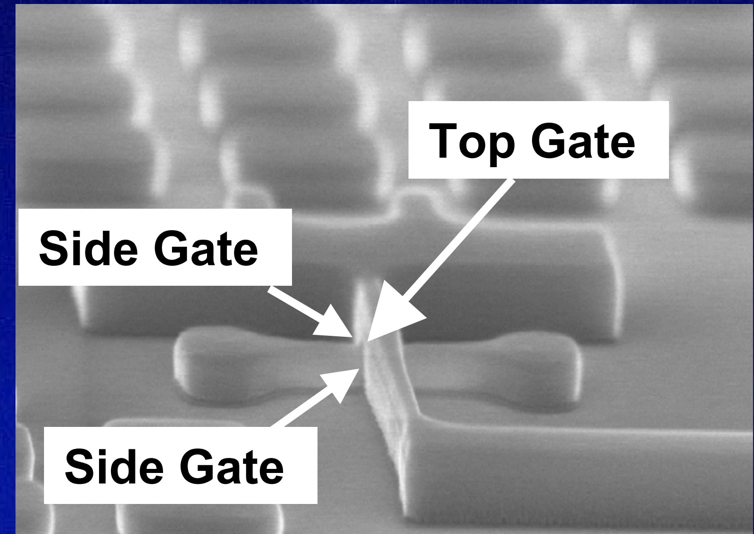
Double-gate (e.g. FINFET) Non-Planar



Tri-gate Non-Planar

Tri-gate Transistor

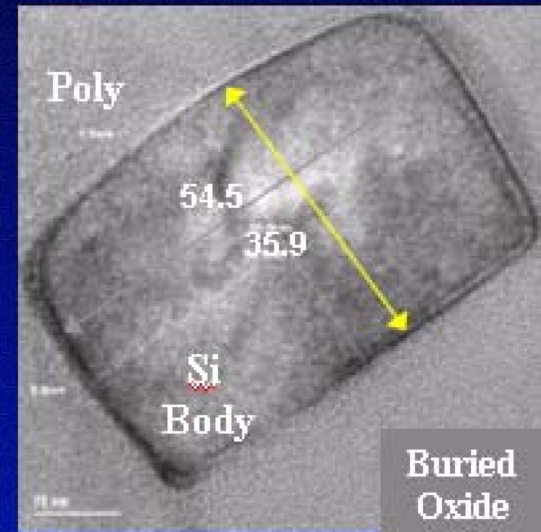


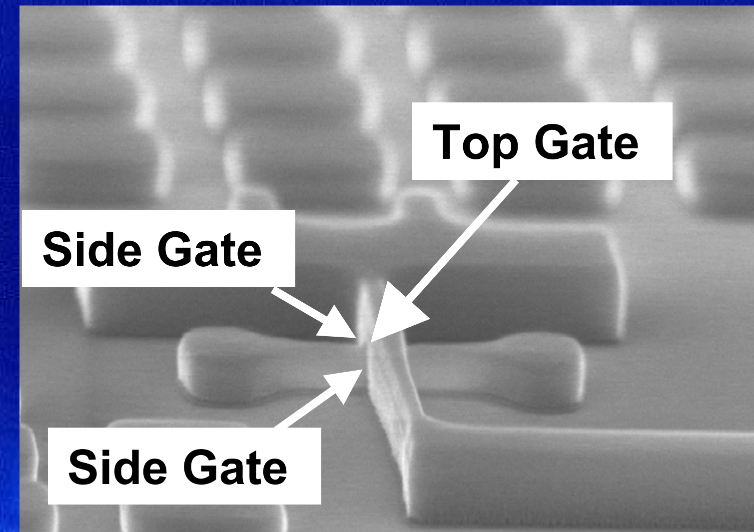


Body controlled on three sides by adjacent gates
-> Excellent electrostatic control of body

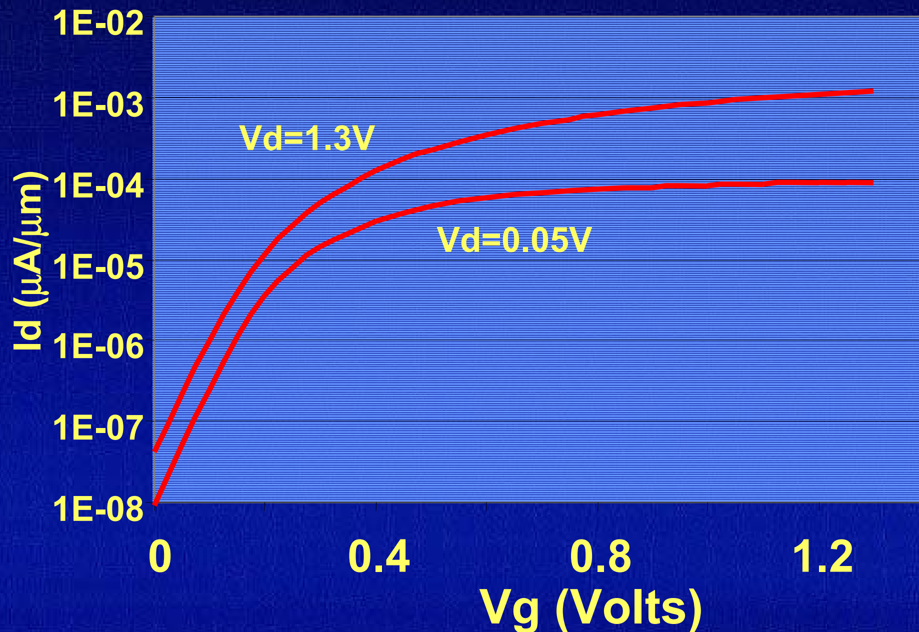
Experimental Tri-Gate Process

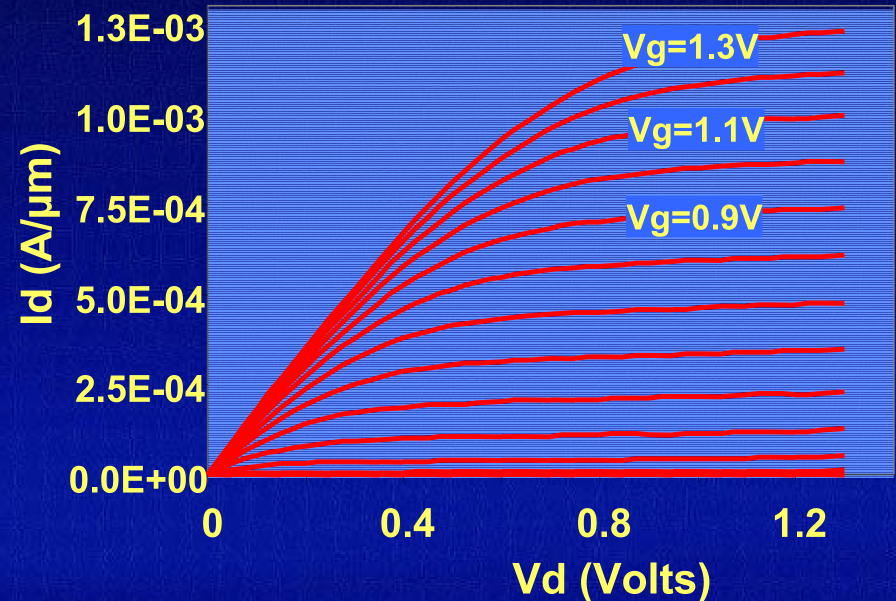
- Starting Si thickness = 50nm
- BOX thickness ~ 200nm
- Well implants
- N_2O sacrificial oxidation
- Physical Tox = 1.5nm
- Poly thickness = 100nm
- Raised source-drain
- Nickel salicide





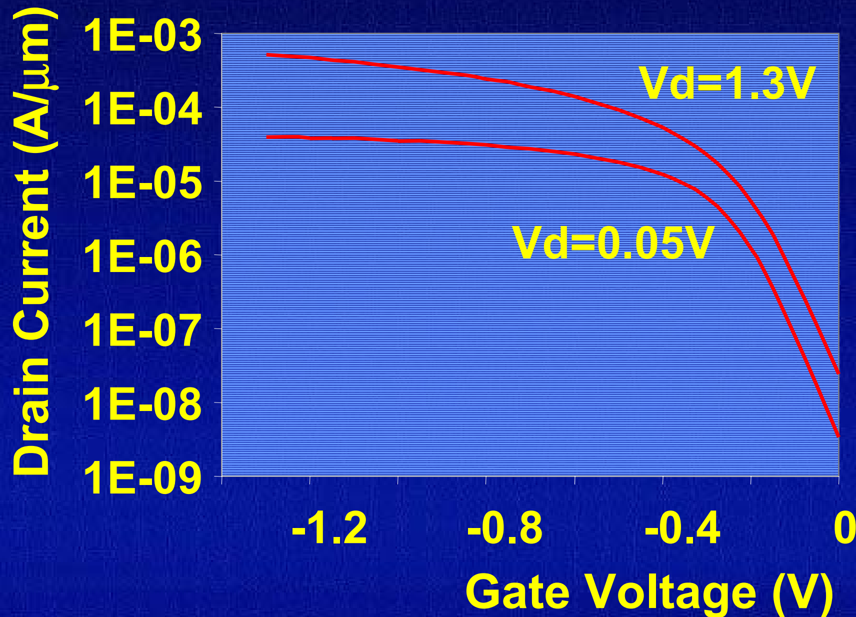
60nm NMOS Tri-Gate Transistors

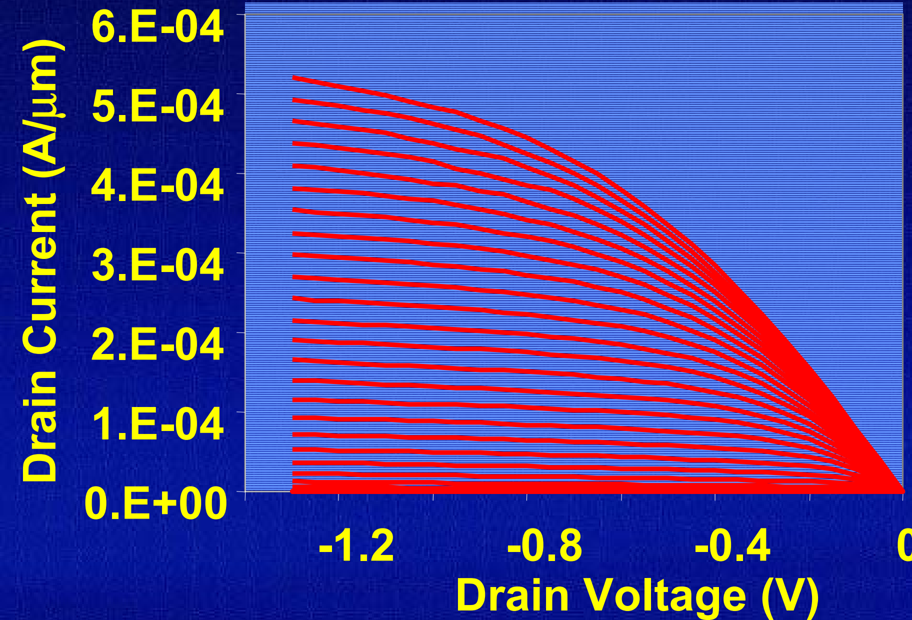




- Idsat = 1.23mA/μm and Ioff = 40nA/um at Vcc = 1.3V
- Subthreshold slope = 72mV/decade
- DIBL (Drain Induced Barrier Lowering) = 35mV/V

60nm pMOS Tri-Gate Transistors





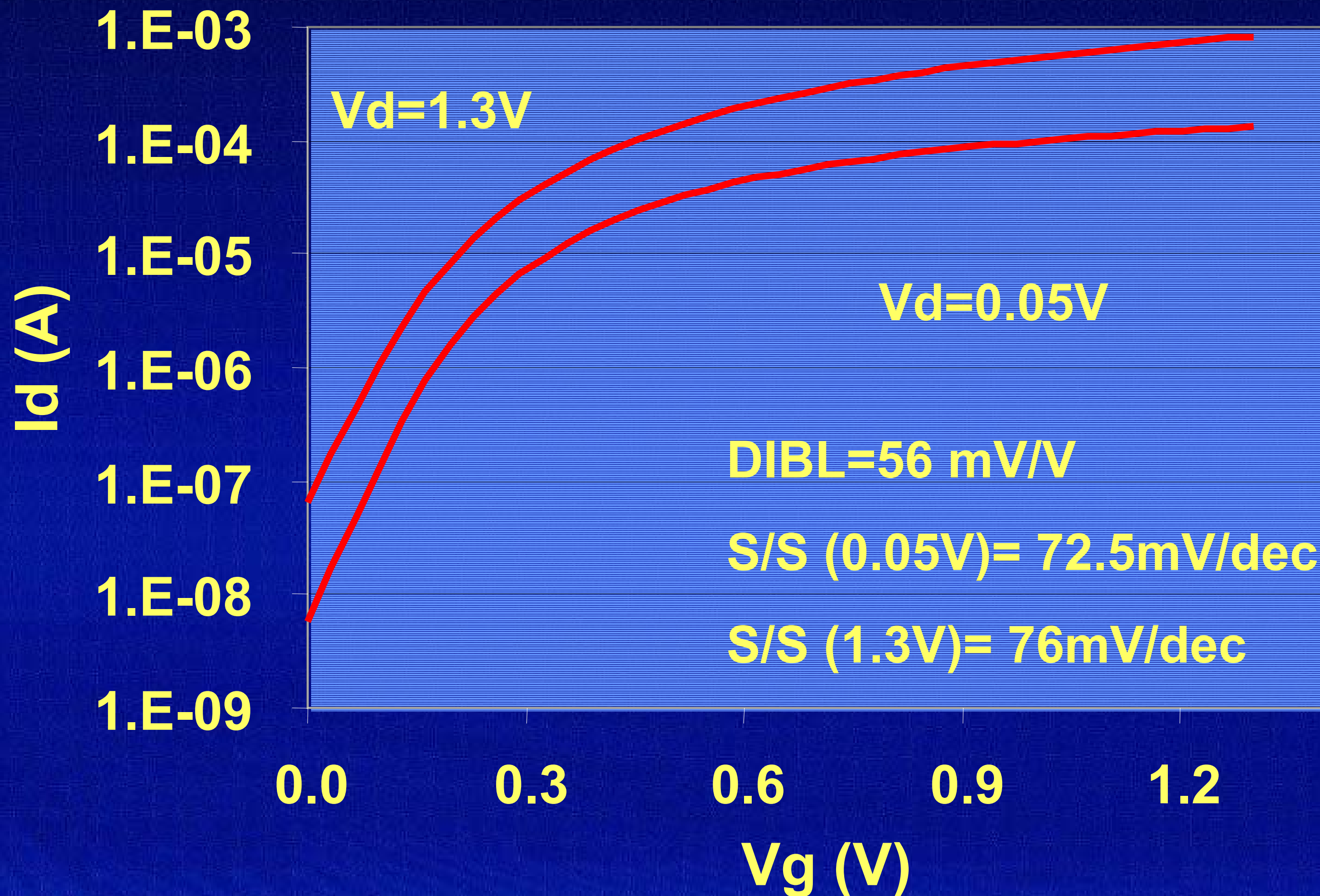
- Idsat = 520 μA/um and Ioff = 24nA/um at Vcc = 1.3V
- Subthreshold slope = 69.5mV/decade
- DIBL (Drain Induced Barrier Lowering) = 48mV/V

Double Gate-like

Understanding Tri-Gate Behavior

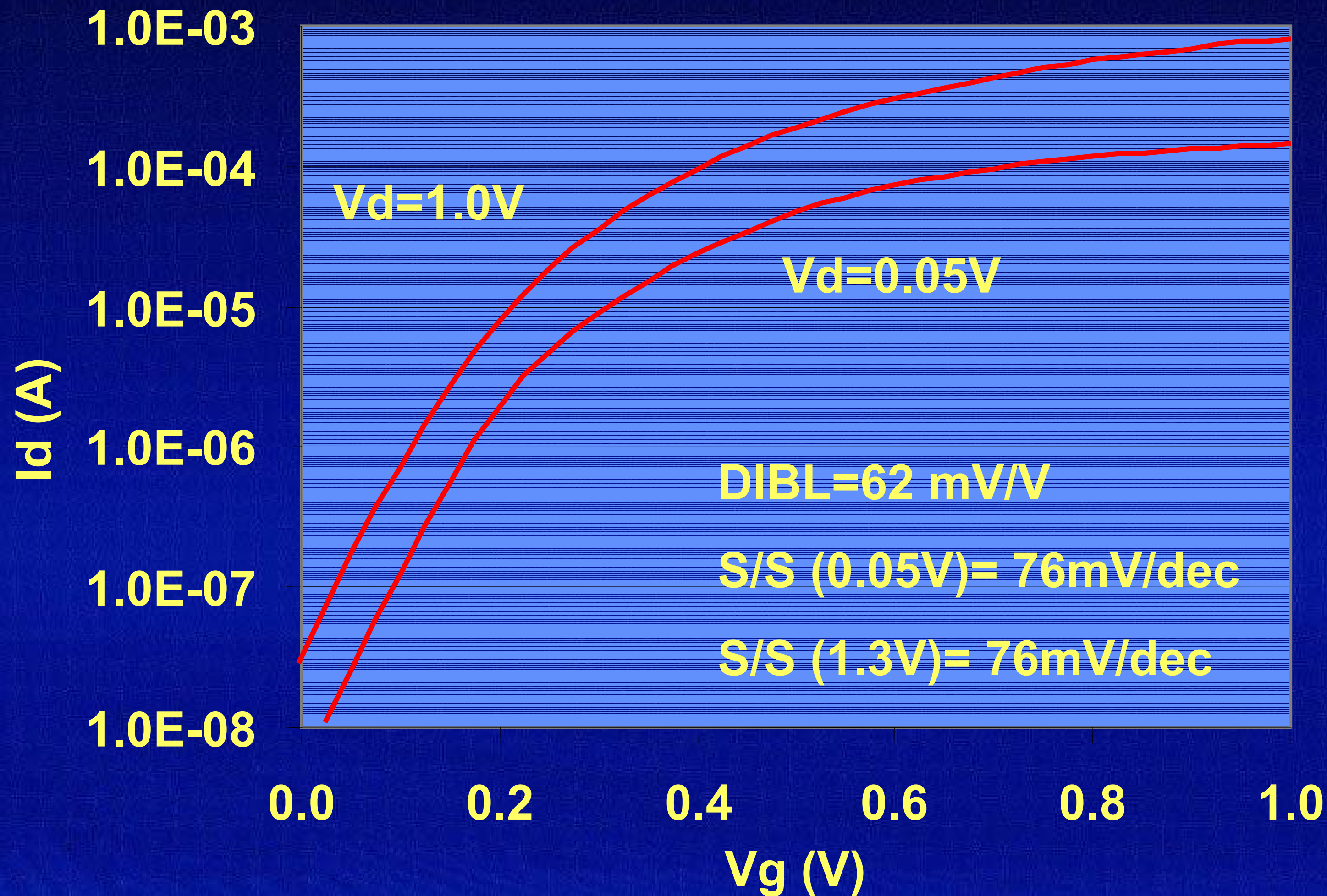
- Device simulator
  - Full 3D single-carrier solution using DESSIS device simulator
  - Hansch quantum correction model applied
  - Intel 2.2 Ghz Xeon processor takes about 1 minute/bias point for an 18000 node mesh
- Simulated structures
  - L_g=60 nm / H_{Si}=60 nm / W_{Si}=60 nm
  - L_g=30 nm / H_{Si}=30 nm / W_{Si}=30 nm
  - Electrical Tox varies from 22 to 34 A
- - Corner radius varied from 0 (right-angle) to 16 nm
  - Adjusted doping adjusted to get I_{off} ~100 nA/μm

Simulation of L_g=H_{Si}=W_{Si}=60nm



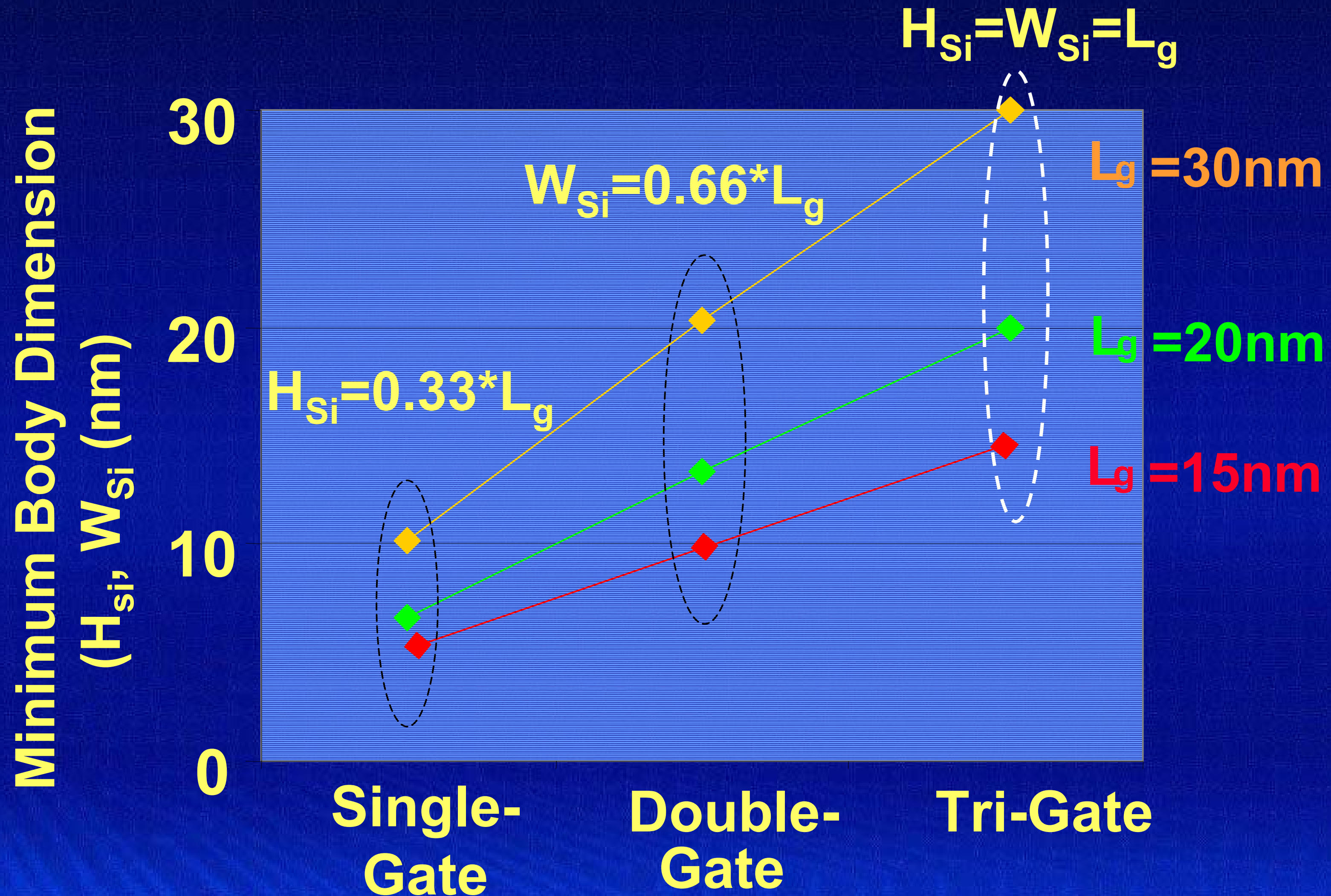
Tri-Gate device shows full depletion effects

Simulation of $L_g=H_{Si}=W_{Si}=30nm$



$L_g = W_{Si} = W_{Si}$ = 30nm device shows excellent electrostatics

Body Scaling Vs DST Architecture



Tri-Gate body size more relaxed than single-gate or Double-Gate

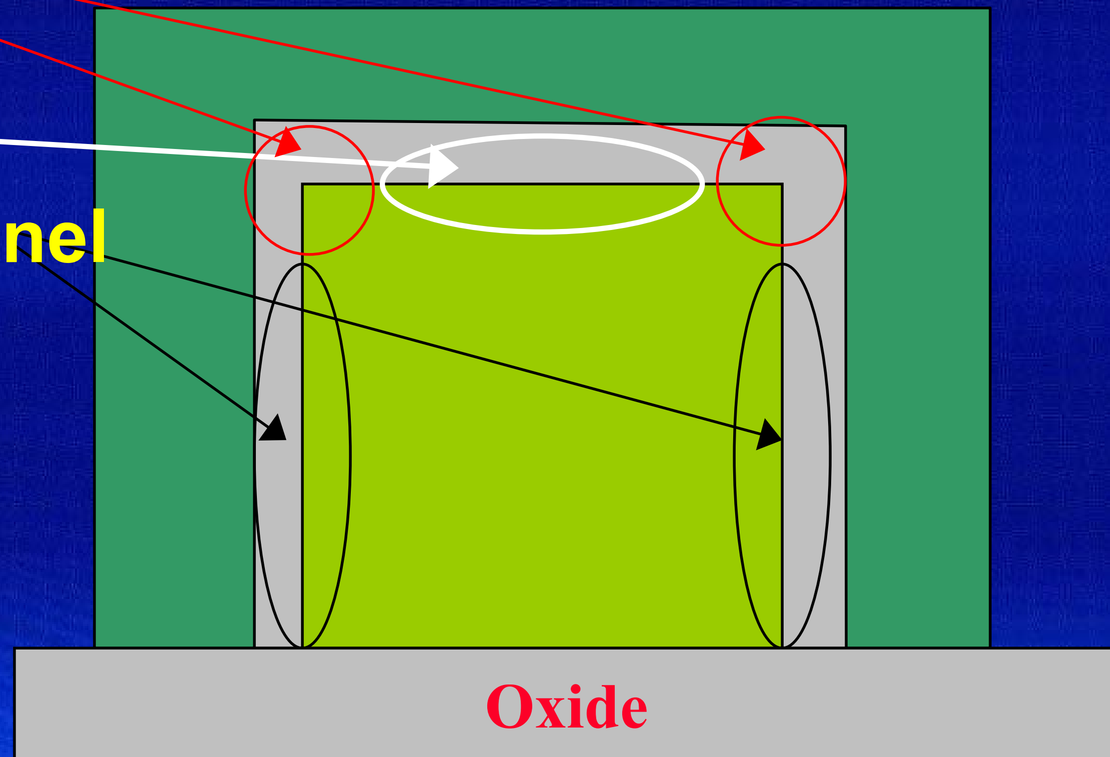
Tri-Gate Device Understanding

- TCAD simulations partitioned into 3 distinct regions:

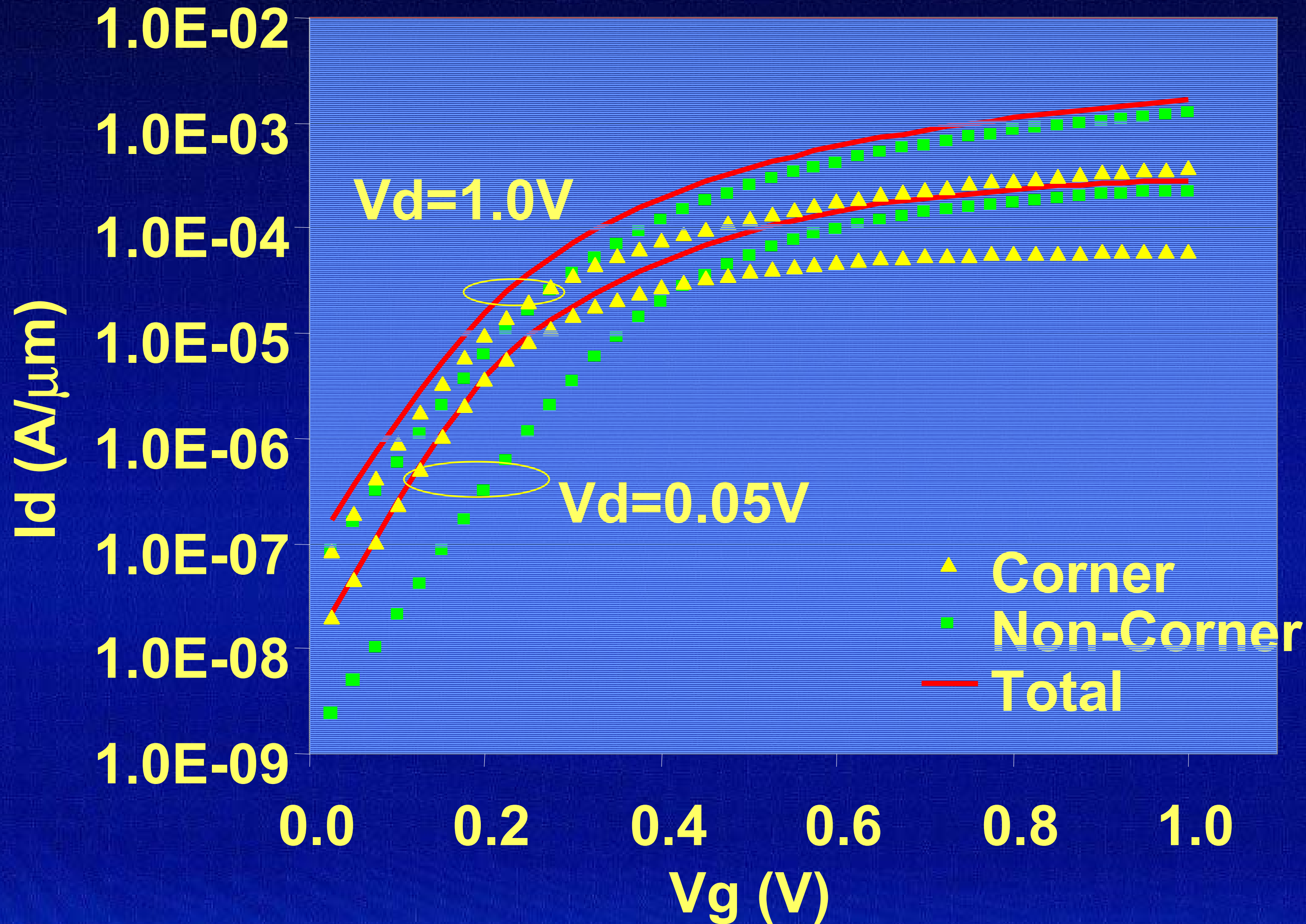
Corners

Top channel

Sidewall channel

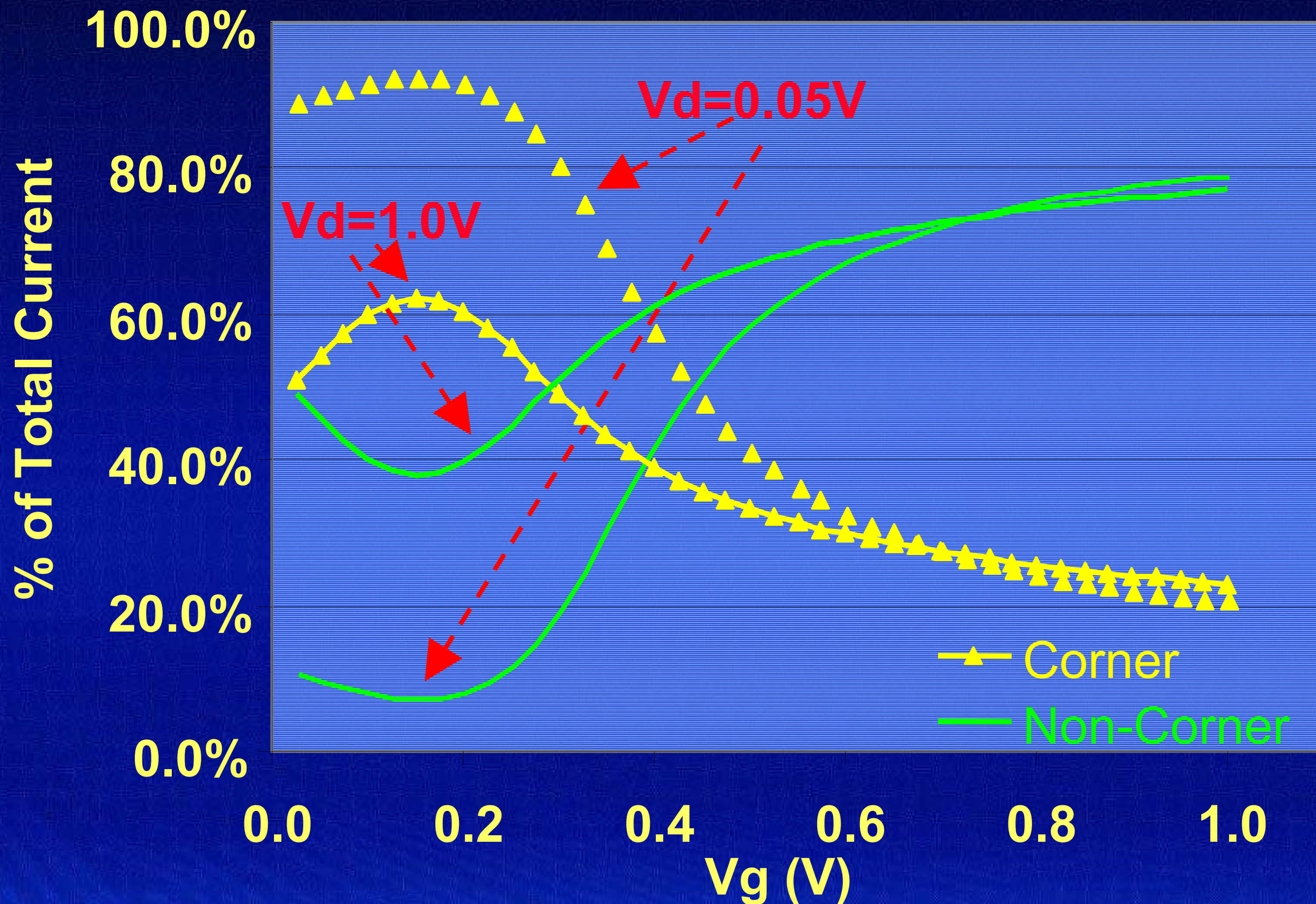


Components of Current



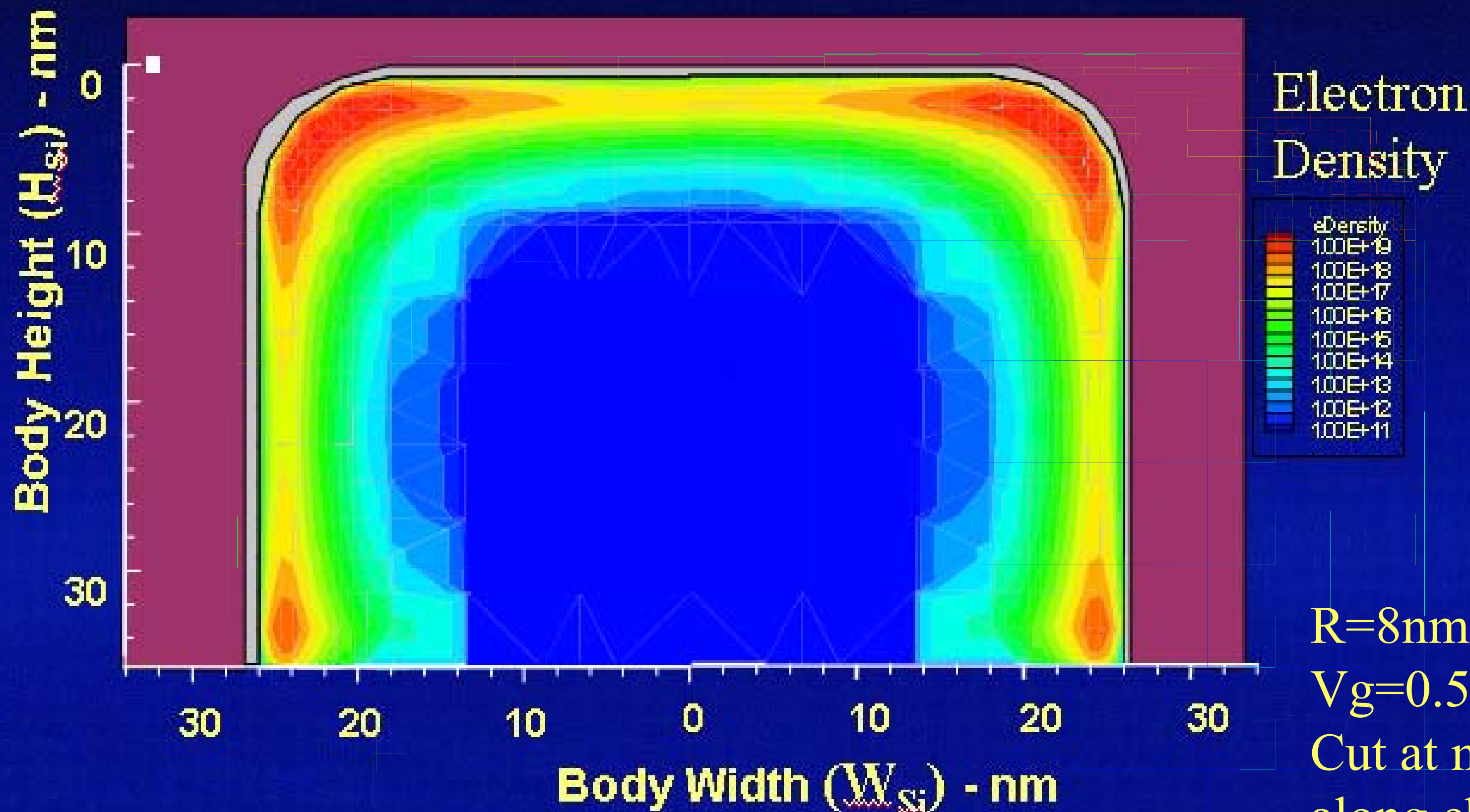
Corner device shows much improved S/S & DIBL over non-corner devices because of proximity of adjacent gates

Components of Current



- Corner device dominates at low Vg's
- Non-Corner device (top & side) dominates at high Vg's

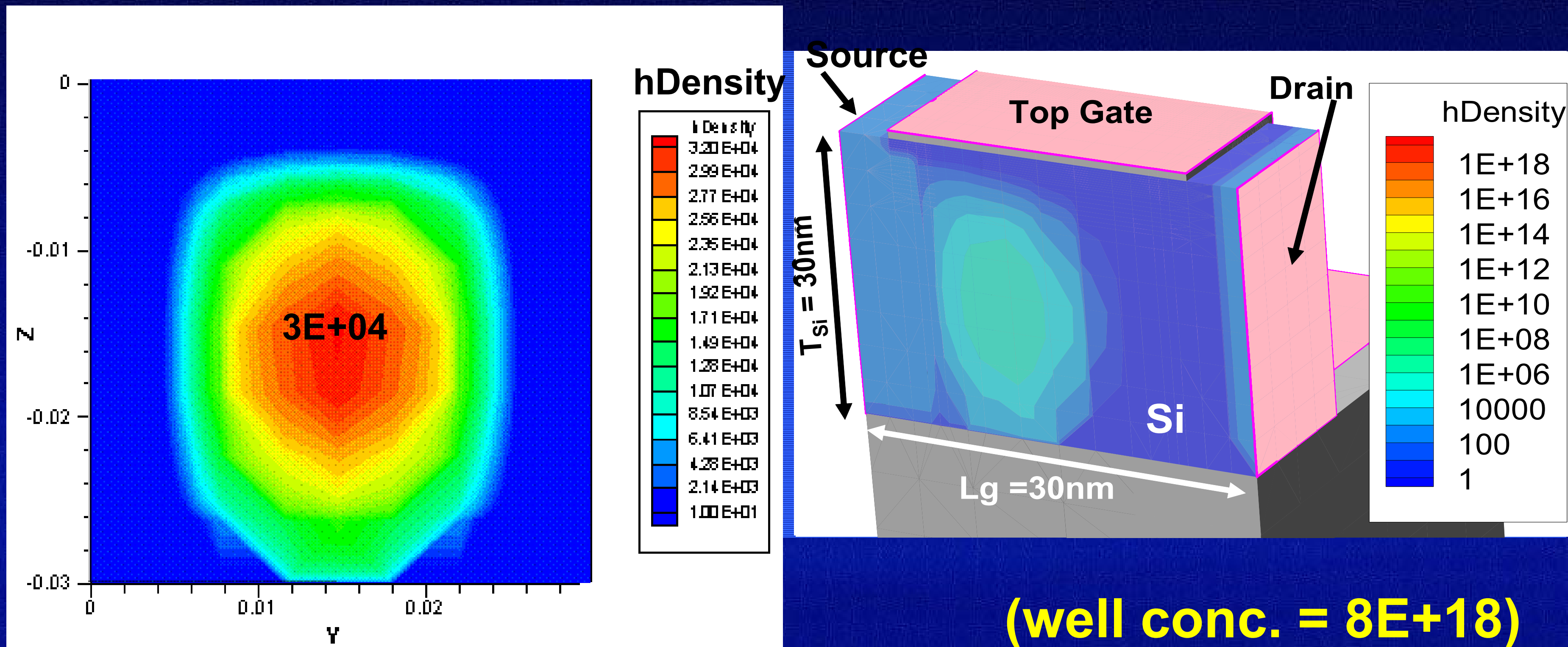
Physics of Corner Device



R=8nm
Vg=0.5V, Vd=1.0V
Cut at midpoint along channel

Proximity of the two gates at the corner give the nearly-ideal characteristics of the corner device, and the high current density

Physics of Tri-Gate Device



- All 3 gates control the depletion regions in the Tri-Gate device to make the Si body fully depleted

Importance of Corner Profile

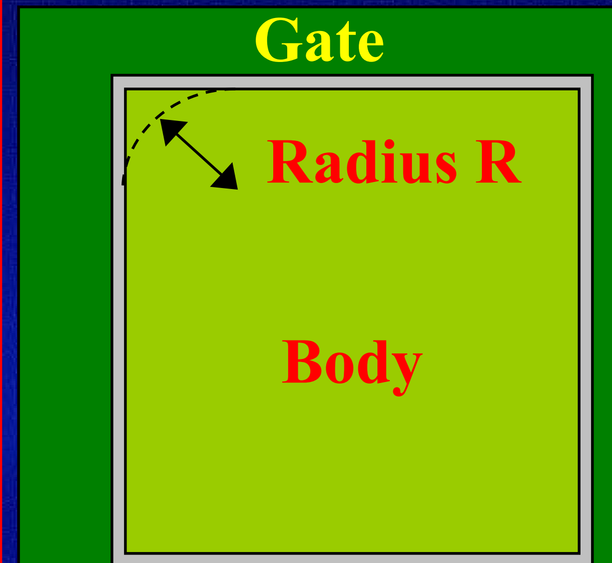
Corner Current (A/μm)

1.E-02
1.E-04
1.E-06
1.E-08
1.E-10
1.E-12

0 0.2 0.4 0.6 0.8 1

Vg (V)

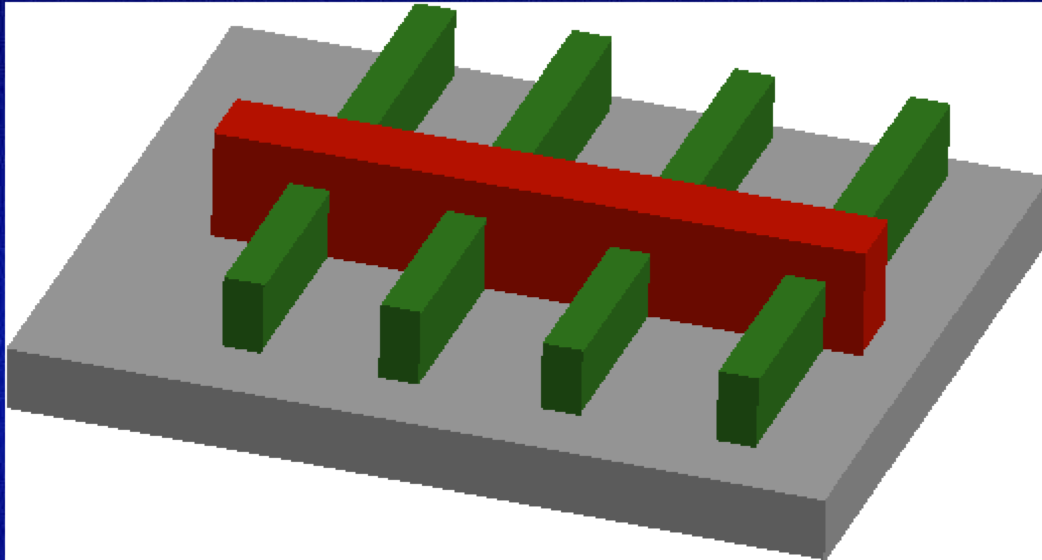
R=0 nm
R=5 nm
R=10 nm
R=15 nm
R=20 nm
R= infinity

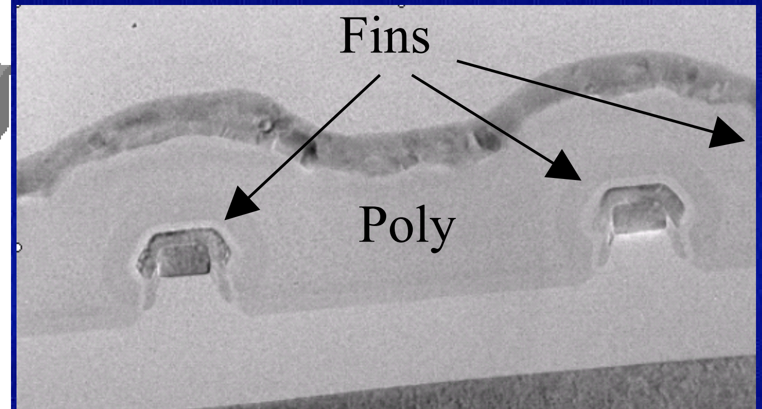


R is the radius of curvature of the corner

Corner profile affects the sub-threshold characterisics of the corner device

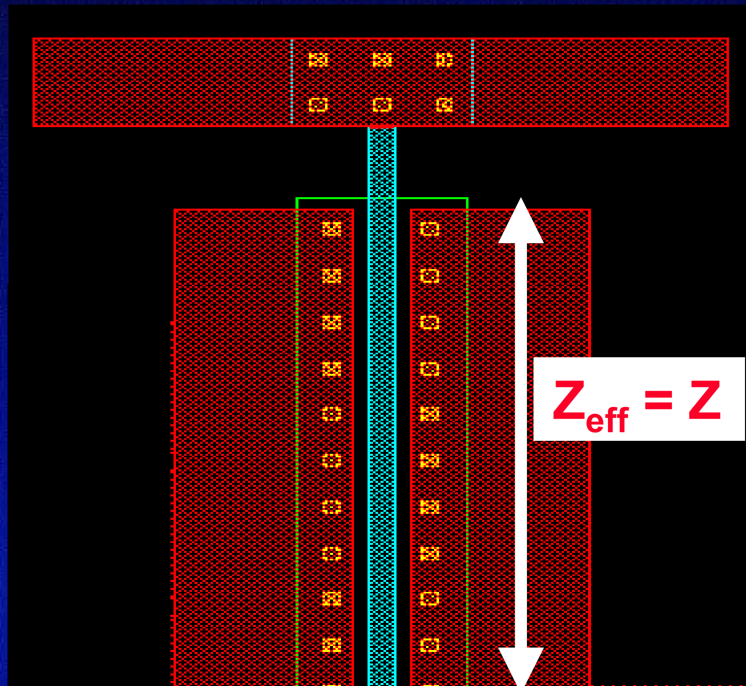
Layout Implications:
Fabricating Different Widths



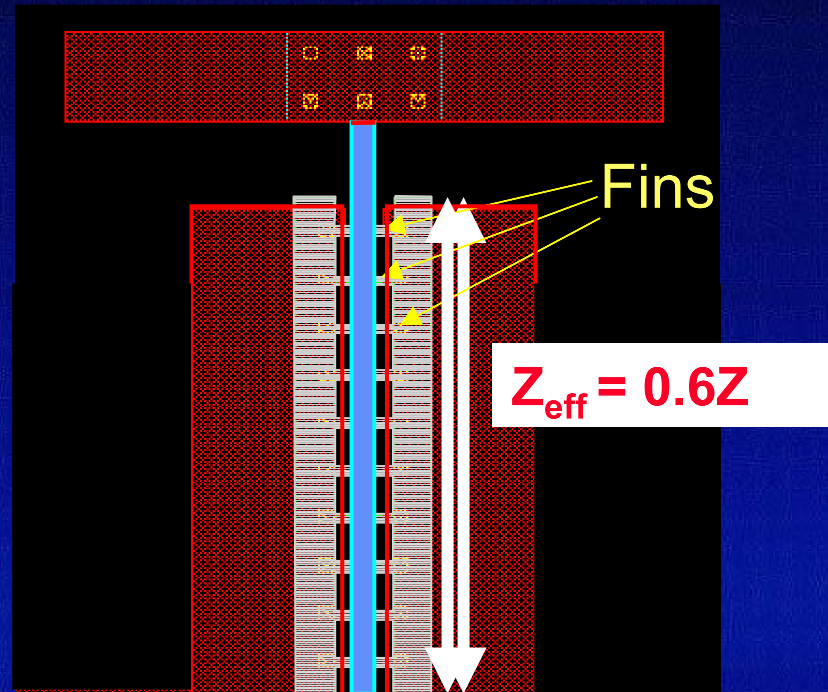


To meet different required widths for transistors, multi-Tri-Gate fins are required. What are the layout width implications?

Layout Considerations



Planar Transistor



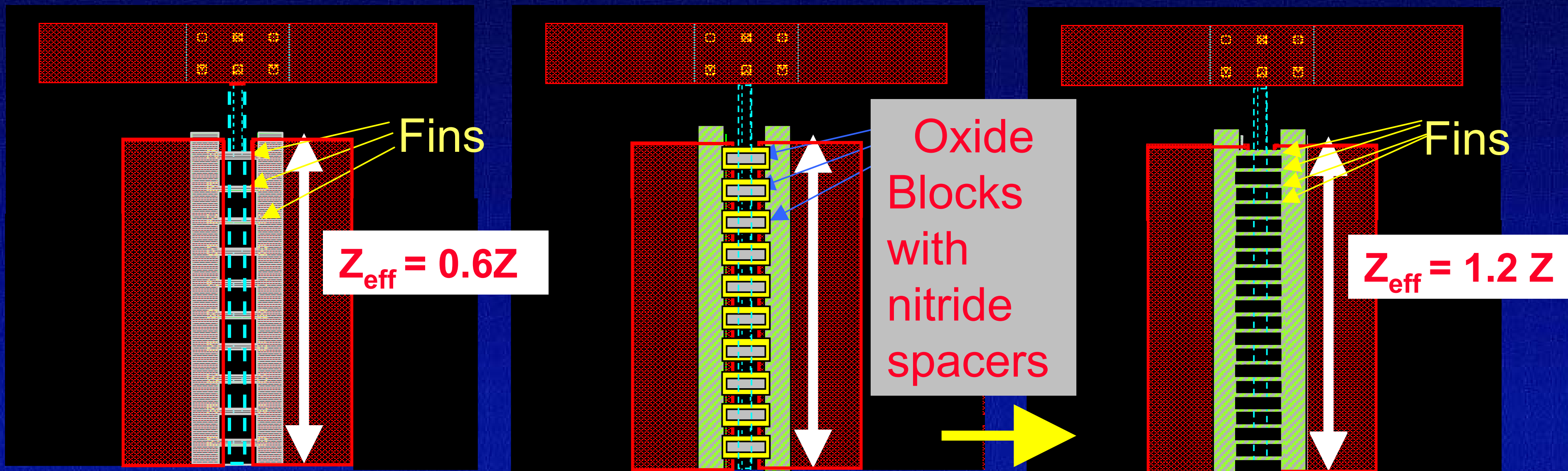
Tri-Gate Transistor

For a given pitch, total current per unit layout-width of the Tri-gate transistor has only 0.60X the channel width of the standard transistor

- *Need to use spacer-litho technique to double the # of fins for a given pitch to increase total current*

(R.Chau et al., SSDM, Nagoya, Japan, Sept. ,2002)
(C-M Hu et al., IEEE Trans El Dev.,Vol. 49, pp. 436-441, 2002)

Spacer-Defined Fins



Litho-defined Fins

Oxide blocks to define spacer-masks for forming Si fins

For the same pitch, # of spacer-defined fins doubles that of litho-defined fins

- Use of spacer-litho technique enables the Tri-gate transistor to have 20% more total current per unit layout-width than the standard planar transistor

Conclusions

- Tri-Gate transistors have been fabricated and achieve excellent drive current with near-ideal DIBL, S/S.
- Tri-Gate corners are responsible for the excellent sub-threshold slope, DIBL characteristics, as well as relaxing the body dimensions compared to double-gate devices.
- In addition to the corners, the top-gate and sidewall channel regions are important in achieving optimal device performance.
- Layout analysis shows Tri-Gate achieves 20% higher total current per unit layout area than standard planar devices.