Schottky-Barrier Engineering for Low-Resistance Contacts

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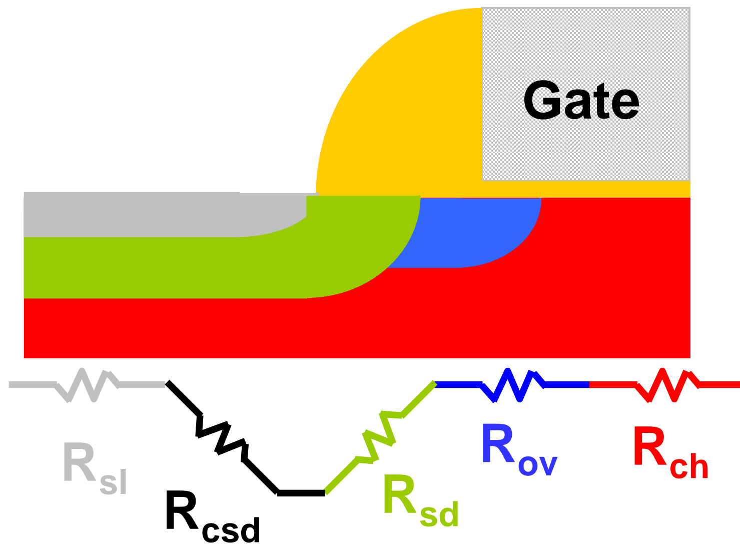
Outline

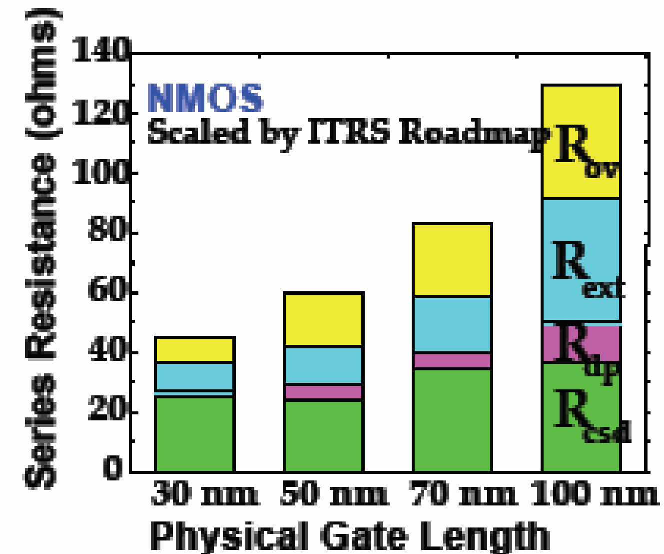
- **Introduction**
- **Characterization Schemes**
- **$Si_{1-x}Ge_x$ Source/Drain**
- **Dopant Segregation**
- **Strain**
- **Summary**

Parasitic Resistance Components



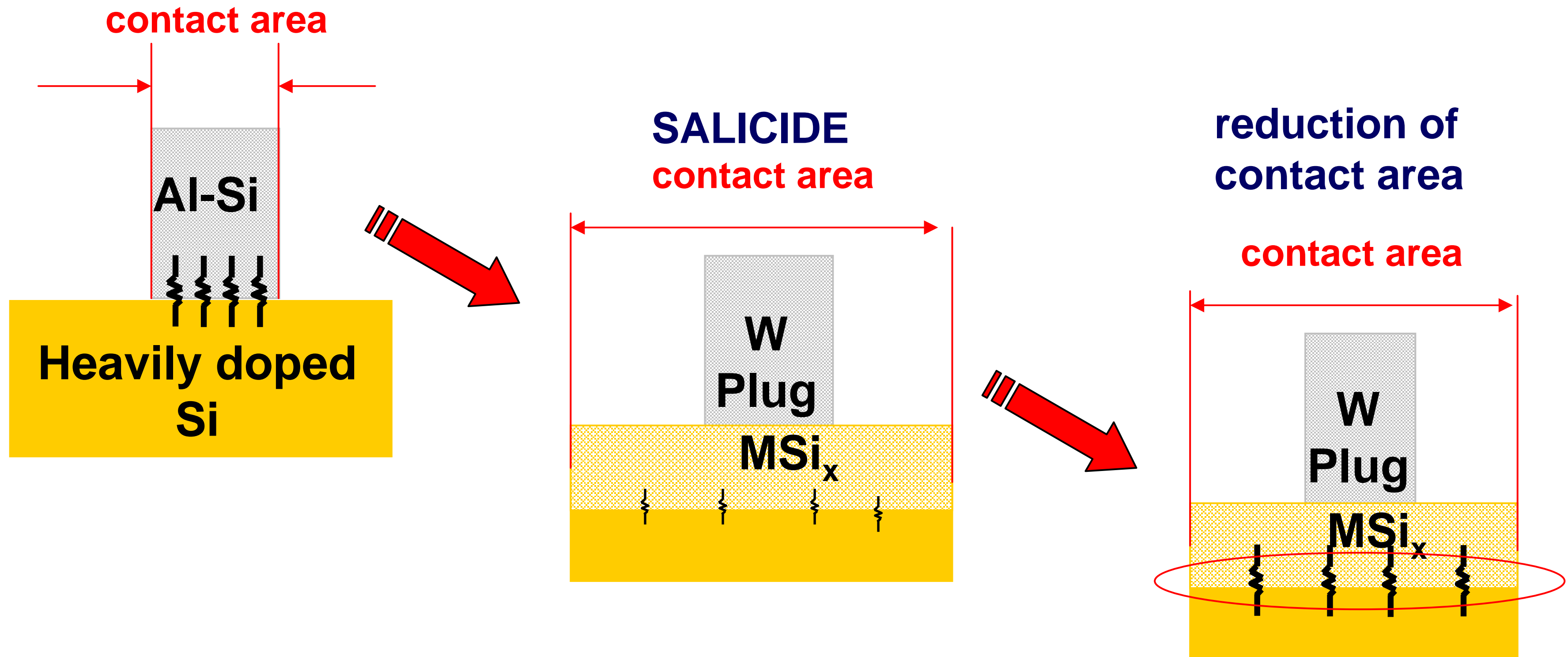
- $\mathbf{R_{sl}}$ Silicide sheet resistance
- $\mathbf{R_{csd}}$ Contact Resistance
- $\mathbf{R_{sd}}$ Silicon Sheet Resistance
- $\mathbf{R_{ov}}$ Overlap resistance

- Parasitic resistance must be <10% of total FET resistance
- CMOS scaling
  - reduces channel resistance ∝ 1/L
  - increases contact resistance



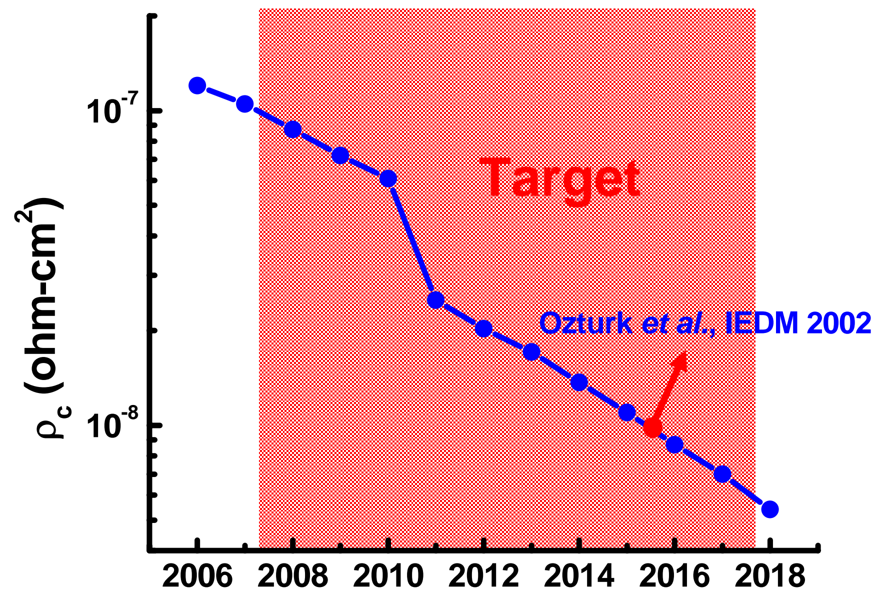
Source: Prof. Jason Woo, UCLA

Contact Resistance Scaling



- Change in contact scheme (adoption of SALICIDE) has extended the contact scaling
- Due to the reduction of active area, silicide/Si contact resistance is now an issue

Int'l Technology Roadmap for Semiconductors (2004 update)



– New materials and processes are needed

Impact of R_c on FinFET

H. Kam and T.-J. King, *2004 Silicon Nanoelectronics Workshop*

L_{gate} = 18 nm, L_{eff} = 22 nm

Wrapped Contact, ρ_c = 0

V_{ds}							
I_{ds} axis: 0, 400, 800, 1200	0	0.1	0.2	0.3	0.4	0.5	0.6

Wrapped Contact

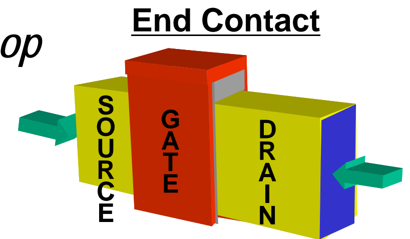
End Contact

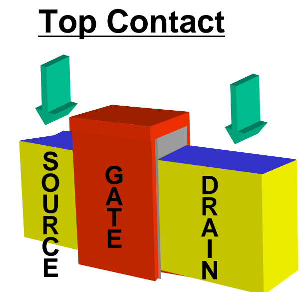
Top Contact

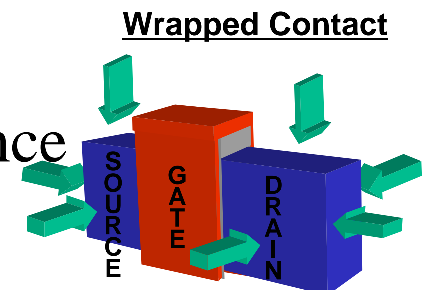
16% reduction

34% reduction

$\rho_c = 10^{-8}\ \Omega\text{-cm}^2$







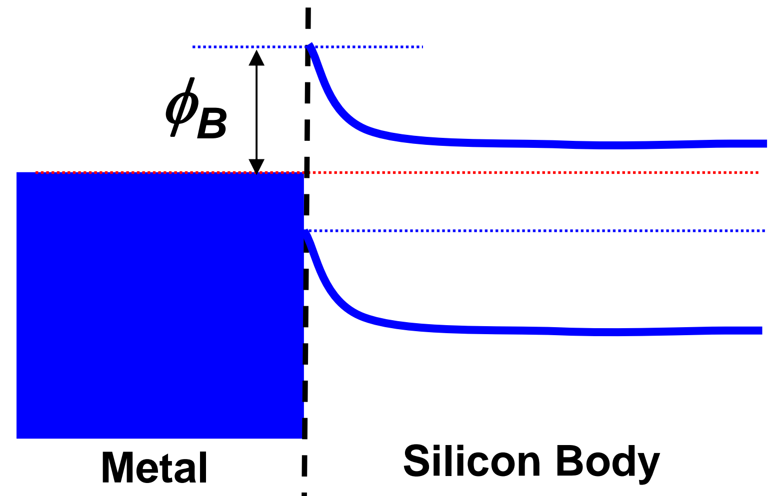
- Parasitic resistances dominate FinFET performance
- $\rho_C < 10^{-8}\ \Omega\text{-cm}^2$ required

Specific Contact Resistivity

Barrier Height and Active Dopant Concentration

$$R_{co} = \frac{\rho_c}{A_c}$$

$$\rho_c \propto \exp\left(\frac{4\sqrt{\varepsilon m^*}}{\hbar}\frac{\phi_B}{\sqrt{N}}\right)$$



– Dopant concentration, N
– Barrier height, ϕ_B

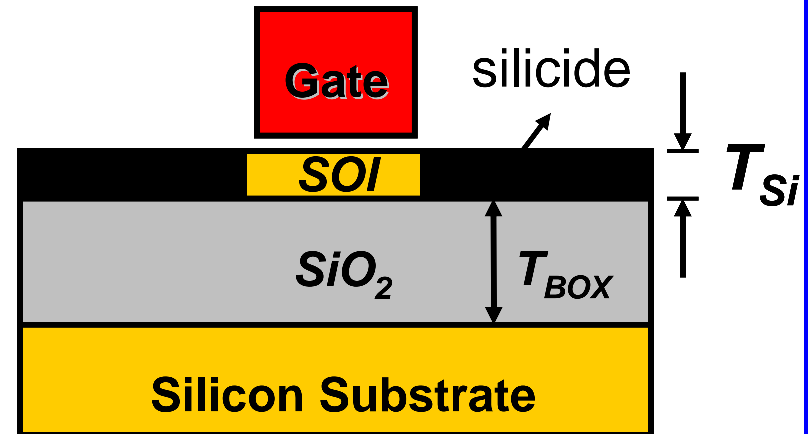
- Fermi-level pinning results in:
  – Barrier height independent of metal work function

Approaches to Lowering ρ_c

- **Material engineering**
  - SiGe source/drain M. Ozturk et al, *IEDM, 2002*
    - smaller bandgap → smaller Schottky barrier
      $\rho_c \sim 10^{-8}\ \Omega\text{-cm}^2$ for Ni germanosilicides on SiGe
    - lower resistivity
- **Barrier height tuning**
  - image force lowering by dopant segregation
    A. Kinoshita *et al.*, *Symp. VLSI Technology, 2004*
  - strain-induced ϕ_B reduction A. Yagishita *et al.*, *SSDM,* 2003
- **Fermi-level de-pinning by interface engineering**
  - insertion of insulator layer D. Connelly *et al.*, *IEEE Trans. Nanotech.*, 2004
  - selenium passivation M. Tao *et al.*, *APL*, 2003

Research Objective

- To understand the mechanisms for tuning the effective Schottky barrier height of a metallic electrode, to guide the engineering of contact-formation processes
  - Low-ϕ_B contacts for reduced parasitic resistance
  - Demonstrate fully silicided source/drain UTB MOSFETs with improved I_{dsat} by reducing ρ_c (to $<10^{-8}$ Ω-cm^2) for silicide-to-silicon contacts



Schematic Cross-section of Silicide S/D UTB MOSFET

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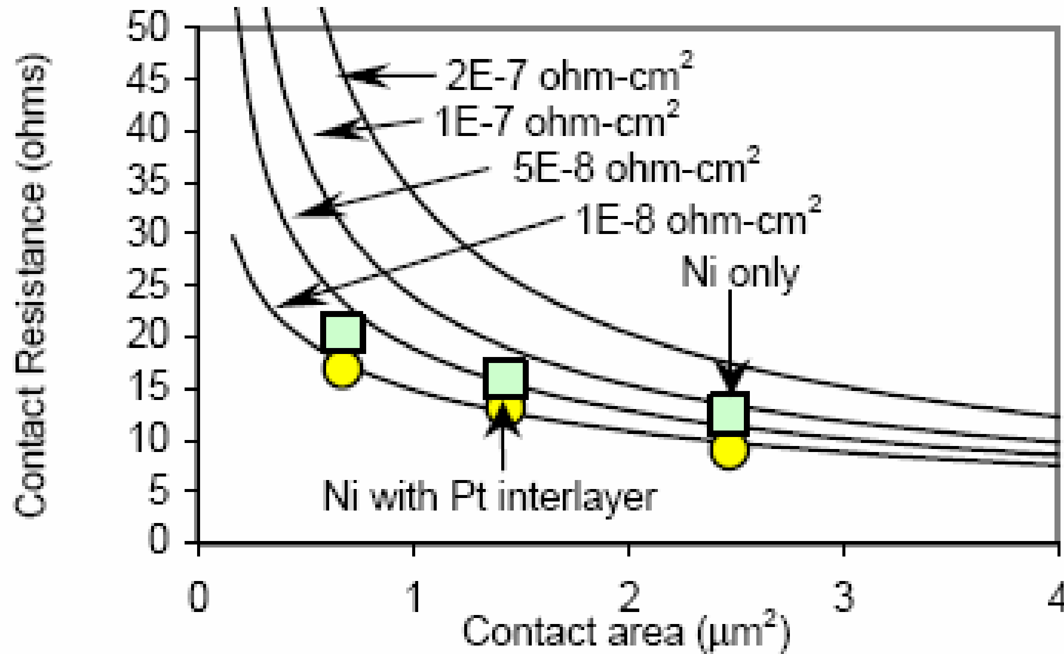
Contact Resistance Measurement



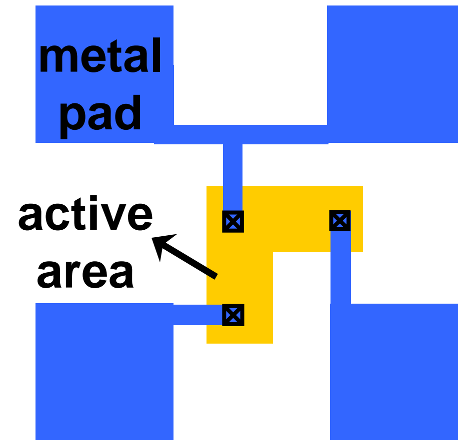
M. Ozturk et al, *IEDM, 2002*

Minimum measurable resistance is ~10 Ω

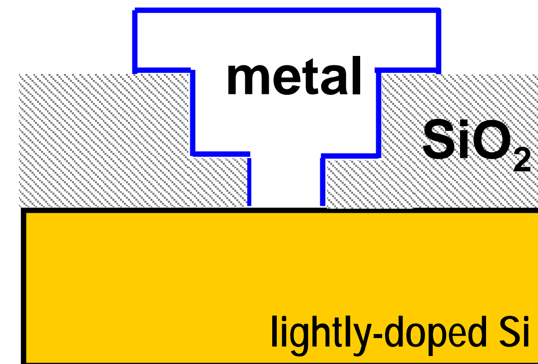
→ Need very small contact holes to determine ρ_c accurately below 10^{-8} Ω-cm^{-2}

Test structures

- Fabrication of Kelvin structures
  - Evaluation of contact resistance
- Fabrication of diode
  - Measure schottky barrier height



Kelvin Structure: Plan View

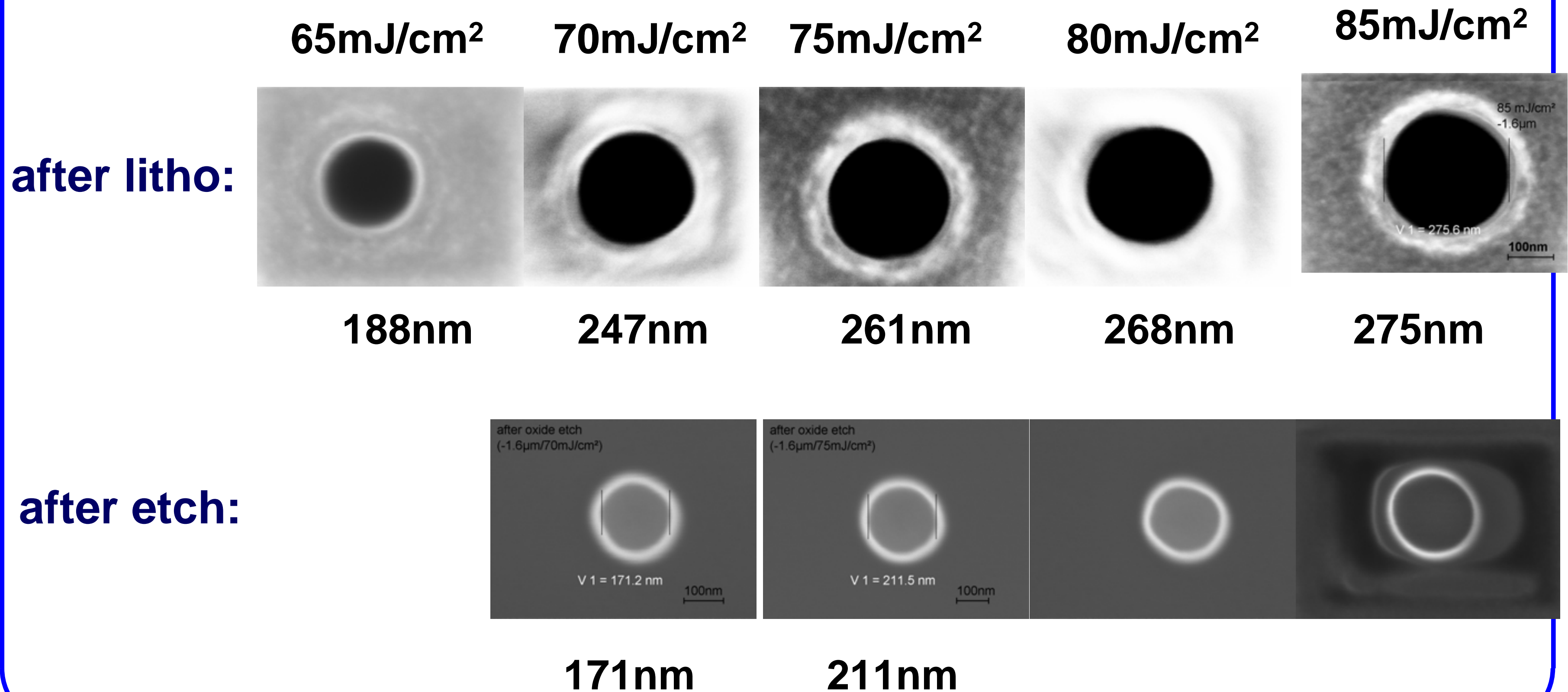


Diode: Schematic Cross section

Fabrication of Sub-0.25µm Contacts

- Contacts were fabricated using DUV stepper

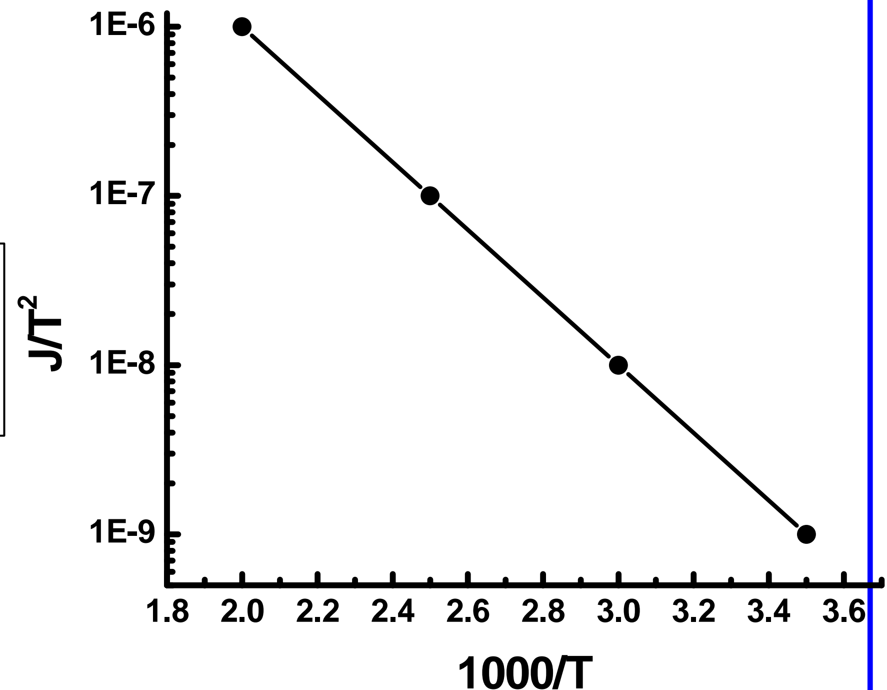
  ASML5500/90; Cymer KrF excimer laser (l=248nm)



ϕ_B extraction

- Measure diode *I-V* characteristic at different temperatures

$$\ln\left(\frac{I_F}{T^2}\right) \approx \ln\left(A_e A^{**}\right) - \frac{q}{kT}\left(\phi_{Bn} - V_F\right)$$



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  (This work is sponsored by the FLCC project)
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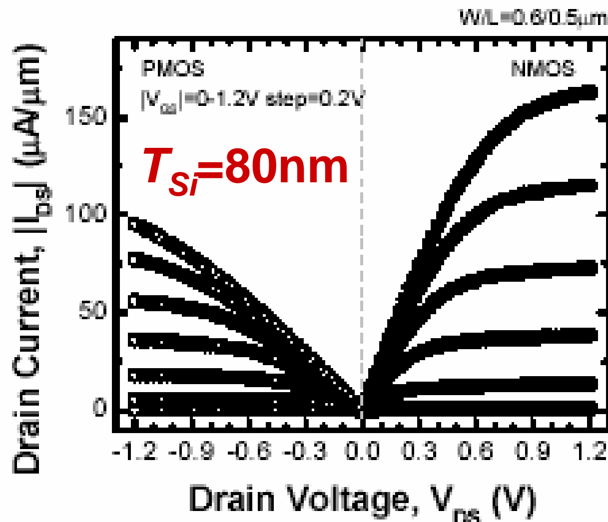
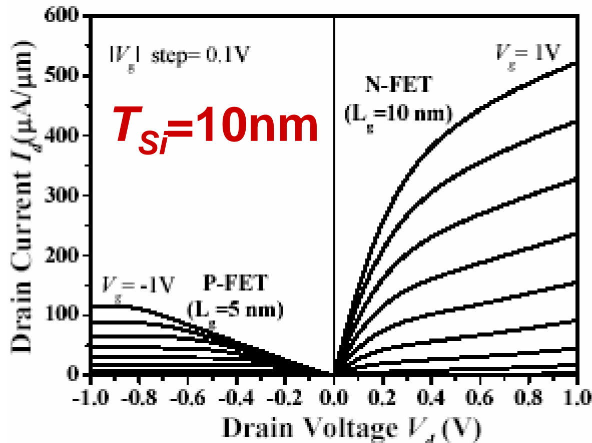
Dopant Behavior in Ultra-Thin SOI



D. Ha *et al.*, *IEDM* 2004



F.-L. Yang *et al., 2004 Symp. VLSI Technology*

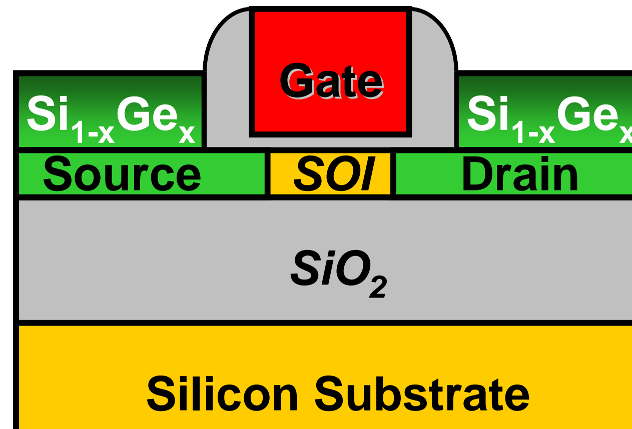
- P-channel thin-body FETs exhibit higher series resistance

→ Different behaviors of B and P in ultra-thin Si

  – dopant segregation to interface(s), or into surrounding oxide?

Epitaxial $Si_{1-x}Ge_x$ Source/Drain

- Epitaxial $Si_{1-x}Ge_x$ source/ drain regions for lowering R_{series} and inducing compressive strain to enhance hole mobility
  - Conventional approach for epitaxial growth of $Si_{1-x}Ge_x$ is not possible for thin-body devices because there is not sufficient crystalline substrate after S/D etchback



Approach

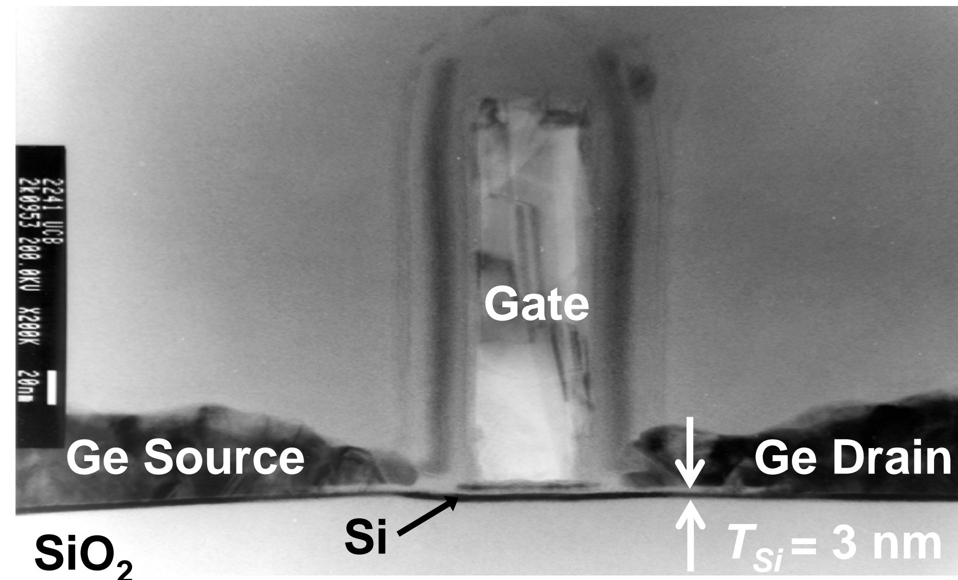
- Develop a process for selectively forming strained $Si_{1-x}Ge_x$-in-SOI by intermixing Ge & Si
  - Study the intermixing of Ge with SOI films
    - effects of anneal temperature, time, boron doping
  - Investigate strain in the resultant $Si_{1-x}Ge_x$ alloy
  - Characterize metal-to-$Si_{1-x}Ge_x$ contact resistance
  - Germano-silicidation of $Si_{1-x}Ge_x$ to achieve dopant pile-up (to study ϕ_B reduction)

Advantages of This Approach

- **Selective deposition of Ge by conventional LPCVD**
  - GeH_4 gas, 320°C, 200mT
  - high process throughput (batch process)

  → **low cost**

XTEM of UTB MOSFET w/ raised Ge S/D

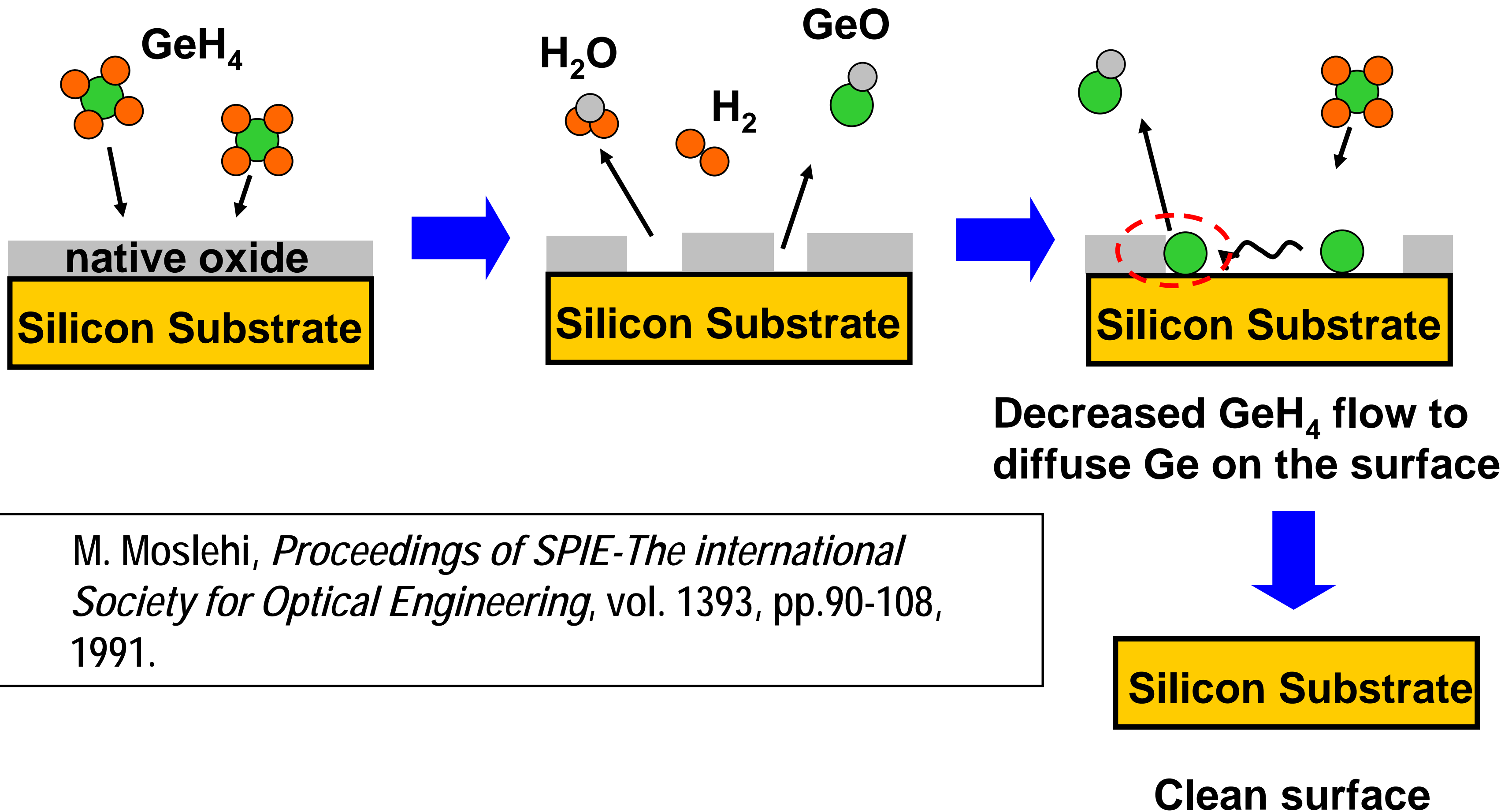


Y.-K. Choi *et al.*, *IEEE Electron Device Lett.*, Vol. 22, p. 447, 2001

Ge/Si Interface Preparation

- Selective Ge deposition in LPCVD furnace requires a clean silicon surface
  - Interface preparation is critical
- Native oxide removal methods
  - *in-situ* HF vapor clean
  - *in-situ* HF vapor clean and Hydrogen bake
  - HF dip followed by Hydrogen bake
  - *in-situ* cleaning by GeH_4
  - Si I/I after Ge deposition
    - for breaking up any native oxide at the Ge/Si interface

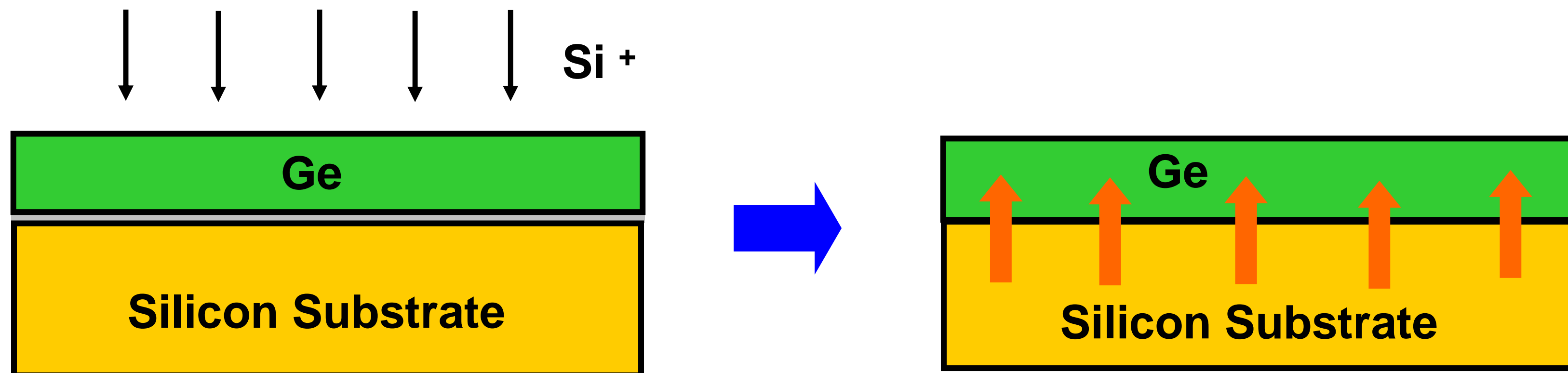
In-Situ GeH_4 Cleaning



Si Ion Implantation to Break Up Native Oxide

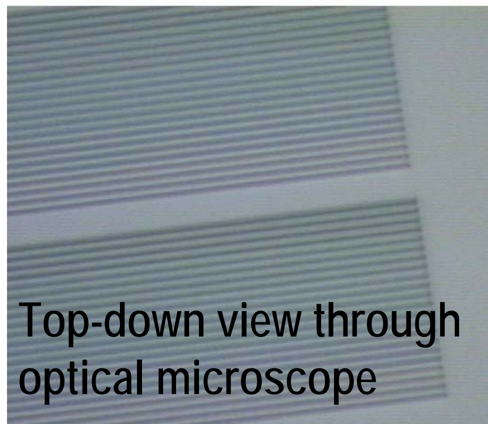
- Si^+ implant has been used to break up the native oxide barrier for Solid-Phase Epitaxy (SPE)

Y. C. Yeo *et al.*, *IEEE Transactions on Electron Devices,* Vol. 49, No. 2, pp.279-286, 2002.



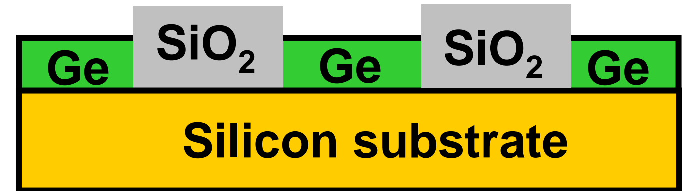
Test Sample Process Flow

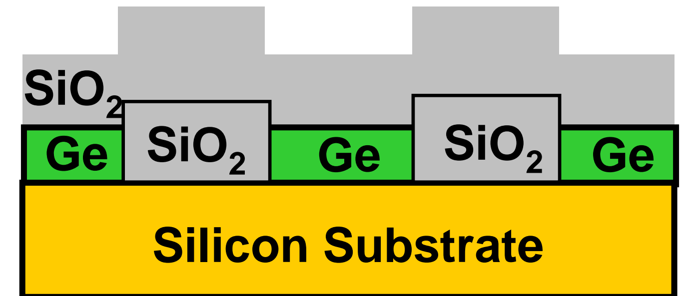
- Starting wafers
  - n-type, ρ=5-10 $\mu\Omega$-cm
- Cross-sectional TEM pattern formation
  - CVD SiO_2 deposition (52nm)
  - Lithography
  - Oxide etching (90% dry + 10% wet)

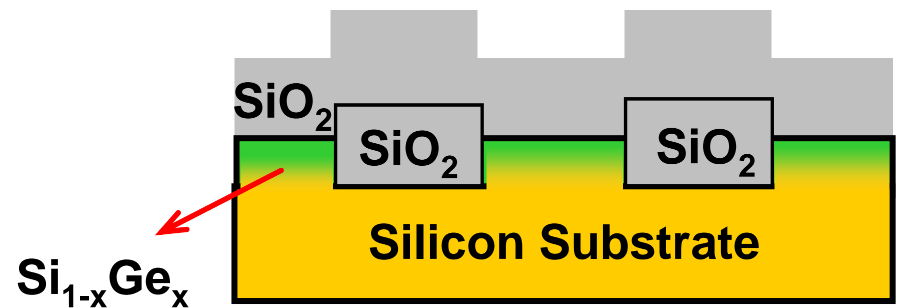


Process Flow (Cont'd)

- Interface Preparation
  - HF last / HF vapor
- Selective Ge deposition (22nm)
  - 320°C/200mTorr/100sccm
  - Capping layer (25nm)
- Si Implant
  - Si : 40keV, 1E15 cm^{-2}
- Doping
  - B : 10keV, 2E15 cm^{-2}
- Recrystallization
  - 500°C, 1 hour
- Intermixing anneal
  - 800°C/ 850°C, 1minute

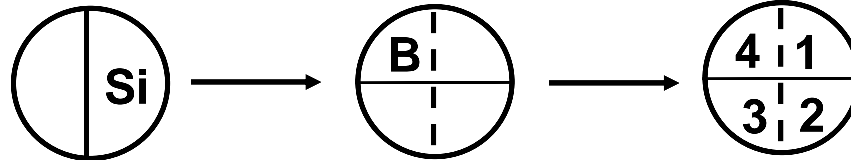






Experimental Splits

on wafer splits = 4



1	Si I/I + B I/I
2	Si I/I
3	none
4	B I/I

Split Table:

Wafer ID																	
Cleaning	HF Last	x	x	x	x	x	x	x	x								
	HF vapor									x	x	x	x	x	x	x	x
I/I splits	Si I/I	x				x				x				x			
	B I/I		x				x				x				x		
	Si I/I + B I/I			x				x				x				x	
	none				x				x				x				x
Annealing	800 C	x	x	x	x					x	x	x	x				
	850 C					x	x	x	x					x	x	x	x

Determining Ge and B profiles

(in collaboration with Prof. Haller's group)

- Characterization of vertical and lateral co-diffusion of Ge and B
  - Available Options:
    - Cross-sectional TEM with EDX nanoprobe
    - Cross-sectional TEM with EELS
    - Cross-sectional SEM with EDX nanoprobe

Summary and Future Goals

$Si_{1-x}Ge_x$ Source/Drain

- Fabrication of first batch is finished
  - Splits for Doped/ undoped Ge, interface preparation, annealing conditions etc.
  - Results of this batch are awaited
- Future Work:
  - Characterization of boron-doped $Si_{1-x}Ge_x$-on-insulator resistance
  - Characterization of metal-to-$Si_{1-x}Ge_x$ contact resistance
    - Germano-silicidation of $Si_{1-x}Ge_x$ to achieve dopant pile-up for Schottky barrier height (ϕ_B) reduction

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- Strain
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ϕ_B Reduction by Dopant Segregation

- ϕ_B can be reduced by using an ultrathin (<10nm) heavily doped layer at the semiconductor surface

J. Shannon, *Applied Physics Letters*, Vol. 24, pp. 369-371, 1974.

  – image force lowering ($\Delta\phi$) due to surface electric field

$$\Delta\phi = \frac{q}{\varepsilon_{si}}\sqrt{\frac{Na}{4\pi}}$$

N = dopant concentration in surface layer
a = width of heavily doped surface layer

Such a thin heavily doped layer can be formed by silicidation-induced dopant segregation:

A. Kinoshita *et al.*, *2004 Symp. VLSI Technology, Digest of Technical Papers*, pp. 168-169.

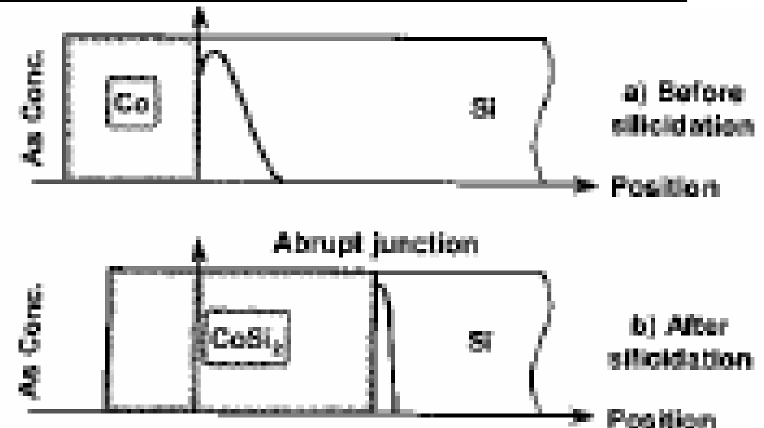


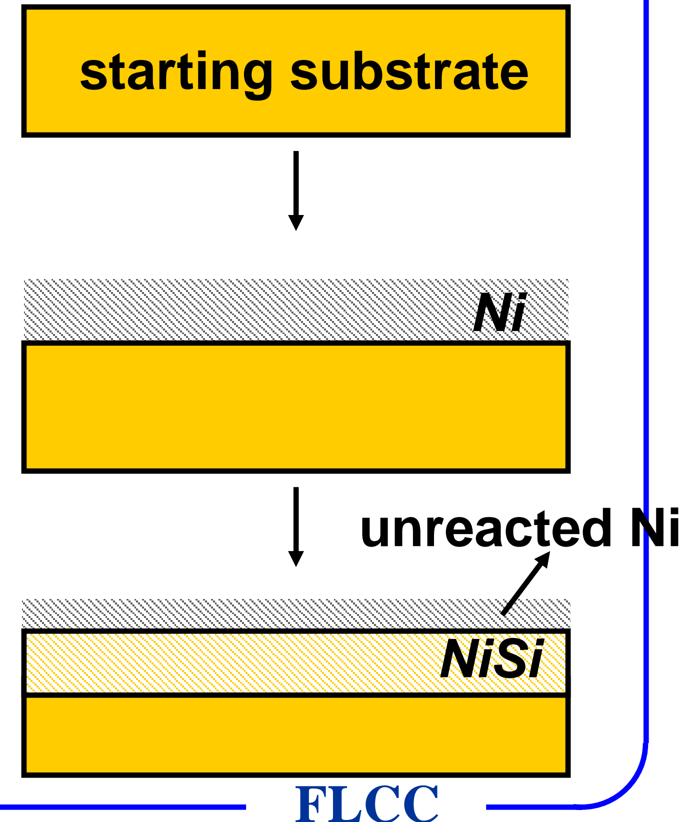
Fig.3 Schematic of DS technique, which was proposed by R. L. Thornton [10].

Experiment

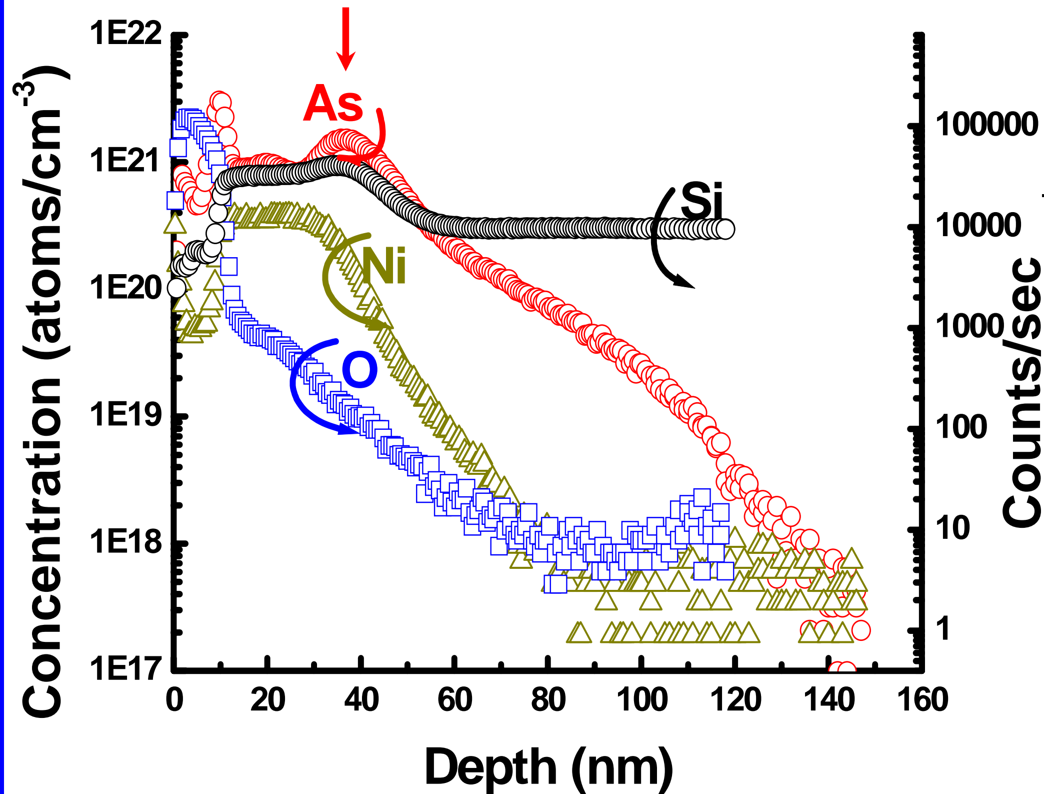
Goals: Confirm dopant segregation w/ NiSi
Investigate dopant activation

Process sequence:

- **starting Si wafer (n-type/ p-type)**
- **deposit capping layer, CVD SiO_2**
- **blanket implantation**
  (B- 20KeV, $10^{16}cm^{-2}$ As- 80KeV, $6\times10^{15}cm^{-2}$)
- **spike annealing@1000C**
- **strip capping layer**
- **excimer laser annealing**
- **Ni deposition**
- **silicidation**
- **strip unreacted Ni**



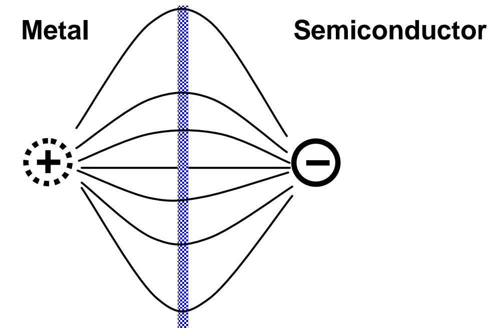
Results: SIMS Analyses

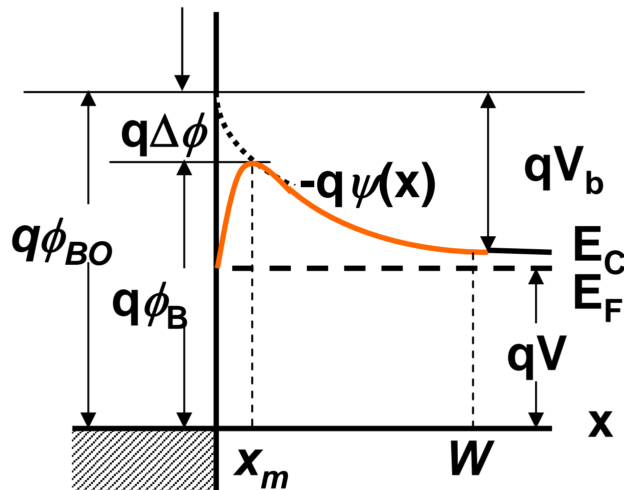


– Dopant pile-up at silicide/ Si interface is seen for both As and B doping (only As shown here)

Schottky Barrier Lowering

- Image Force Effect
  - Induced charges at the interface
  - Equivalent to an image charge





$$x_m = \sqrt{\frac{q}{16\pi\varepsilon_S E}}$$

$$PE(x) = -\frac{q^2}{16\pi\varepsilon_s x} - qEx$$

$$\Rightarrow \Delta\phi = \sqrt{\frac{q}{4\pi\varepsilon_s}} \bullet \sqrt{E}$$

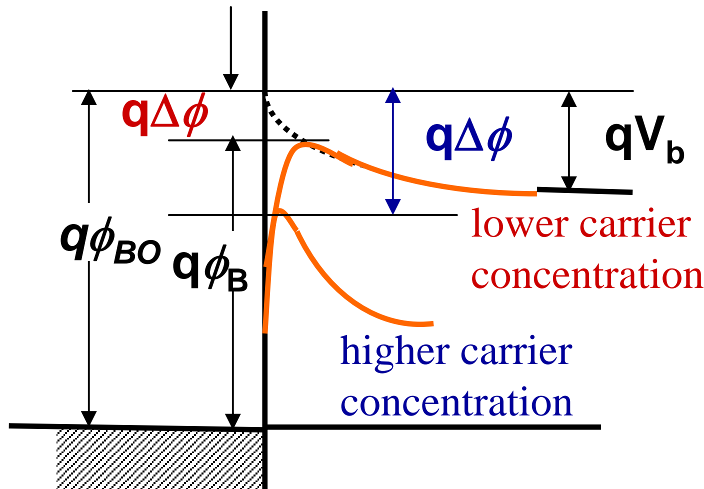
Tailoring the Surface Electric Field

- $\Delta\phi$ depends on the surface electric field
  - Lightly doped substrate:
    - Low E, barrier-lowering is sensitive to reverse bias
  - Heavily doped substrate:
    - High E → ϕ_B is reduced, but reverse current increases

      ➔ tunneling Ohmic contact !
- To retain Schottky junction properties and to achieve $\Delta\phi$ that is insensitive to bias, a heavily doped surface layer that is fully depleted by the built-in potential is needed

Fully-Depleted Doped Surface Layer

- The required electric field has been shown to be $>5\times10^5$ V/cm
  J. Shannon, *Applied Physics Letters,* Vol. 24, pp. 369-371, 1974.
  - Maximum surface field arising from implantation of a symmetrical distribution of charge about range R_p:



$$E_{s,\max} \cong \frac{V_b}{R_p}$$

$$qV_b = q\phi_{B0} - (E_c - E_f)$$

For a metal contacting a lightly doped substrate, built-in potential V_b~0.45V

$$\Rightarrow R_p < 100A$$

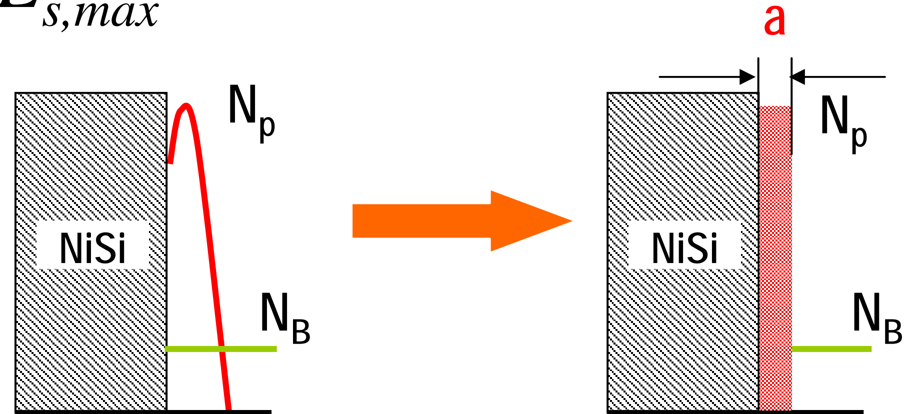
Φ_B Reduction Model

- Maximum surface field, $E_{s,max}$

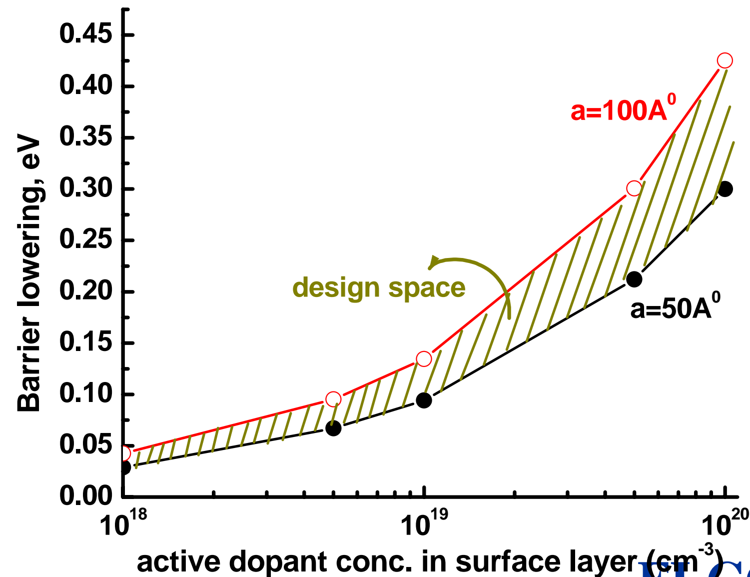
$$E_{s,\max} = \frac{q}{\varepsilon_s}\left[N_p a + N_B (W - a)\right]$$

$$E_{s,\max} \cong \frac{q}{\varepsilon_s} N_p a$$

$$\Rightarrow \Delta\phi \cong \frac{q}{\varepsilon_s}\sqrt{\frac{N_p a}{4\pi}}$$



Expected barrier height lowering due to a thin highly doped surface layer:

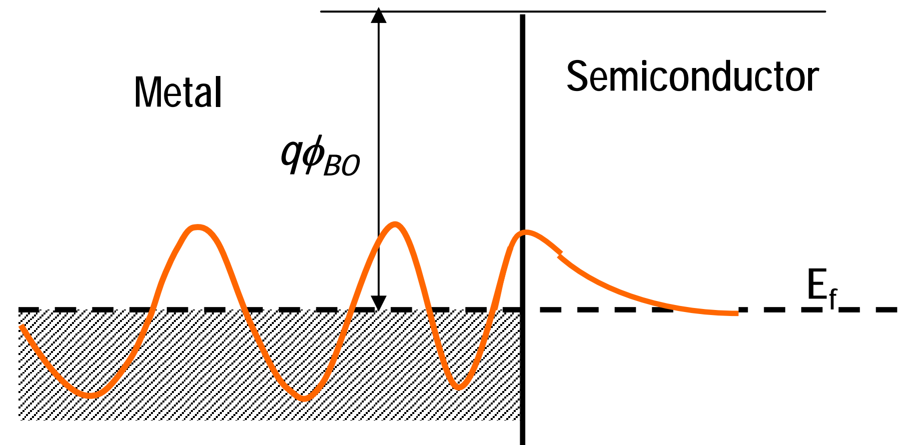


Effect of Interface States

- Metal-induced gap states (MIGS)
  - Penetration of wave function from the metal into the forbidden energy gap of Si

Electron potential energy including the contributions of image force and MIGS

K. Shenai *et al.*, *IEEE TED*, Vol. ED-32, No. 4, pp. 793-799, 1985



Metallic wave penetration in metal-semiconductor system

$$PE(x) = -\frac{q^2}{16\pi\varepsilon_s x} - qEx - \frac{qQ\lambda}{\varepsilon_s} e^{-x/\lambda}$$

Q = magnitude of surface state charge

λ = penetration depth of surface state charge

$\Delta\phi$ Inverse Modeling Approach

– Find the location of *PE(x)* minimum

$$\frac{d}{dx}(PE(x))\Big|_{x=x_m} = 0 \quad \Rightarrow \frac{q^2}{16\pi\varepsilon_s x_m^2} - qE(x_m) + \frac{qQ}{\varepsilon_s} e^{-x_m/\lambda} = 0$$

– Total barrier lowering is given by

$$\Delta\phi = \frac{q}{16\pi\varepsilon_s x_m} - \psi_0(0) - \psi_0(x_m) + \frac{Q\lambda}{\varepsilon_s} e^{-x_m/\lambda}$$

– Solve Poisson's equation to find $\Psi_0(x)$

$$\nabla^2\psi_0(x) = -\frac{\rho(x)}{\varepsilon_s}$$

– Extract Q and λ from measured forward *I-V* characteristics

– Predict total barrier lowering from the model

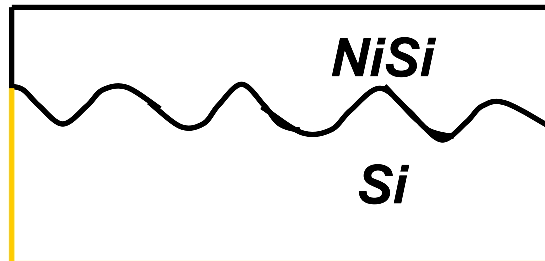
- N_p, work-function difference, Q, and λ are input parameters

Determining Active Dopant Concentration

- Spreading Resistance Probe (SRP):
  - within 1/2 the probe spacing (~10μm) of the Si/ silicide interface, silicide starts affecting readings because of low resistance

→ Need to remove NiSi selectively

- surface roughness increase
- difficult to find bevel edge



Summary and Future Work

Dopant Segregation

- Ni silicidation induced dopant segregation phenomenon confirmed
- A quantitative inverse-modeling approach has been established for determining the amount of Schottky-barrier lowering
- Future Work:
  - Fabrication and characterization of diode structures and Kelvin structures
  - Application of dopant-segregation technique to improve FinFET performance by reducing S/D contact resistance

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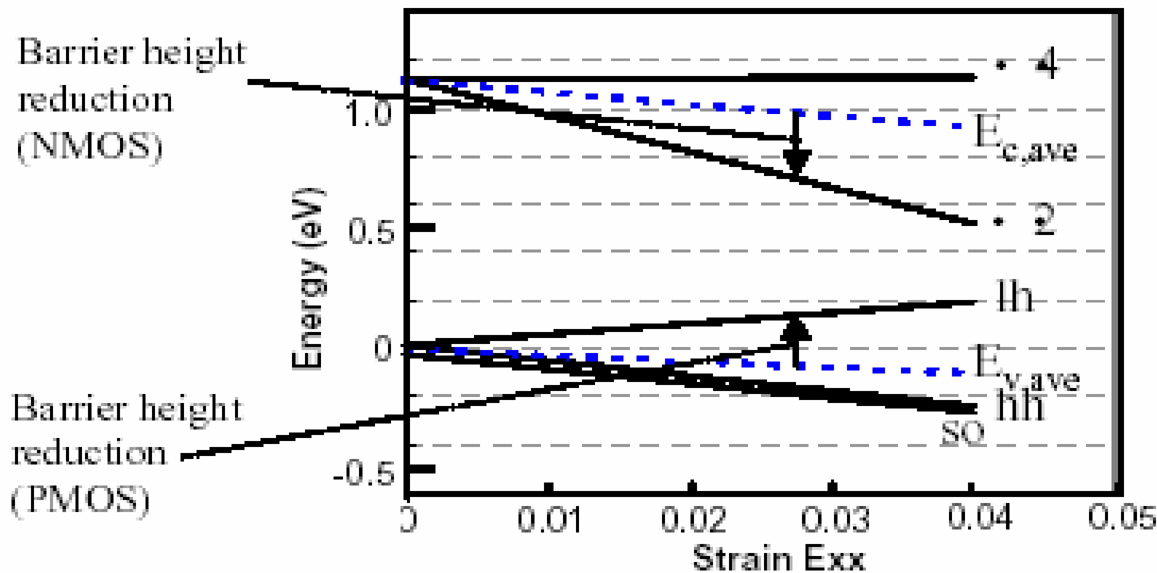
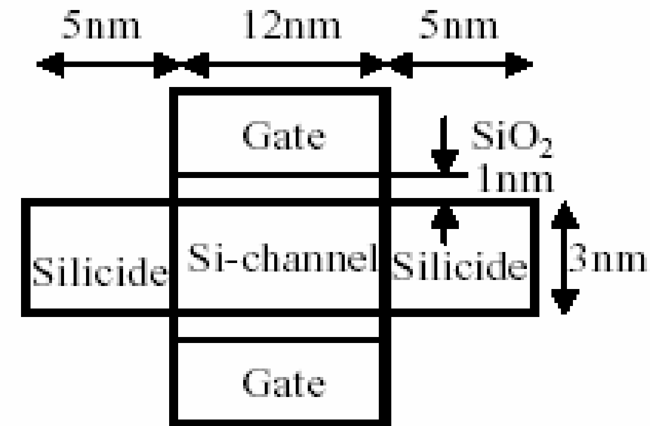
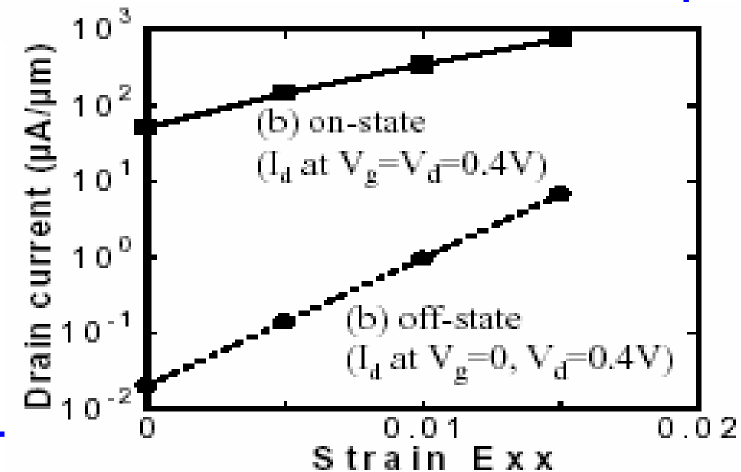
ϕ_B Reduction by Si Strain

A. Yagishita *et al.*, *SSDM* 2003



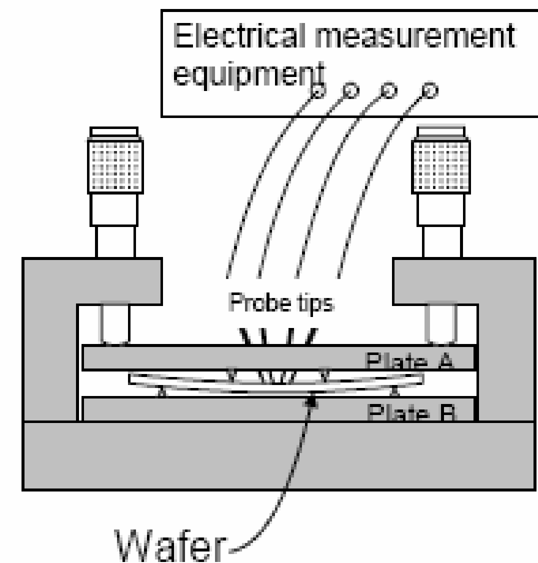




– 1% bi-axial strain reduces ϕ_B by 0.1eV ($ErSi_{1.7}$ S/D NMOSFET)

Experimental Plan

- Use a bending apparatus
  - apply uniaxial or biaxial bending stress to Si chips
- Study ϕ_B reduction
  - Fabricate Schottky diodes and contact test structures to measure effect of strain on ρ_c



K. Uchida *et al.*, *IEDM* 2004

Outline

- **Introduction**
- **Characterization Schemes**
- **$Si_{1-x}Ge_x$ Source/ Drain**
- **Dopant Segregation**
- **Strain**
- **Summary**

Summary

- Source/drain contact resistance can limit the performance of nanoscale FETs
  - $\rho_c \sim 10^{-9}\ \Omega\text{-cm}^2$ will be required
- Approaches for reducing ρ_c include use of $Si_{1-x}Ge_x$ in the source/drain regions, dopant segregation, and strain
- Work in progress will clarify the mechanisms for lowering the effective Schottky barrier height ϕ_B

→ Application to nanoscale thin-body FETs

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