Power Amplifier Linearization using RF Pre-Distortion

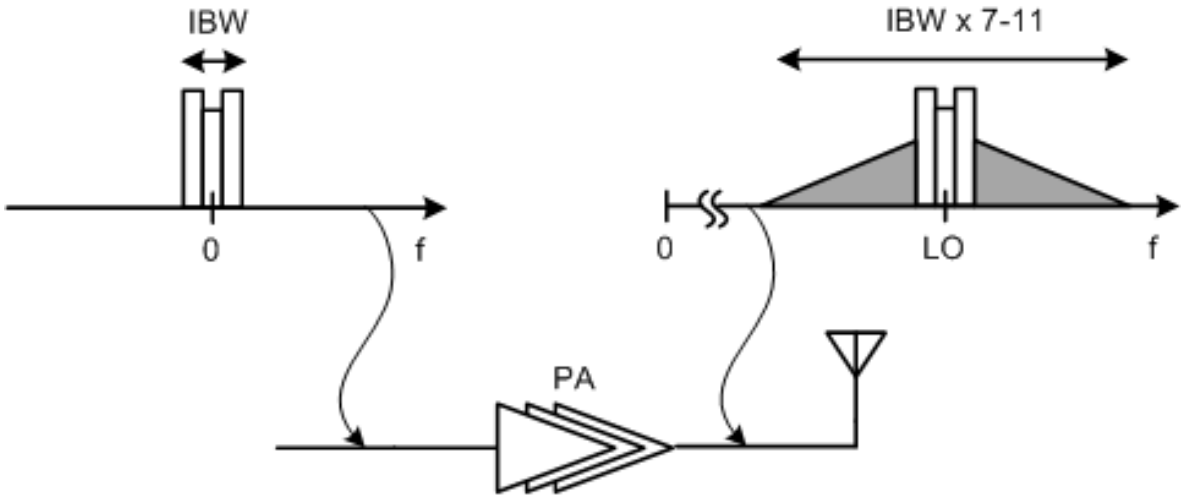
JUNE, 2012

PA Linearization Overview

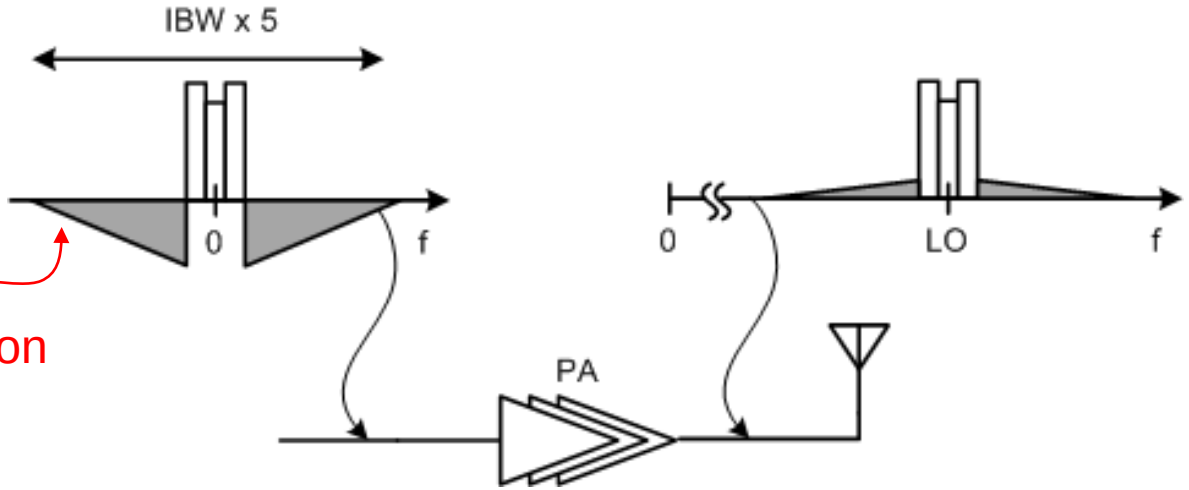
- General principles
- Overview/Block Diagram of DPD and RFPD
- RFPAL System architecture & Implementation

Predistortion Principle

No predistorion



With predistorion



5-10 x BW expansion

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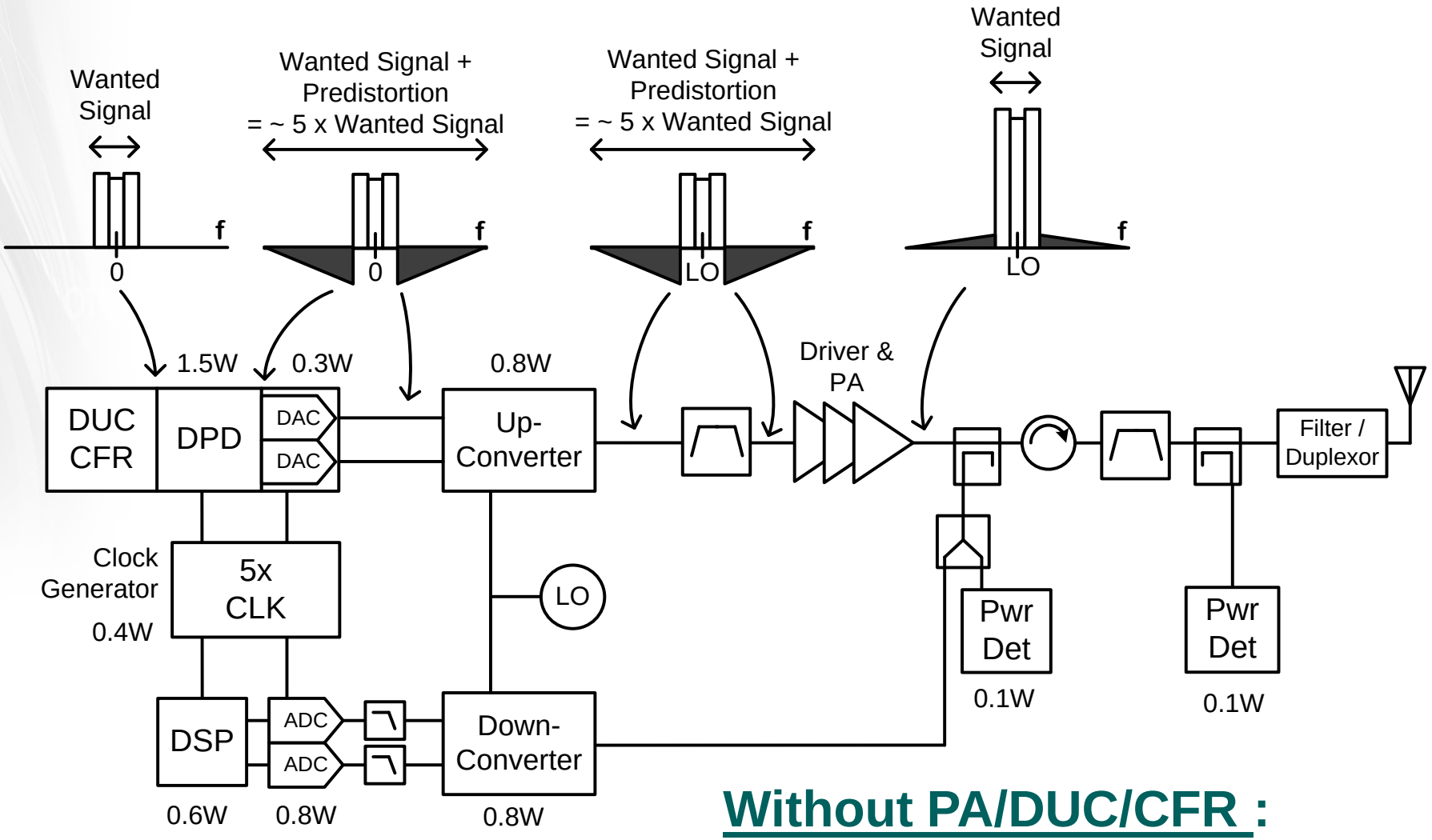
Digital Pre-Distortion (DPD)



Without PA/DUC/CFR :

Power consumption ~5.4W

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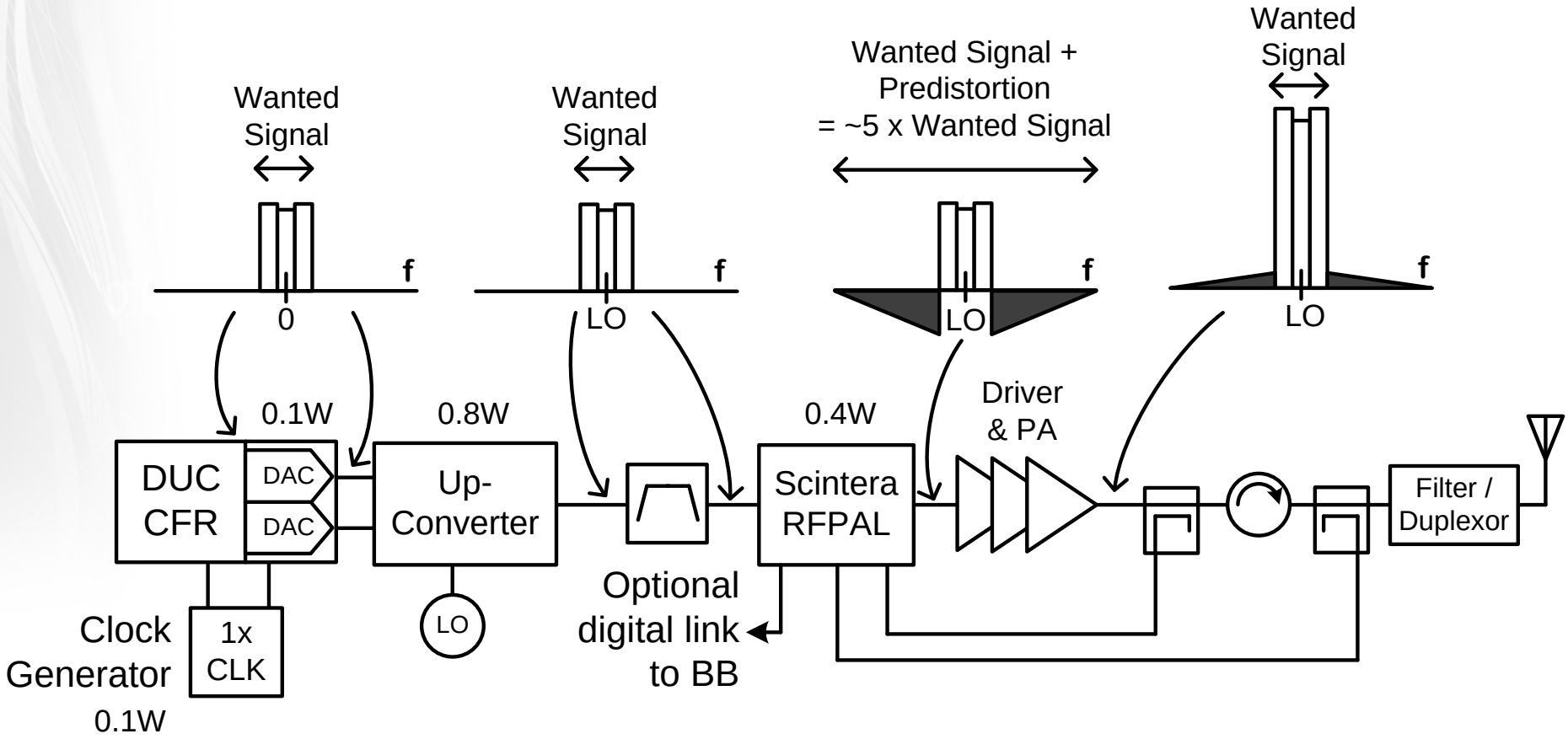
RFPAL (RF PA Linearization)



Without PA/DUC/CFR

Power consumption ~1.4W

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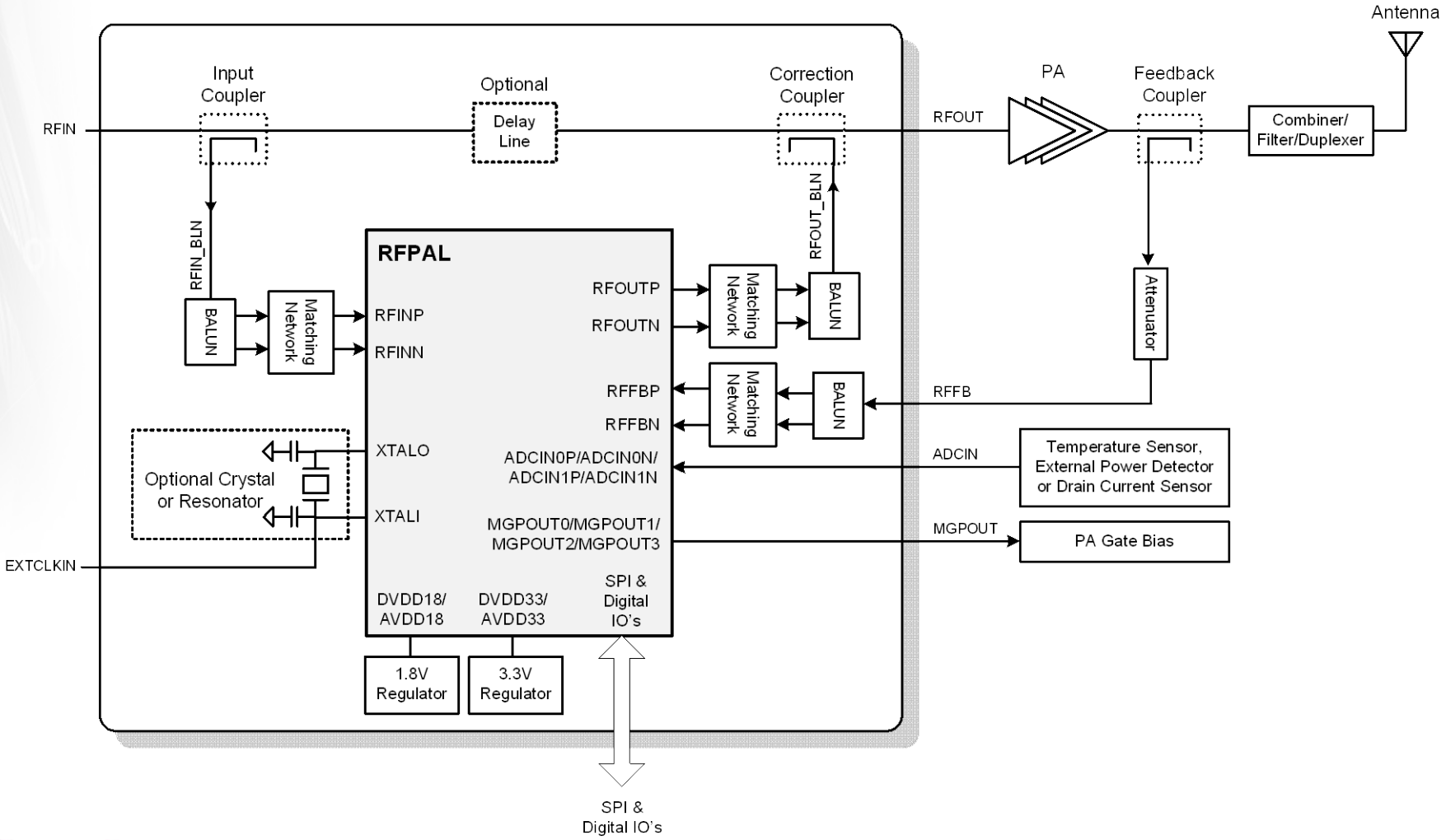
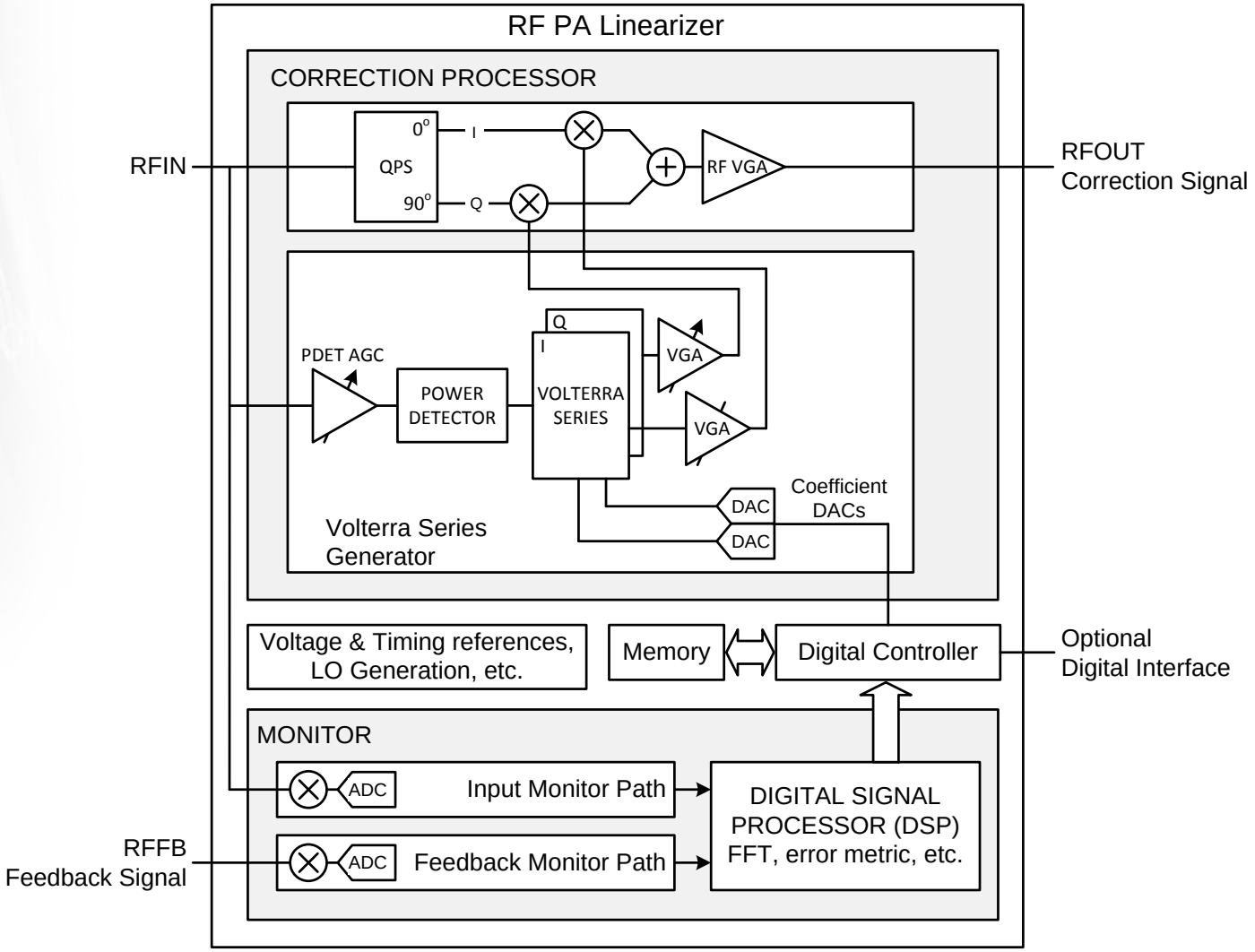
RFPAL System Architecture & Implementation

RFPAL Application



RFPAL System Architecture



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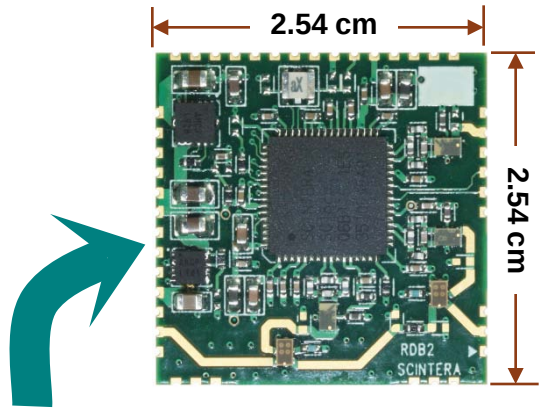
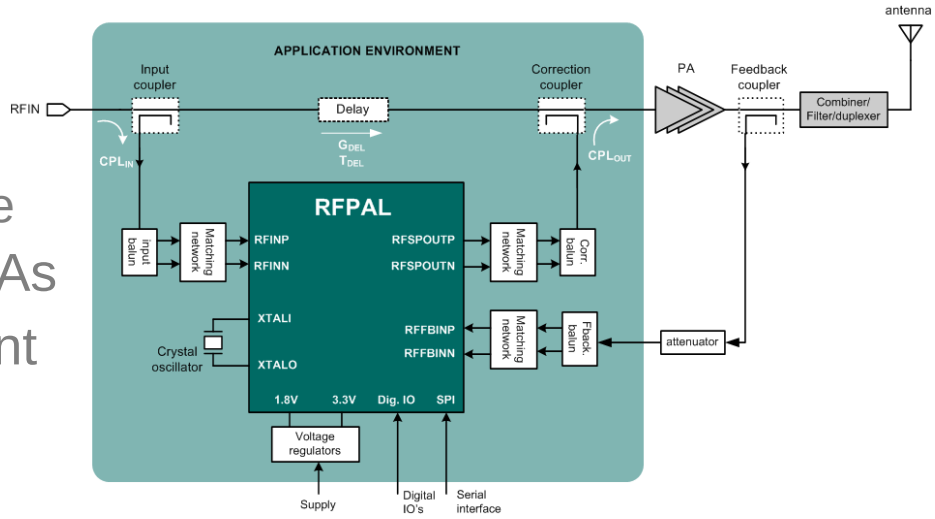
Scintera Advantages

- Single chip CMOS linearization solution
  - Easy to evaluate and design in
  - Simplifies TX chain
- High system efficiency
  - Very low power consumption
- Low system cost
- Small footprint
- Future proof
  - In-system & in-field reprogrammable
- RFin/RFout supports stand-alone PAs
- Waveform & modulation independent
- Power Amp Independent
  - Linearize even lowest power PAs
- Robust & field-proven solution





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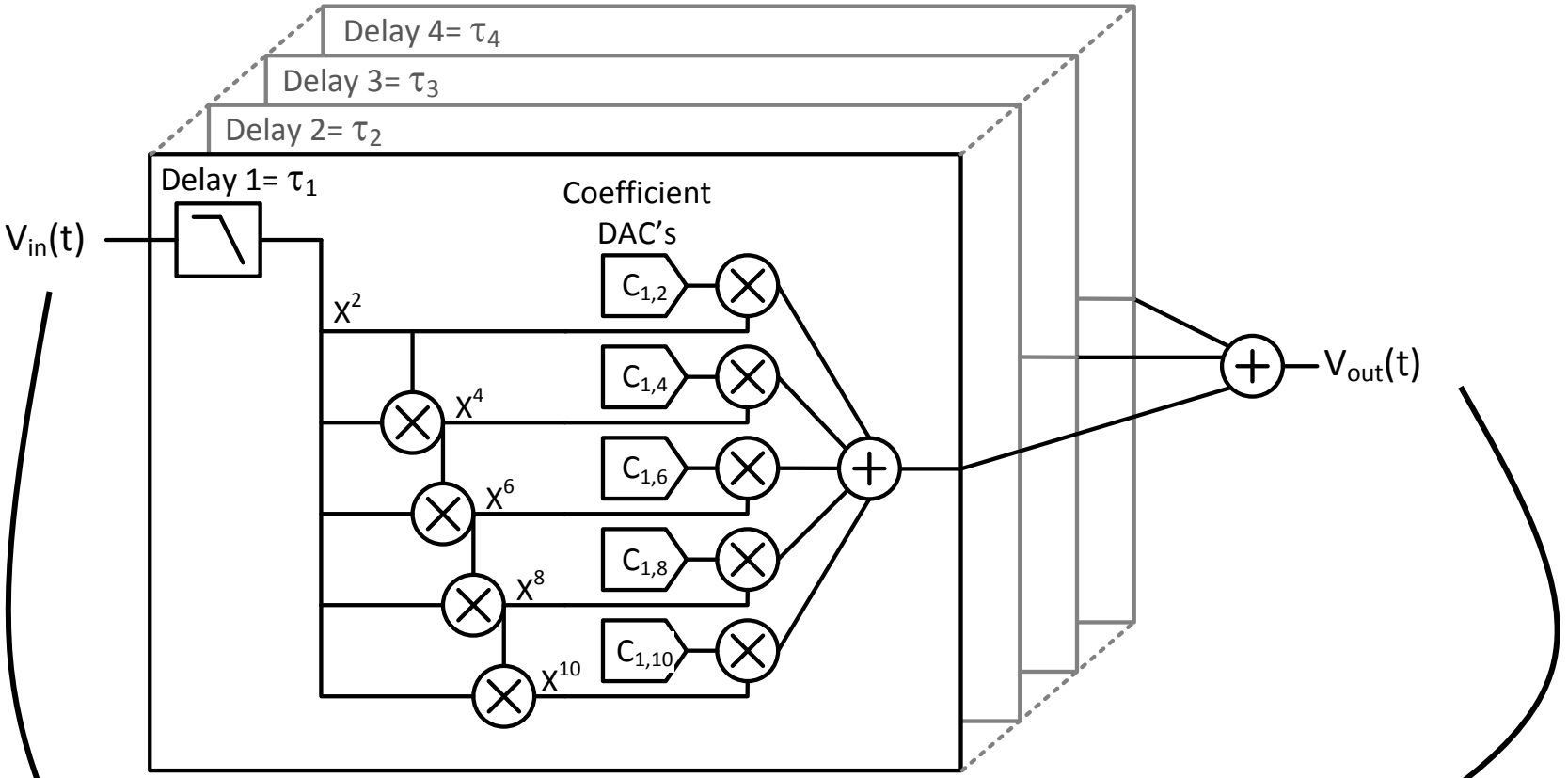
More Complete Information on Theory of Operation and Datasheets Available on Line at www.scintera.com or Richardson RFPD website

Please Visit Us at Booth # 208

Additional Slides

Analog Volterra Series



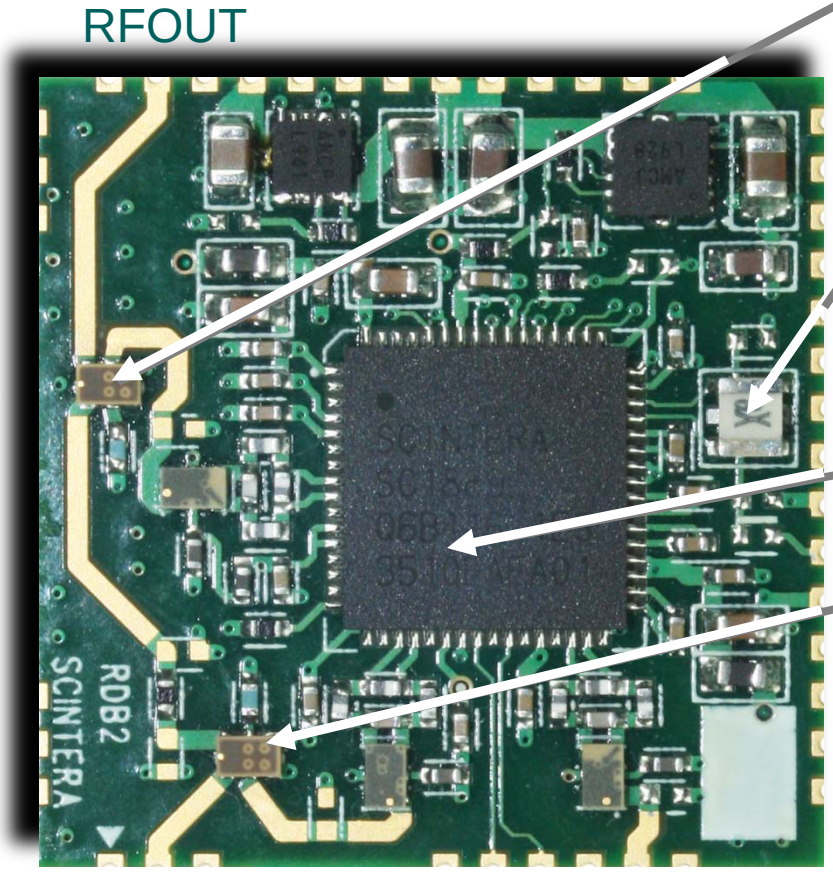
$$V_{IN}(t) = r^2(t)$$

$$V_{OUT}(t) = \sim \sum_{p=1}^{4} \sum_{m=1}^{5} c_{p,2.m} r^{2.m}(t - \tau_p)$$

RFPAL Key Architectural Attributes

- Analog (RF & BB), Digital (high & low-speed) and SW partitioning minimize power & area
  - Computation of correction terms in digital (software and hardware) domain
  - Application of correction in the analog domain
- RF and most of baseband analog circuitry is *unclocked*
  - enables robustness and flexibility for various modulation schemes & carrier frequencies.
- Flexible Work Function
  - Synthesizes wide range of PA AM/AM and AM/PM compensation and memory compensation (1ns - 300ns)
  - Enables robust adaptation (orthogonal basis terms of work function)
- Robust performance with process, voltage, aging and temperature variations
  - Extensive digital/analog compensation loops for analog cells, with process/temp sensing, calibration routines, etc.
  - Optimized calibration algorithms using a low-power, on-chip spectral estimator.
  - *Software-driven* analog circuit design that can be conveniently tuned /optimized.
- Software-driven correction enables flexibility
  - With respect to waveforms, PA, power consumption (duty-cycle), etc.
  - Allows customization of solutions by application and customer

RFPAL Reference PCB



Output coupler

Ceramic resonator

RFPAL Linearizer SoC
- 9 x 9 x 0.9 mm standard QFN package

Input coupler

Other: Decoupling + matching networks