

# Design of DC-DC Converters

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# Design of DC-DC Converters

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- DC-DC Converter Basics
  - Topology and Operation of DCDC Converters
  - Control Scheme for DCDC
- DC-DC Converter Design Techniques
  - System Level Modeling and Design
  - Building Block Design Considerations



# DC-DC Converter Basics

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- DC-DC Converter is a Voltage Regulator
  - Use Switches, Inductor and Capacitor for Power Conversion
  - Switched Mode Operation
- Why DC-DC Converters?
  - High Efficiency
  - Can Step-Down, Step-up, or Both, or Invert
  - Can Achieve Higher Output Power



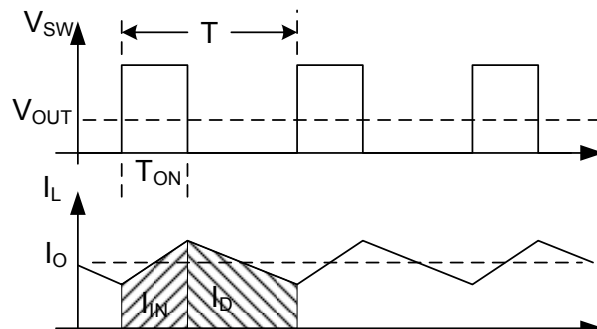
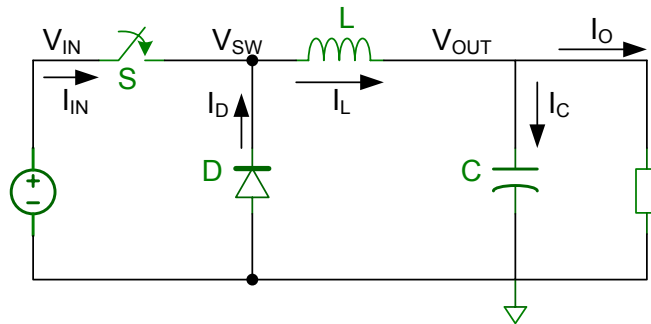
# DC-DC Converter Basics

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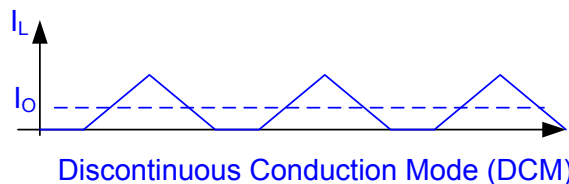
- Why not DC-DC Converters?
  - Complex Control Loop
  - Higher Noise and Output Ripple
  - More External Components
- Basic DC-DC Converter Topologies
  - Majority of DC-DC uses PWM Control Operated in CCM Mode

# DC-DC Converter Basics

## ■ Step-down (Buck)



Continuous Conduction Mode (CCM)



Discontinuous Conduction Mode (DCM)

## Basic Relationships

### ■ CCM Mode

- $I_L$  always supplies load
- $I_C$  small, independent of load

$$V_{OUT} = \frac{T_{ON}}{T} V_{IN} = D \cdot V_{IN}$$

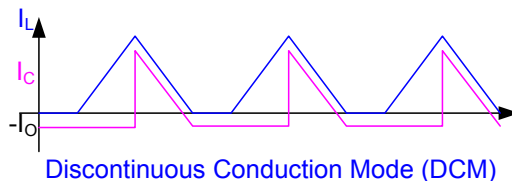
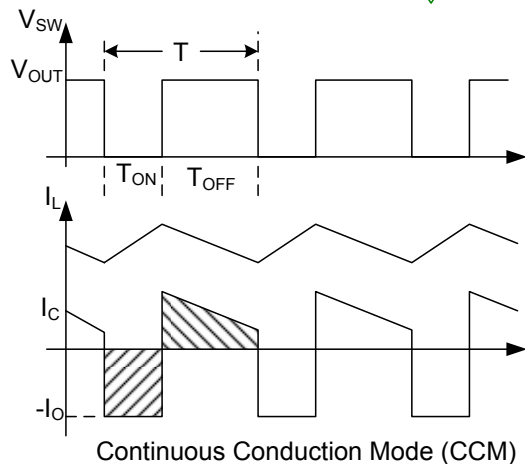
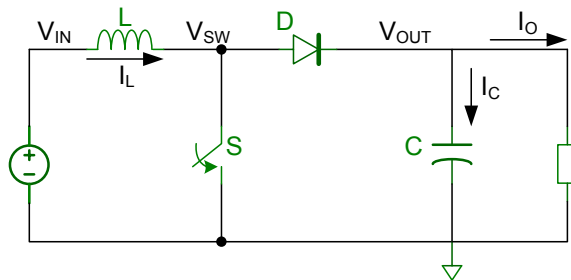
$$I_{IN} = D \cdot I_{OUT}$$

### ■ DCM Mode

$$V_{OUT} = \frac{T_{ON}^2}{T_{ON}^2 + \frac{2I_O \cdot L \cdot T}{V_{IN}}} V_{IN}$$

# DC-DC Converter Basics

## ■ Step-up (Boost)



## Basic Relationships

### ■ CCM Mode

- $I_L$  only supplies load during  $T_{OFF}$  period
- $I_C$  large and load dependent

$$V_{OUT} = \frac{T}{T_{OFF}} V_{IN} = \frac{1}{1-D} \cdot V_{IN}$$

$$I_{IN} = I_L = \frac{1}{1-D} \cdot I_{OUT}$$

### ■ DCM Mode

$$V_{OUT} = \frac{T_{ON}^2 + \frac{2I_O \cdot L \cdot T}{V_{IN}}}{T_{ON}^2} V_{IN}$$



# Common Control Architectures

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- Modulation Scheme
  - PFM (Pulse-Frequency-Modulation)
    - Pulse Skipping, Hysteretic, Constant-on etc.
    - High Efficiency at Light Load
    - Inherently Higher Output Ripple
    - Unmanaged Spectrum Noise
  - PWM (Pulse-Width-Modulation)
    - Fixed Frequency with Variable Duty Cycle
    - Better Transient Response (except Hysteretic?)
    - Most Widely Used



# Common Control Architectures

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- Control Method (for PWM)
  - Voltage Mode
    - Regulates Output Voltage by Adjusting Duty Cycle
    - Constant Ramp for Modulation, Better Noise Immunity
    - LC Filter Contributes to Complex Conjugate Poles
    - Loop Has No Information on Inductor Current
    - Slower Response to Input Voltage Change
    - Bandwidth Varies with Input Voltage
    - Current Limit Done Separately





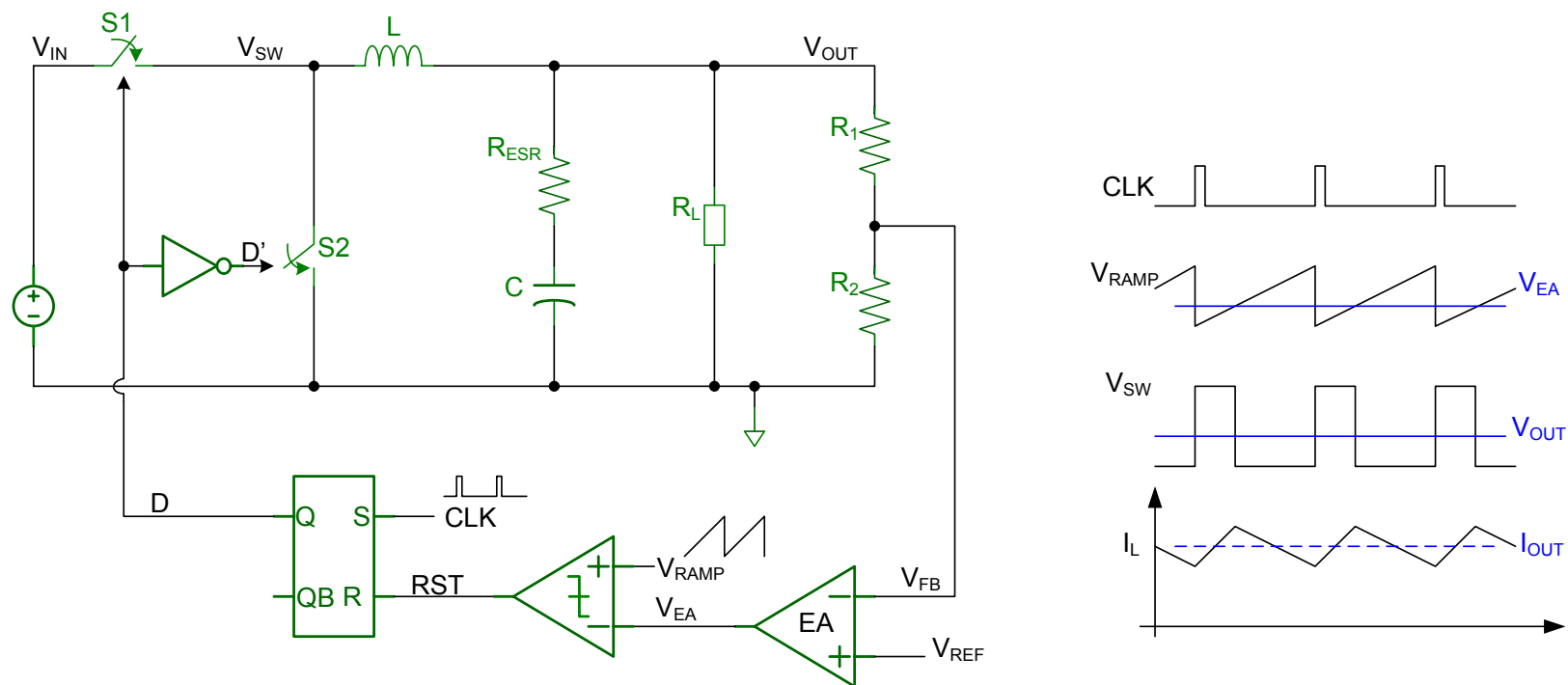
# Common Control Architectures

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- Current Mode
  - PCM (Peak-Current-Mode) Most Commonly Used
  - Regulates Inductor Current to Satisfy Load Demand and Maintain Output Voltage
  - Fast Current Loop makes Inductor to be a VCCS, eliminates Complex Conjugate Poles
  - Easy Built-in Cycle-to-Cycle Current Limit
  - Naturally Suitable for Multi-Phase Operation
  - Current Sense Susceptible to Noise
  - Need Slope Compensation for  $>50\%$  Duty Cycle Operation

# DC-DC Converter Design

- Examples of Common DC-DC Converters
  - Voltage Mode Buck





# Voltage Mode Buck

Voltage Mode Buck Transfer Functions:

$$\frac{v_O}{d} \approx V_{IN} \frac{(1 + sCR_{ESR})}{s^2LC + s\left(\frac{L}{R_L} + CR_{ESR}\right) + 1} = V_{IN} \frac{(1 + sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}, Q = \frac{1}{\frac{1}{R_L} \sqrt{\frac{L}{C}} + R_{ESR} \sqrt{\frac{C}{L}}}$$

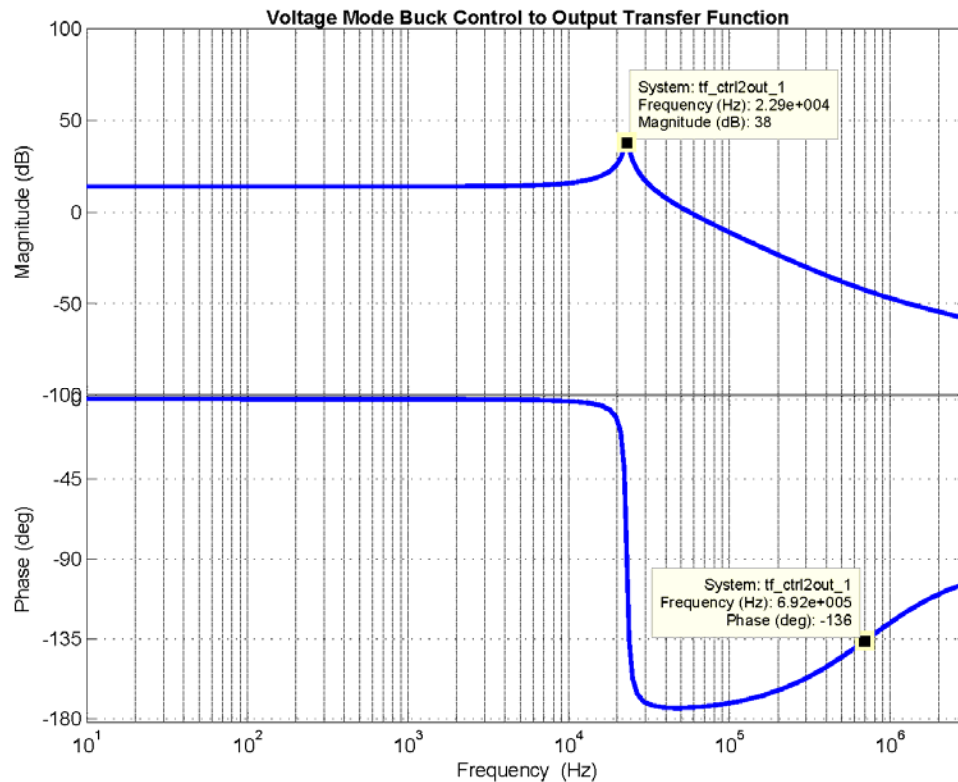
and

$$\frac{d}{v_{FB}} = \frac{1}{V_R} a(s)$$

where  $a(s)$  is the transfer function of the error amplifier

# Voltage Mode Buck

Control (Duty Cycle) to Output Transfer Function:



Example:

$L=2.2\mu\text{H}$ ,  $C=22\mu\text{F}$ ,

$R_{\text{ESR}}=10\text{m Ohm}$

$V_{\text{IN}}=5\text{V}$ ,  $V_{\text{OUT}}=3.3\text{V}$

$R_{\text{L}}=10\text{ Ohm}$

$F_{\text{SW}}=1.5\text{MHz}$

$V_{\text{RAMP}}=100\text{mV}$

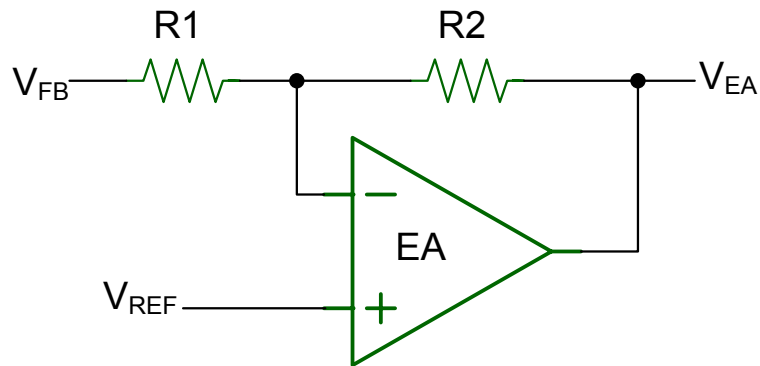
$\omega_0 = 22.9\text{kHz}$

$Q = \sim 15.8$

$\omega_z = 700\text{kHz}$

# Voltage Mode Buck - Error Amp Ex. 1

Use low DC gain to set the bandwidth so that the phase margin is acceptable:

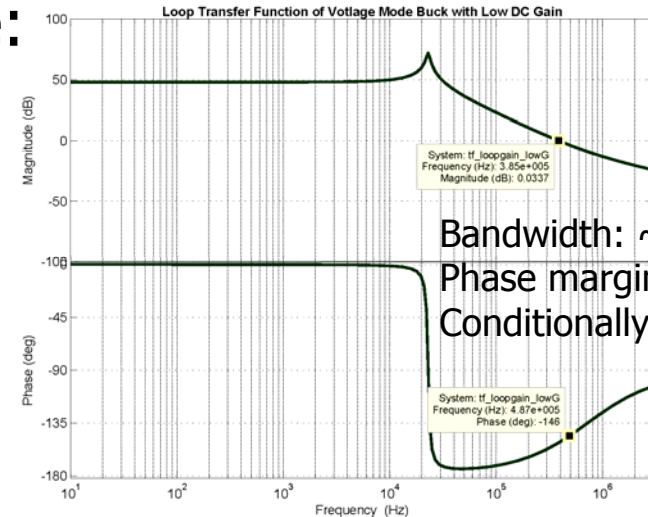


$$V_{EA} = V_{REF} + \frac{R_2}{R_1}(V_{REF} - V_{FB})$$

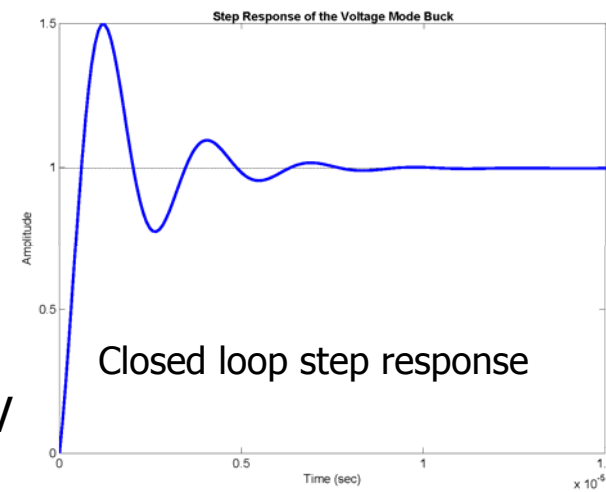
$$V_{EA} = -\frac{R_2}{R_1}V_{FB}$$

$$LG = -\frac{R_2}{R_1} \cdot \frac{V_{IN}}{V_R} \frac{(1 + sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

Example: R2=500k, R1=100k, V<sub>R</sub>=100mV



Bandwidth: ~400kHz  
Phase margin: ~35°  
Conditionally stable



Closed loop step response



# Voltage Mode Buck - Error Amp Ex. 1

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## Some Improvements Can Be Added:

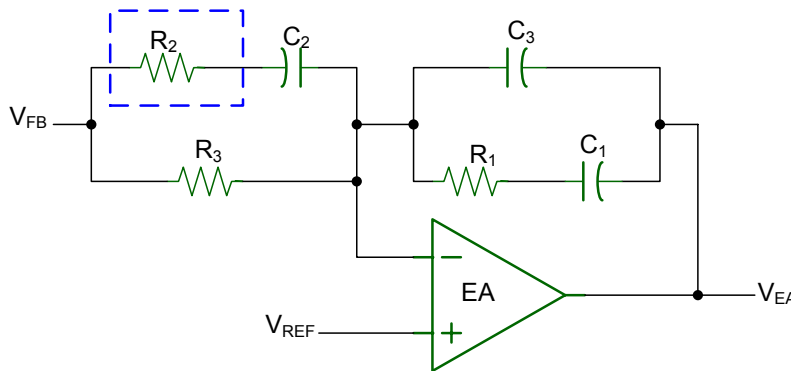
- Make  $V_{\text{RAMP}}$  proportional to  $V_{\text{IN}}$  -> Constant Bandwidth
- Add Feed-forward Cap on Feedback Resistor String -> better phase margin

## Limitations of Low DC Gain:

- Loose Output Regulation
- Need some ESR to Stabilize the Loop
- Small Modulation Ramp Sensitive to Noise
- DC Offset if Output Cap has large ESR

# Voltage Mode Buck - Error Amp Ex. 2

Use Type-III Compensation Network to Re-Shape Loop Frequency Response:



$$\frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{(1 + sC_1R_1)[1 + s(R_3 + R_2)C_2]}{[1 + sR_3(1 + A_0)(C_1 + C_3)](1 + sR_2C_2)(1 + sR_1C_3 \parallel C_1)}$$

$$LG \approx -A_0 \frac{(1 + sC_1R_1)(1 + sR_3C_2)}{[1 + sR_3A_0C_1](1 + sR_2C_2)(1 + sR_1C_3)} \cdot \frac{V_{IN}}{V_R} \frac{(1 + sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

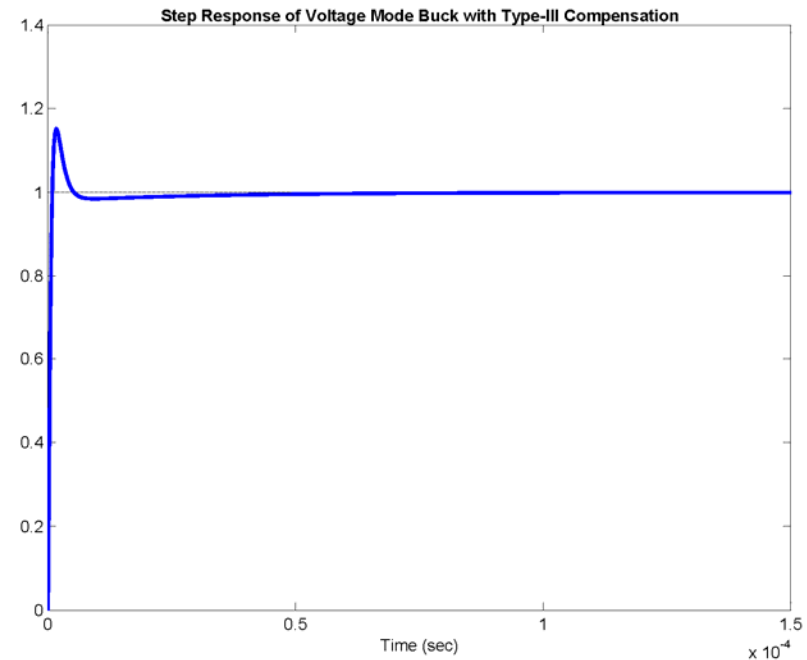
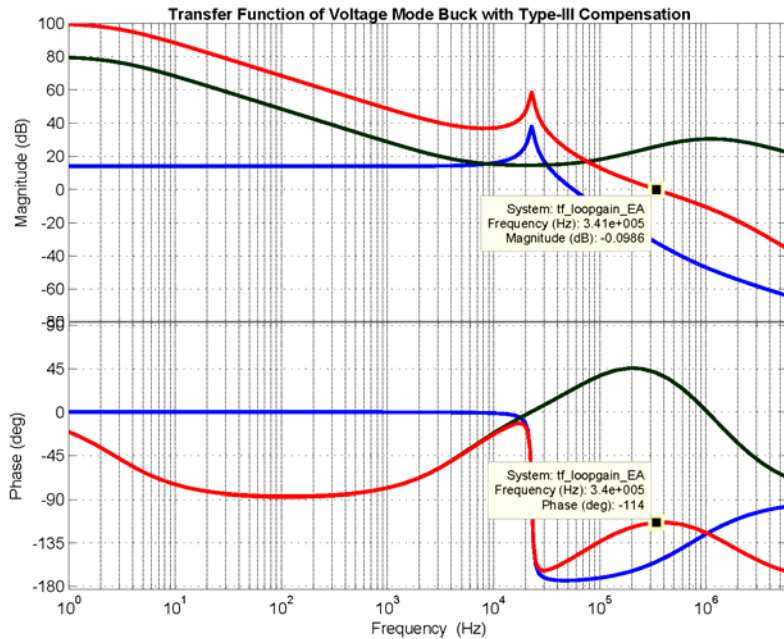
$$UGBW \approx R_1C_2 \cdot \frac{V_{IN}}{V_R} \cdot \frac{1}{LC}$$

- High DC gain rolls off by dominant pole and, phase shift recovered by 1<sup>st</sup> zero before  $\omega_0$
- 2<sup>nd</sup> zero brings back phase shift above  $\omega_0$
- 2<sup>nd</sup> and 3<sup>rd</sup> pole attenuates high frequency noise

Example Design Steps:

1. Set  $R_1C_2 = 100\mu\text{s}$  for desired BW of  $\sim 300\text{kHz}$
2. Set 1<sup>st</sup> zero to be 1/5 of  $\omega_0$ :  
 $R_1 = 1\text{Meg}$ ,  $C_1 = 30\text{pF}$ ,  
 $\omega_{z1} = 5.3\text{kHz}$
3. Set 2<sup>nd</sup> zero to be 4x of  $\omega_0$ :  $C_2 = 10\text{pF}$ ,  $R_3 = 200\text{k}$ ,  
 $\omega_{z2} = 79.5\text{kHz}$
4. mid-band DC gain of 5:  
 $R_3 = 200\text{k}$
5. Set 2<sup>nd</sup> and 3<sup>rd</sup> pole to near switching frequency for high frequency noise attenuation:  
 $C_3 = 0.2\text{pF}$ ,  $\omega_{p2} = 795\text{kHz}$ ;  
 $R_2 = 10\text{k}$ ,  $\omega_{p3} = 1.5\text{MHz}$

# Voltage Mode Buck - Error Amp Ex. 2



- Modulation ramp  $V_{RAMP}$  increased to 500mV for better noise immunity
- Blue: control to output transfer function
- Green: Type-III compensation error Amp transfer function
- Red: Complete loop transfer function bandwidth:  $\sim 340\text{kHz}$ , PM:  $\sim 65$  degree

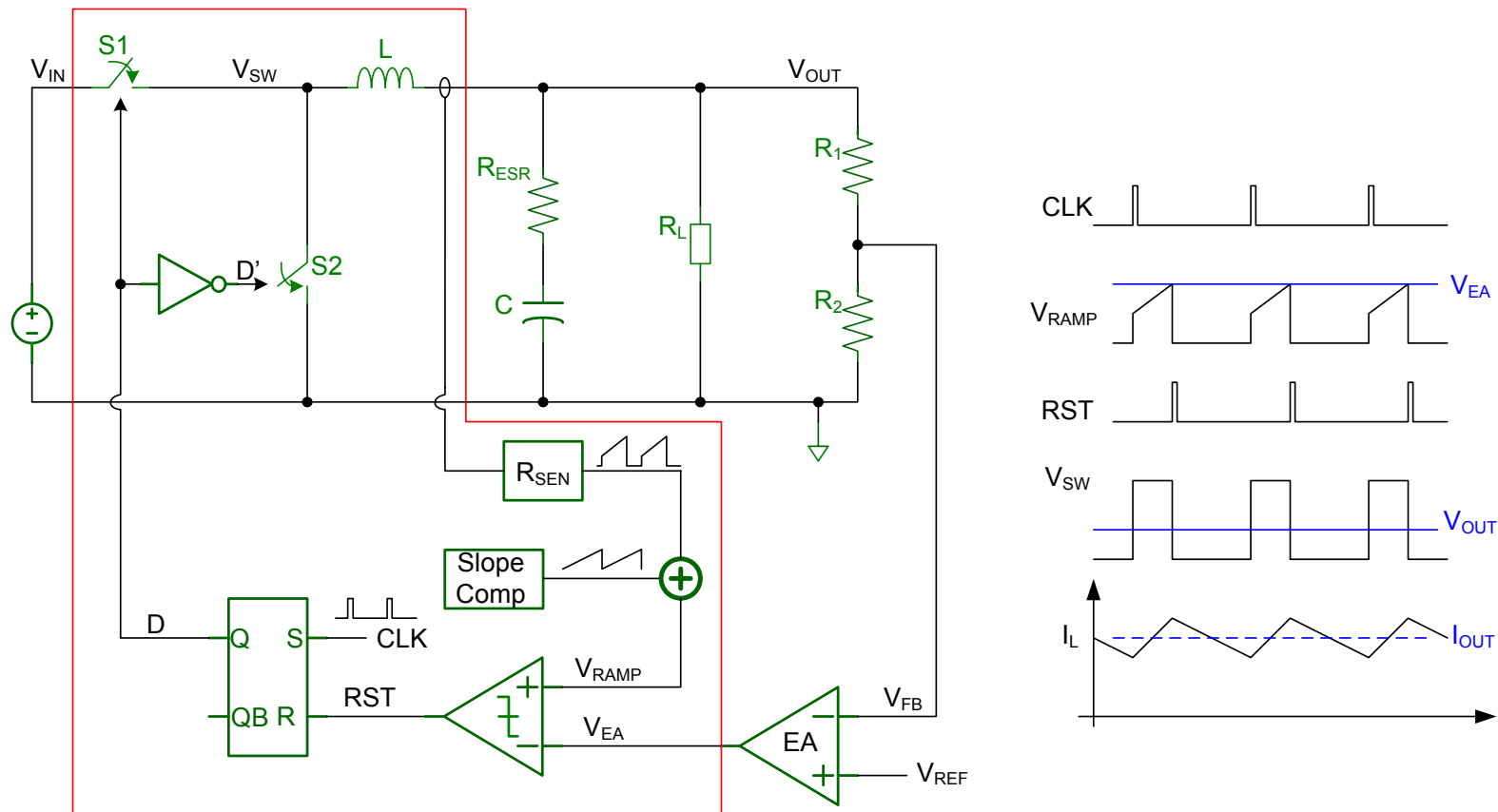
Compare to Error Amp Ex. 1:

- Step response has less overshoot due to better phase margin
- Settling is much slower due to 1<sup>st</sup> zero at low frequency



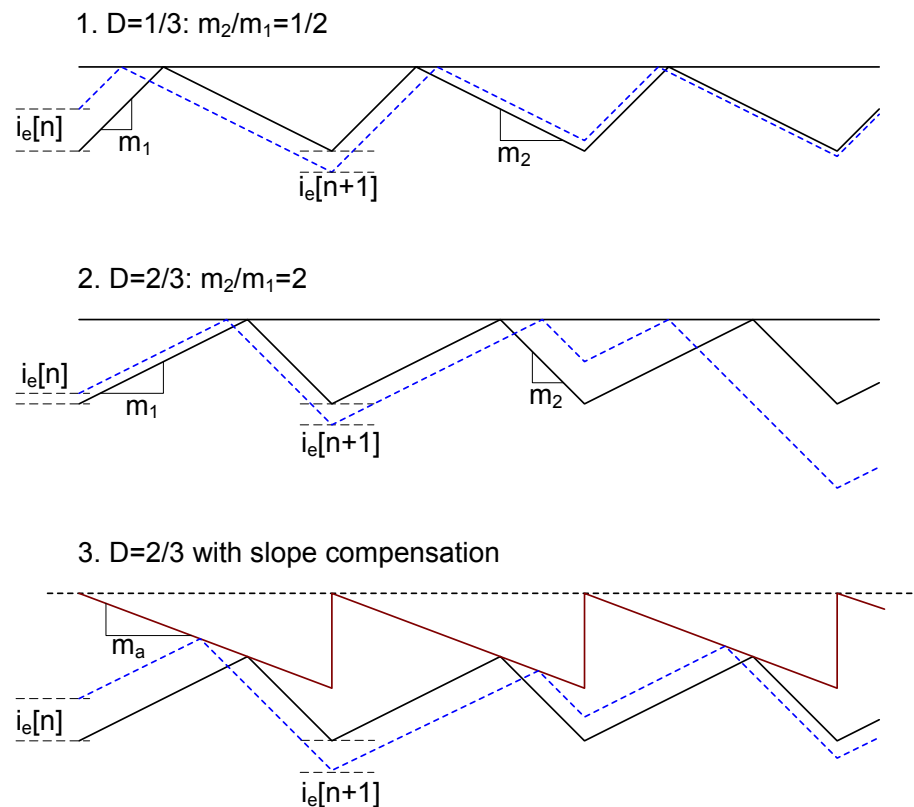
# DC-DC Converter Design

- Current Mode Buck (Peak Current Control)



# Current Mode Buck

## Inductor Current Instability for Duty Cycle > 50%:



$$i_e[n+1] = i_e[n] \cdot \left(-\frac{m_2}{m_1}\right) = i_e[0] \cdot \left(-\frac{m_2}{m_1}\right)^n$$

$$\left|\frac{m_2}{m_1}\right| < 1: i_e \text{ attenuates over cycles}$$

$$\left|\frac{m_2}{m_1}\right| > 1: i_e \text{ grows over cycles}$$

Requires Slope Compensation:

$$i_e[n+1] = i_e[n] \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a}\right)$$

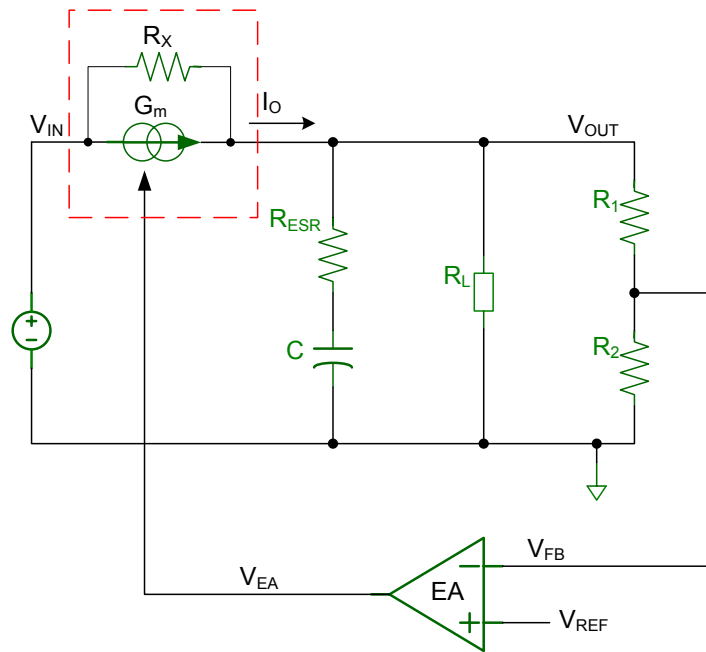
$$m_a \text{ is chosen so that } \left|\frac{m_2 - m_a}{m_1 + m_a}\right| < 1$$

$$\text{ex : } m_a = \frac{m_2}{2}, \text{ guaranteed stable}$$

$$m_a = m_2, 1 \text{ cycle correction}$$

# Current Mode Buck

- Fast current loop regulates inductor peak current, can be modeled as a VCCS with output impedance  $R_x$
- Slower voltage loop provides reference for current loop



$$G_m = \frac{i_o}{v_{EA}} = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_L T_s}{L} [(1 + \frac{m_a}{m_1})(1 - D) - 0.5]} = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_X}}$$

$$\text{where } R_X = \frac{L}{T_s [(1 + \frac{m_a}{m_1})(1 - D) - 0.5]}$$

Switched Operation results in delay and sampling effect :

$$H_e(s) = \frac{1 + \alpha}{1 + \alpha \cdot e^{-sT_s}} \frac{1 - e^{-sT_s}}{sT_s} \quad \text{where } \alpha = \frac{m_2 - m_a}{m_1 + m_a}$$

Complete VCCS transconductance including frequency response :

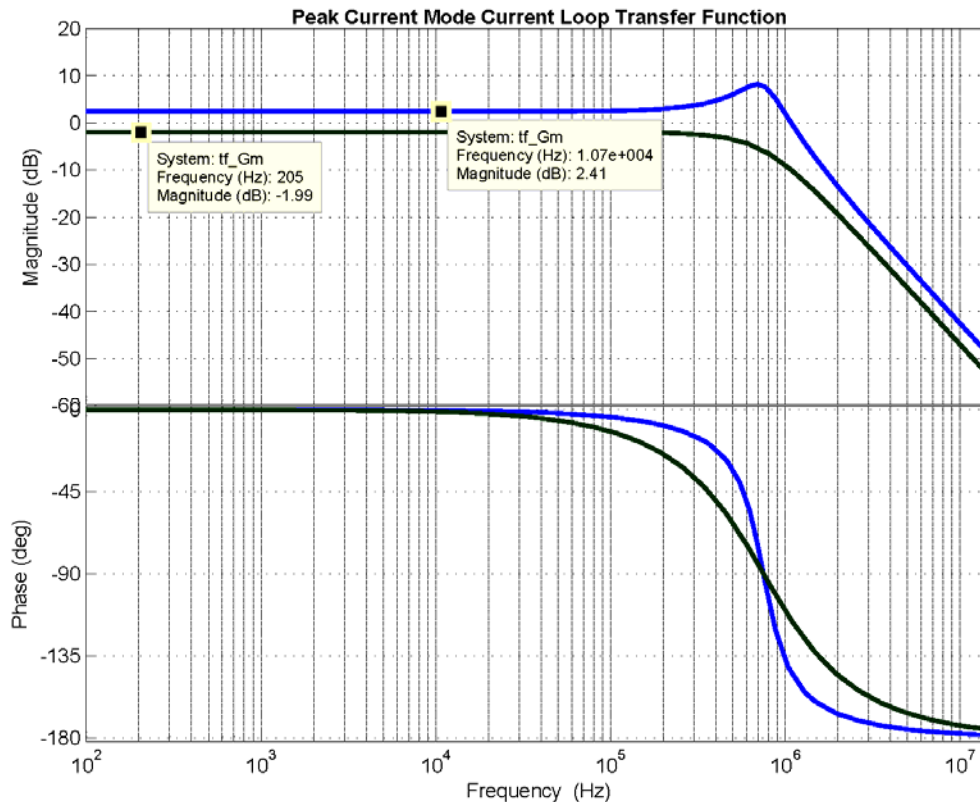
$$G_m(s) = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_L T_s}{L} [(1 + \frac{m_a}{m_1})(1 - D) - 0.5]} \frac{1 + \alpha}{1 + \alpha \cdot e^{-sT_s}} \frac{1 - e^{-sT_s}}{sT_s}$$

$$G_m(s) \approx \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_X}} \frac{1}{1 + \frac{s}{Q\omega_s} + \frac{s^2}{\omega_s^2}}$$

$$Q = \frac{2}{\pi} \frac{1}{(1 + \frac{m_a}{m_1})(1 - D) - 0.5} = \frac{2}{\pi} \frac{1}{1 - 2D(1 - \frac{m_a}{m_2})}$$

# Current Mode Buck

## Peak Current Mode Current Loop Transfer Function



Example:

$L=2.2\mu\text{H}$ ,  $V_{\text{IN}}=5\text{V}$ ,  
 $V_{\text{OUT}}=3.3\text{V}$ ,  $R_{\text{L}}=10\text{ Ohm}$   
 $R_{\text{SEN}}=0.5\text{ Ohm}$   
 $F_{\text{SW}}=1.5\text{MHz}$

Blue:  $m_a=0.5*m_2$   
 $R_x=19.4\text{ Ohm}$   
 $G_m=1.32\text{ A/V}$   
 $Q=1.87$

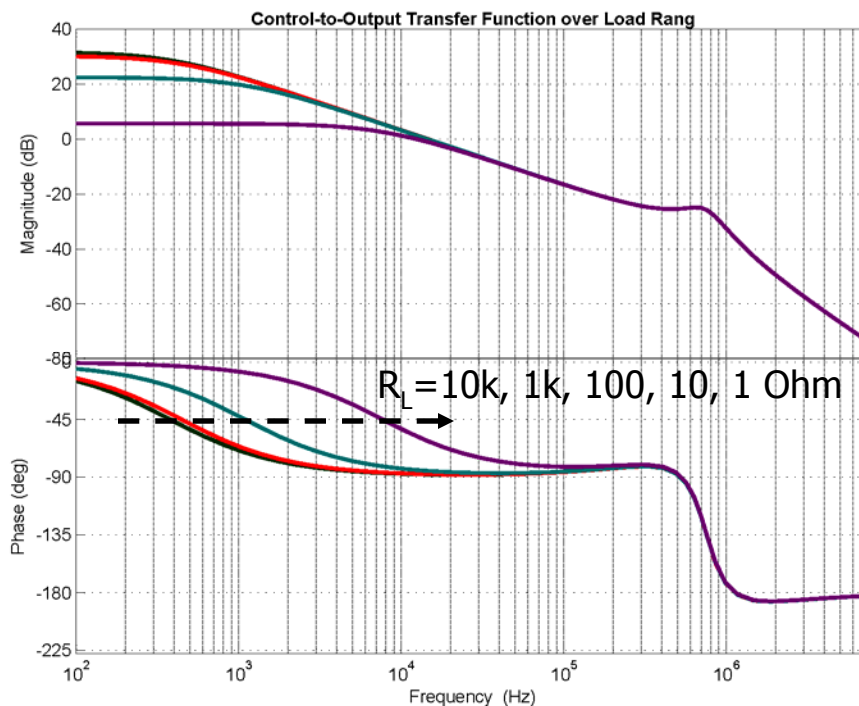
Green:  $m_a=m_2$   
 $R_x=6.6\text{ Ohm}$   
 $G_m=0.80\text{ A/V}$   
 $Q=0.64$

# Current Mode Buck

## Control to Output Transfer Function

## Equivalently Single-Pole System with Current Source Input

$$\frac{v_o}{v_{EA}} = G_m \cdot Z_o = \frac{R_L}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_X}} \frac{1}{1 + \frac{s}{Q\omega_S} + \left(\frac{s}{\omega_S}\right)^2} \frac{1 + sCR_{ESR}}{[1 + sC(R_L \parallel R_X)]}$$



Example:

$C = 22\mu\text{F}$ ,  $R_{ESR} = 10\text{m Ohm}$

$R_{SEN} = 0.5 \text{ Ohm}$

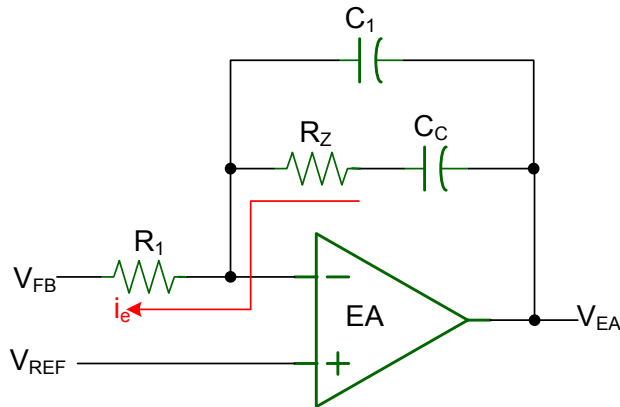
$F_{SW} = 1.5\text{MHz}$

$R_X = 19.4 \text{ Ohm}$

$R_L = 10k, 1k, 100, 10, 1 \text{ Ohm}$

# Current Mode Buck – Error Amp

## Error Amplifier Example:



- Bandwidth defined by  $R_1$  and  $C_1$
- Much smaller  $C_C$ , need large  $R_Z$
- VFB more error during transient

Example:

$$g_m = 100\mu\text{S}, r_o = 10\text{M}\Omega,$$

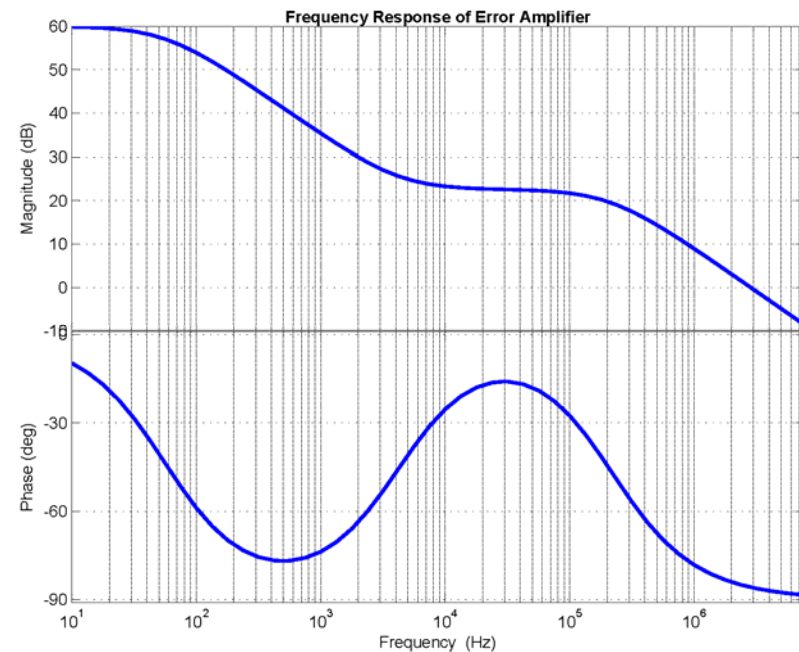
$$R_1 = 100\text{k}\Omega, C_C = 25\text{pF},$$

$$R_Z = 1.5\text{M}\Omega, C_1 = 0.3\text{pF}$$

$$a(s) = \frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{1 + sC_C R_Z}{[1 + sC_C(r_o + g_m R_1 r_o + R_Z)](1 + sC_1 R_Z)}$$

$$(C_C \gg C_1)$$

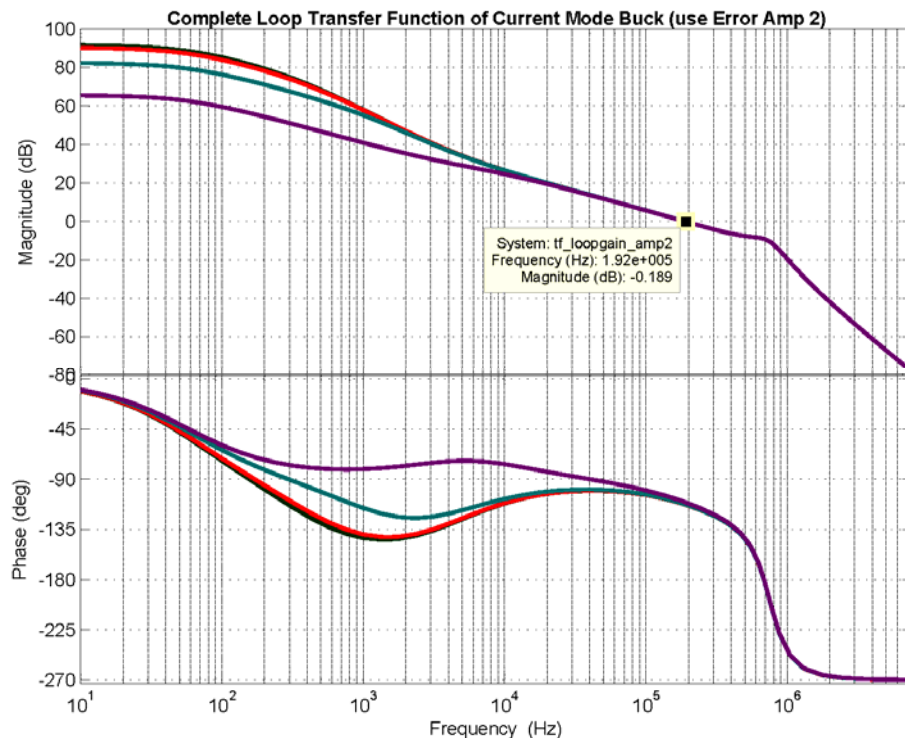
where:  $g_m$  is the transconductance of the error amp  
 $r_o$  is the output impedance



# Current Mode Buck – Error Amp

Complete Loop Transfer Function of Current Mode Buck:

$$LG = -\frac{R_L}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_X}} \frac{1}{1 + \frac{s}{Q\omega_s} + \left(\frac{s}{\omega_s}\right)^2} \cdot \frac{1 + sCR_{ESR}}{[1 + sC(R_L \parallel R_X)]} \cdot A_0 \frac{1 + sC_C R_Z}{[1 + sC_C(r_o + g_m r_o R_1 + R_Z)](1 + sC_1 R_Z)}$$



- 1<sup>st</sup> zero of error amp placed near output filter pole
- ESR zero and 2<sup>nd</sup> pole of error amp are placed out of loop bandwidth

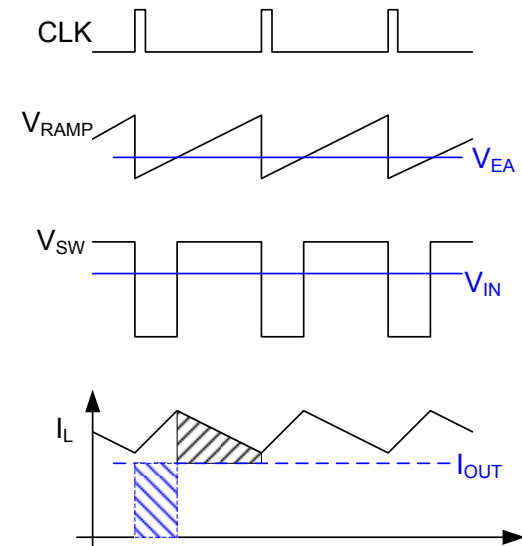
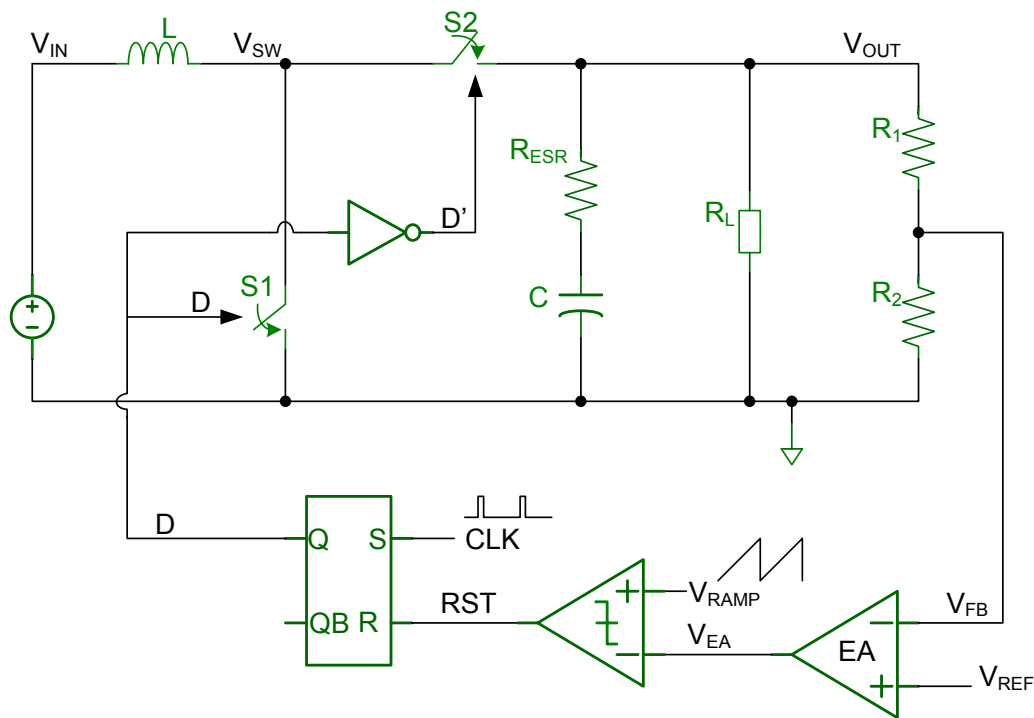
$BW$  obtained by setting  $|LG| = 1$ :

$$|LG(s_{BW})| \approx \frac{1}{R_{SEN}} \cdot \frac{1}{s_{BW} C} \cdot \frac{R_Z}{R_1} = 1$$

$$BW = \frac{1}{2\pi} \frac{R_Z}{R_1} \frac{1}{R_{SEN} C}$$

# DC-DC Converter Design

## ■ Voltage Mode Boost







# Voltage Mode Boost

## Voltage Mode Boost Transfer Functions:

$$\frac{v_O}{d} \approx \frac{V_{IN}}{(1-D)^2} \frac{(1 + sCR_{ESR})(1 - s\frac{L}{R_L(1-D)^2})}{s^2 \frac{LC}{(1-D)^2} + s(\frac{L}{R_L(1-D)^2} + CR_{ESR}) + 1} = \frac{V_{IN}}{(1-D)^2} \frac{(1 + \frac{s}{\omega_Z})(1 - \frac{s}{\omega_{RHP}})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

$$\omega_0 = \frac{(1-D)}{\sqrt{LC}}, \quad \omega_{RHP} = \frac{R_L(1-D)^2}{L}, \quad Q = \frac{1}{\frac{1}{(1-D)R_L} \sqrt{\frac{L}{C}} + (1-D)R_{ESR} \sqrt{\frac{C}{L}}}$$

and

$$\frac{d}{v_{FB}} = \frac{1}{V_R} a(s)$$

where  $a(s)$  is the transfer function of the error amplifier



## Voltage Mode Boost - Effective Inductance

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Perturbation from Output to Inductor Current:

$$L \frac{di_L}{dt} = V_{IN} - (1-D)V_o \Rightarrow i_L = \frac{(1-D)v_o}{sL}$$

and

$$I_o = \bar{I}_L(1-D) \Rightarrow i_o = i_L(1-D)$$

Impedance looking into the Inductor from Output:

$$Z_o = \frac{v_o}{i_o} = \frac{sL}{(1-D)^2}$$

Thus the Effective Inductance  $L_{eff} = \frac{L}{(1-D)^2}$

This makes the  $\omega_0$  of the LC Filter to Move with D



# Voltage Mode Boost - RHP Zero

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Perturbation from Duty Cycle to Output Current:

$$I_o = \bar{I}_L(1-D) \Rightarrow i_o = i_L(1-D) - d \cdot \bar{I}_L = i_L(1-D) - d \cdot \frac{I_o}{1-D}$$

$$L \frac{di_L}{dt} = DV_{IN} + (1-D)(V_{IN} - V_o) \Rightarrow i_L \approx \frac{d \cdot V_o}{sL}$$

Right-Half-Plan Zero forms at frequency where:

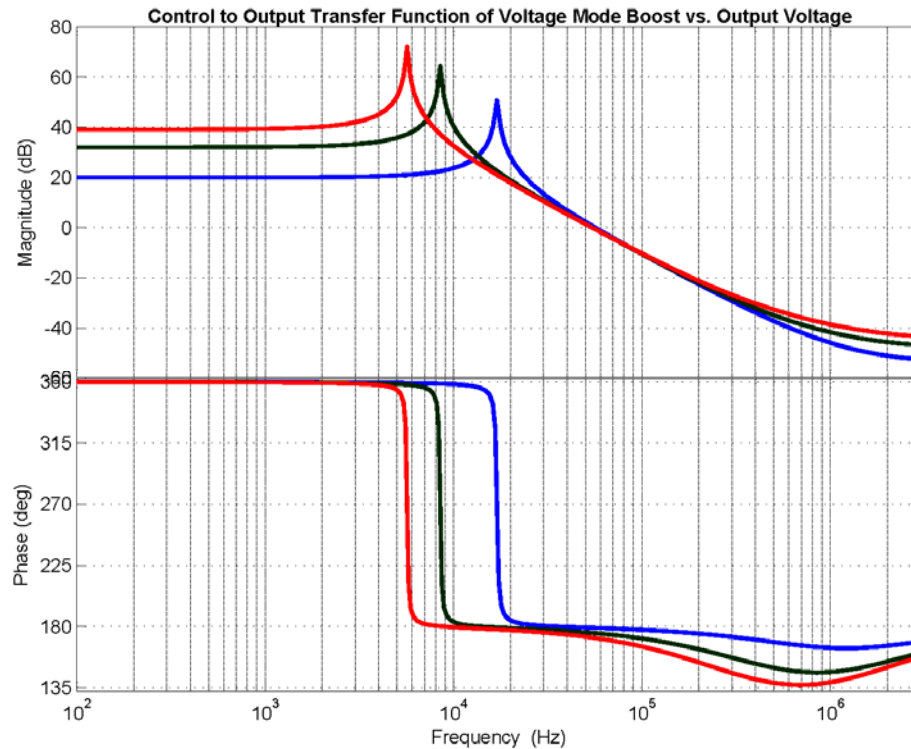
$$\left| \frac{d \cdot V_o}{j\omega_{RHP} L} (1-D) \right| = \left| d \cdot \frac{I_o}{1-D} \right|$$

$$\omega_{RHP} = \frac{R_L(1-D)^2}{L}$$

Right-Half-Plan Zero exists for both Voltage Mode and Current Mode Boost

# Voltage Mode Boost

Control (Duty Cycle) to Output Transfer Function:



Example:

$L=2.2\mu\text{H}$ ,  $C=10\mu\text{F}$ ,

$R_{\text{ESR}}=10\text{m Ohm}$ ,

$V_{\text{IN}}=2.5\text{V}$ ,

$V_{\text{OUT}}=5\text{V}, 10\text{V}, 15\text{V}$ ,

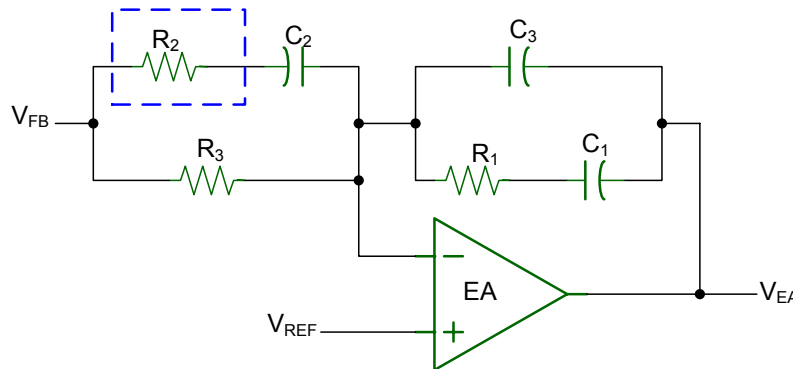
$I_{\text{OUT}}=100\text{mA}$

$F_{\text{SW}}=1.5\text{MHz}$

$\omega_0$  and  $\omega_{\text{RHP}}$  moves  
lower with increased  
duty cycle

# Voltage Mode Boost – Type-III Error Amp

Usually Type-III Compensation Network is Required:



$$\frac{v_{EA}}{v_{FB}} \approx -A_0 \frac{(1 + sC_1R_1)[1 + s(R_3 + R_2)C_2]}{[1 + sR_3(1 + A_0)(C_1 + C_3)](1 + sR_2C_2)(1 + sR_1C_3 \parallel C_1)}$$

$$LG \approx -A_0 \frac{(1 + sC_1R_1)(1 + sR_3C_2)}{[1 + sR_3A_0C_1](1 + sR_2C_2)(1 + sR_1C_3)} \cdot \frac{V_{IN}}{V_R(1 - D)^2} \frac{(1 + \frac{s}{\omega_Z})(1 - \frac{s}{\omega_{RHP}})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

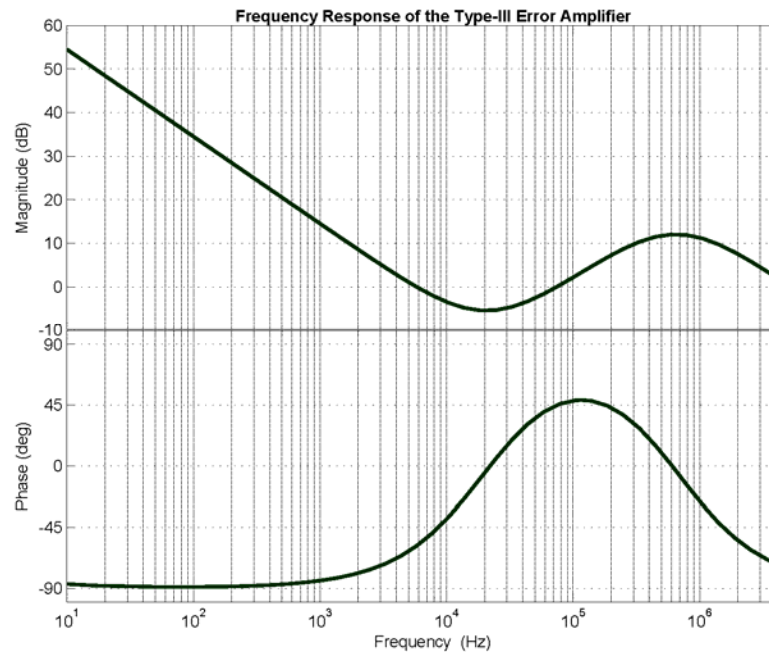
Set BW to be lower than  $\omega_Z$  and  $\omega_{RHP}$  :

$$BW : R_1 \cdot C_2 \cdot \frac{V_{IN}}{V_R} \cdot \frac{1}{s_{BW}LC} = 1 \Rightarrow BW = \frac{1}{2\pi} \frac{R_1 \cdot C_2 \cdot \frac{V_{IN}}{V_R}}{LC}$$

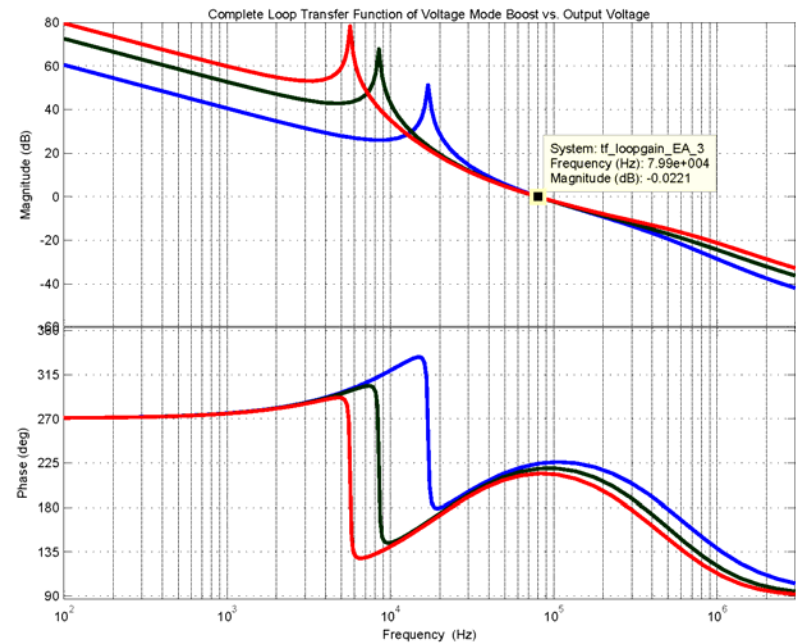
Example Design Steps:

1. Estimate worst case  
 $\omega_{RHP} = 300\text{kHz}$
2. Set  $BW < 100\text{k}$ :  
 $R_1 C_2 < 2.75\mu\text{s}$
3. Set both zeros near  $\omega_0$ :  
 $R_1 = 100\text{k}$ ,  $C_1 = 100\text{pF}$ ,  
 $R_3 = 300\text{k}$ ,  $C_2 = 20\text{pF}$ ,  
 $\omega_{z1} = 16.0\text{kHz}$ ,  $\omega_{z2} = 26.5\text{kHz}$
4. Bandwidth:  $f_{BW} = 80\text{kHz}$
5. Mid-band DC gain of 1/3
6. Set 2<sup>nd</sup> and 3<sup>rd</sup> pole to beyond  $\omega_{RHP}$  :  
 $R_2 = 10\text{k}$ ,  $C_3 = 3\text{pF}$   
 $\omega_{p2} = 530\text{kHz}$ ,  $\omega_{p3} = 790\text{kHz}$

# Voltage Mode Boost – Type-III Error Amp



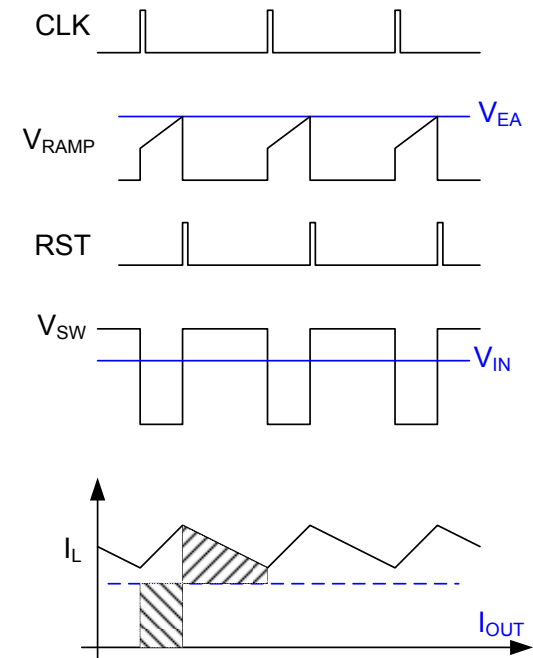
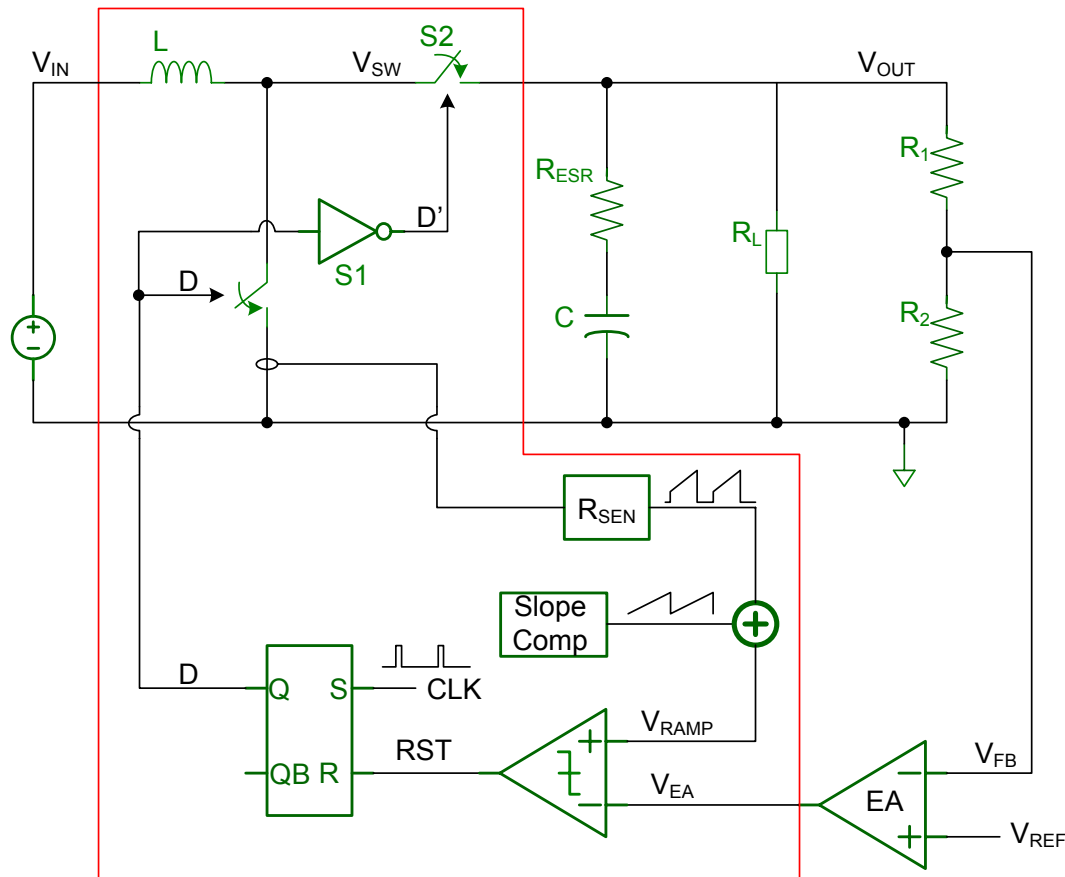
- Adjust  $C_1$  to move 1<sup>st</sup> zero
- Adjust  $R_3$  to move 2<sup>nd</sup> zero and mid-band gain
- 2<sup>nd</sup> pole and 3<sup>rd</sup> poles suppress high frequency noise



- Phase shift exceeds 180° at  $\omega_0$  -> conditionally stable
- Move 1<sup>st</sup> zero lower to improve phase shift -> much larger  $C_1$

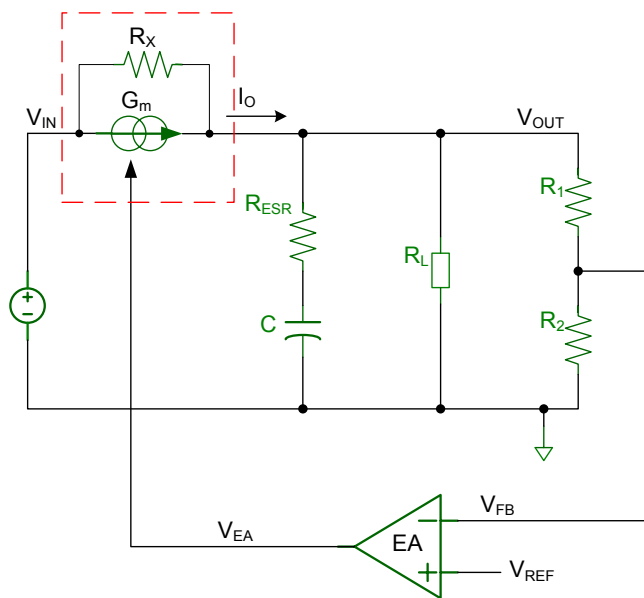
# DC-DC Converter Design

## ■ Current Mode Boost



# Current Mode Boost

Transfer Function of the Current Loop:



$$G_m = \frac{i_o}{v_{EA}} = \frac{1-D}{R_{SEN}} \frac{1}{1 + \frac{R_L}{2R_X}}$$

$$\text{where } R_X = \frac{1}{(1-D)^2} \left( \frac{L}{T_s [(1 + \frac{m_a}{m_1})(1-D) - 0.5]} \parallel \frac{2L}{DT_s} \right)$$

Similar to Peak Current Mode Buck

Delay and sampling effect results in a 2 - pole system :

$$G_m(s) \approx \frac{1-D}{R_{SEN}} \frac{1}{1 + \frac{R_L}{2R_X}} \frac{1}{1 + \frac{s}{Q\omega_s} + \frac{s^2}{\omega_s^2}}$$

$$\omega_s = \frac{\pi}{T_s}$$

$$Q = \frac{2}{\pi} \frac{1}{(1 + \frac{m_a}{m_1})(1-D) - 0.5} = \frac{2}{\pi} \frac{1}{1 - 2D(1 - \frac{m_a}{m_2})}$$



# Current Mode Boost

Control to Output Transfer Function:

$$\frac{v_o}{v_{EA}} = G_m(s) \cdot Z_O = \frac{(1-D)R_L}{2R_{SEN}} \cdot \frac{1}{1 + \frac{R_L}{2R_X}} \cdot \frac{1}{1 + \frac{s}{Q\omega_s} + \left(\frac{s}{\omega_s}\right)^2} \cdot \frac{(1 + sCR_{ESR})\left(1 - \frac{s}{\omega_{ZRHP}}\right)}{[1 + sC\left(\frac{R_L}{2} \parallel R_X\right)]}$$

$$\omega_{RHP} = \frac{R_L(1-D)^2}{L}$$

Example:

$$V_{IN} = 2.5V$$

$$V_{OUT} = 5V, 10V, 15V, 20V$$

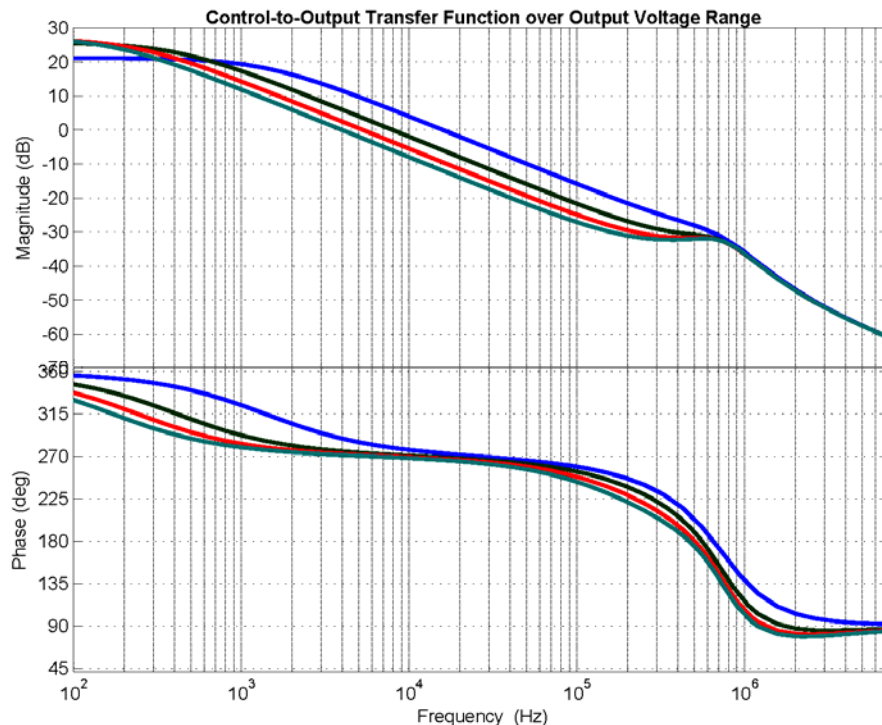
$$L = 2.2\mu H, C = 10\mu F$$

$$R_{ESR} = 10m \text{ Ohm}$$

$$I_{OUT} = 100mA$$

$$R_{SEN} = 0.5 \text{ Ohm}$$

$$F_{SW} = 1.5MHz$$

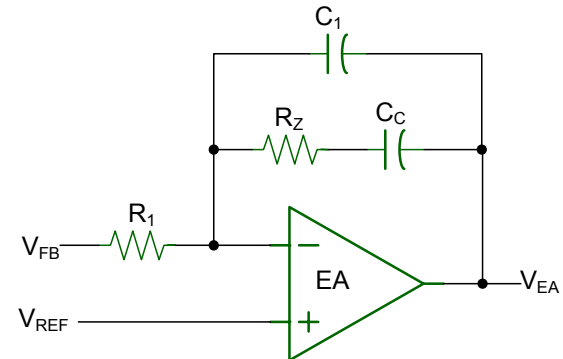


# Current Mode Boost – Error Amp Ex.

Use the same error amp structure as on page 22:

The Complete Loop Transfer Function:

$$T(s) = -\frac{(1-D)R_L}{2R_{SEN}} \frac{1}{1 + \frac{R_L}{2R_X}} \frac{1}{1 + \frac{s}{Q\omega_s} + \left(\frac{s}{\omega_s}\right)^2} \cdot \frac{(1 + sCR_{ESR})(1 - s\frac{s}{\omega_{ZRHP}})}{[1 + sC(\frac{R_L}{2} \parallel R_X)]} \cdot A_0 \frac{1 + sC_C R_Z}{[1 + sC_C(r_o + g_m r_o R_1 + R_Z)](1 + sC_1 R_Z)}$$



Generally Guideline:

- To ensure loop stability, the unity-gain bandwidth is set to be 3-5x lower than the worst case RHP zero
- The ESR zero and 2<sup>nd</sup> pole of the amplifier is placed higher than the RHP zero
- The current loop poles are usually much higher than RHP zero



# Current Mode Boost – Error Amp Ex.

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Loop Bandwidth can be estimated as:

$$BW = \frac{1}{2\pi} \frac{(1-D)}{R_{SEN}C} \cdot \frac{R_Z}{R_1} \leq \frac{\omega_{RHP}}{3} \quad (\text{RHP zero contributes } < 18^\circ \text{ phase shift})$$

$$\text{Since } \omega_{RHP} \propto R_L(1-D)^2 = R_L \left(\frac{V_{IN}}{V_O}\right)^2 = \frac{V_{IN}^2}{V_O \cdot I_O}, \quad BW \propto (1-D)$$

Bandwidth should be set at max. duty cycle and load

Example:

$$V_{IN}=2.5V, V_{OUT}=5V, I_O=500mA$$

$$L=2.2\mu H, C=10\mu F,$$

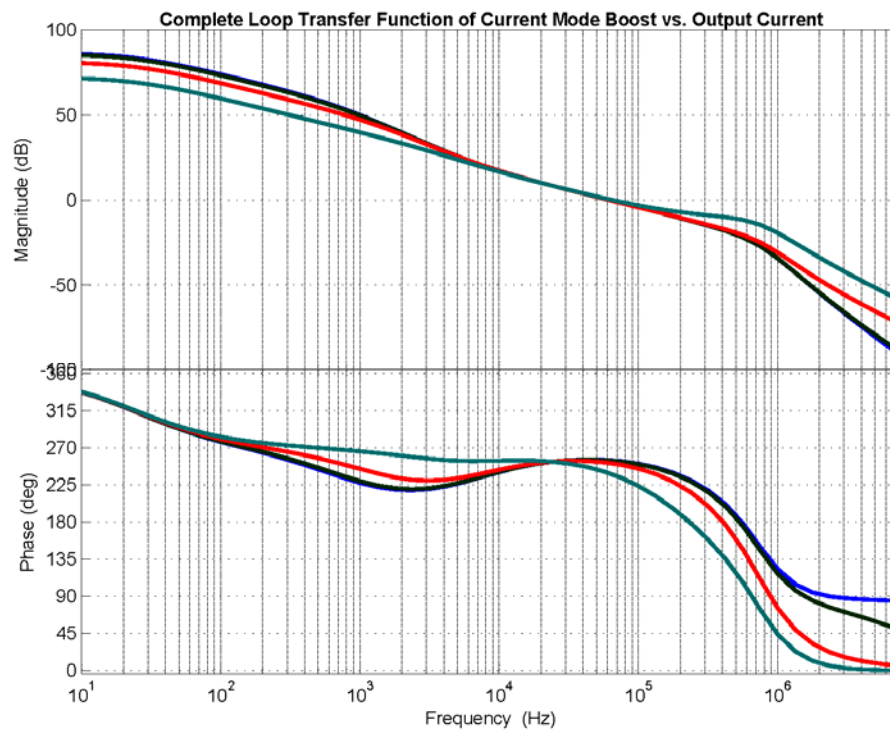
$$R_{SEN}=0.5 \text{ Ohm}, R_Z=1M \text{ Ohm},$$

$$\omega_{ZRHP}=181kHz, BW \text{ chosen to be } \sim 60kHz$$

$$\text{Calculate: } R_1: \sim 300k \text{ Ohm}$$

# Current Mode Boost

Complete Loop Transfer Function of Current Mode Boost Converter:



Error Amplifier Example:

$R_1=250k$ ,  $R_2=1M$

$C_C=25pF$ ,  $C_1=0.3pF$

Output Current:

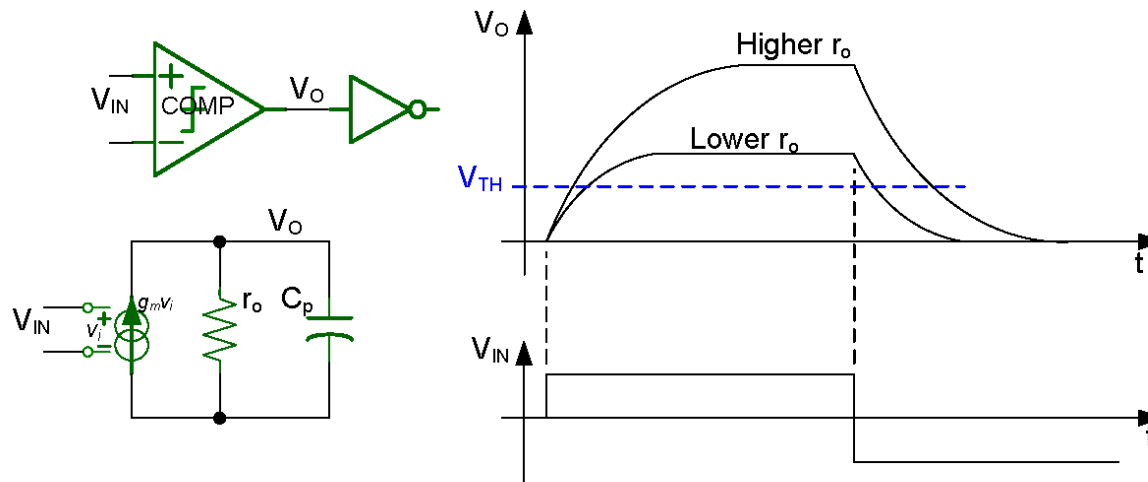
1mA, 10mA, 100mA, 500mA

Loop BW:  $\sim 60kHz$

# DC-DC Converter – Building Blocks

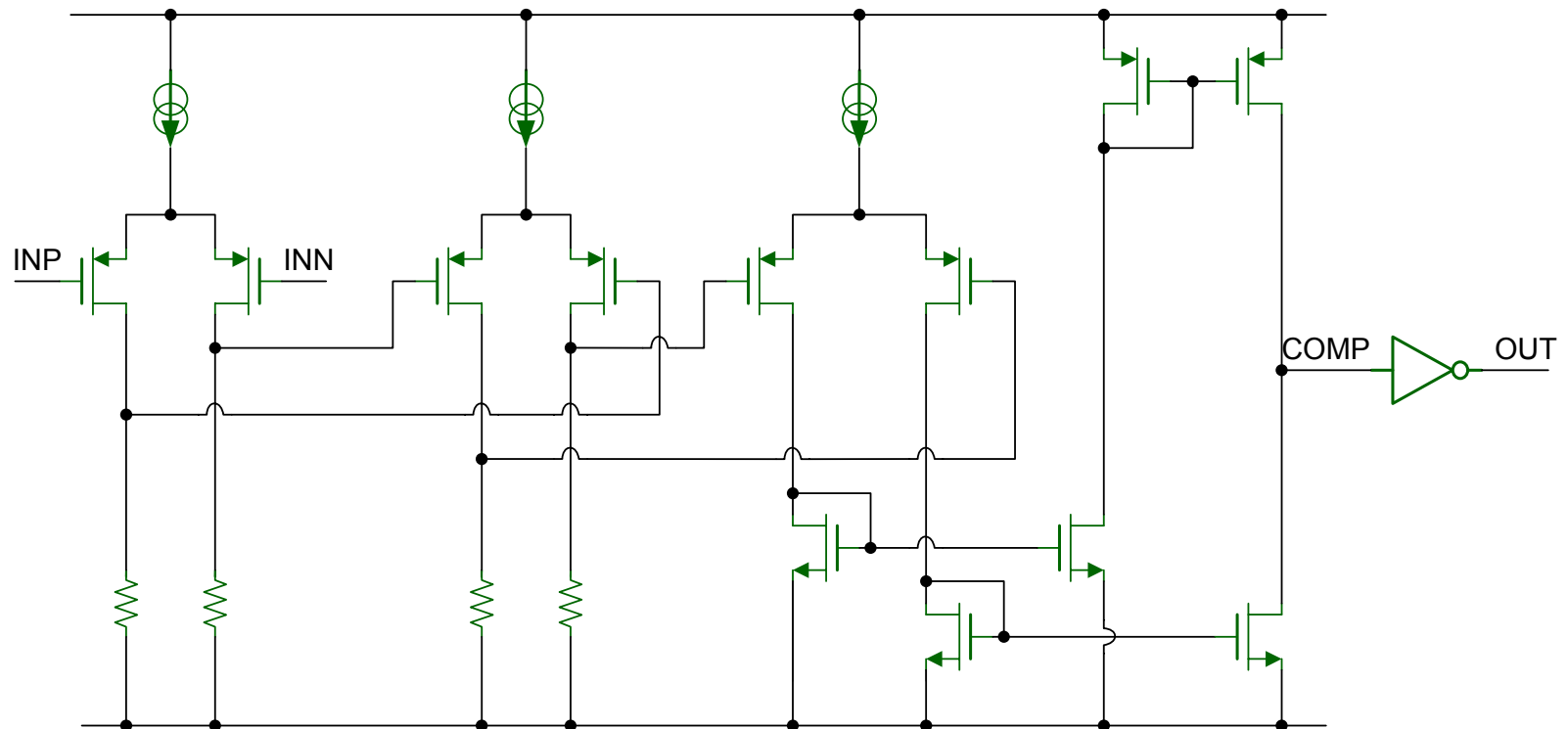
## ■ PWM Comparator

- Multi-Stage Gain -> Faster For Small Input Signal
- But, High-Gain Stage Has Longer Recovery Time
- So, Usually Low-Gain Amp(s) Followed by High-Gain Comparator



# Building Blocks – PWM Comparator

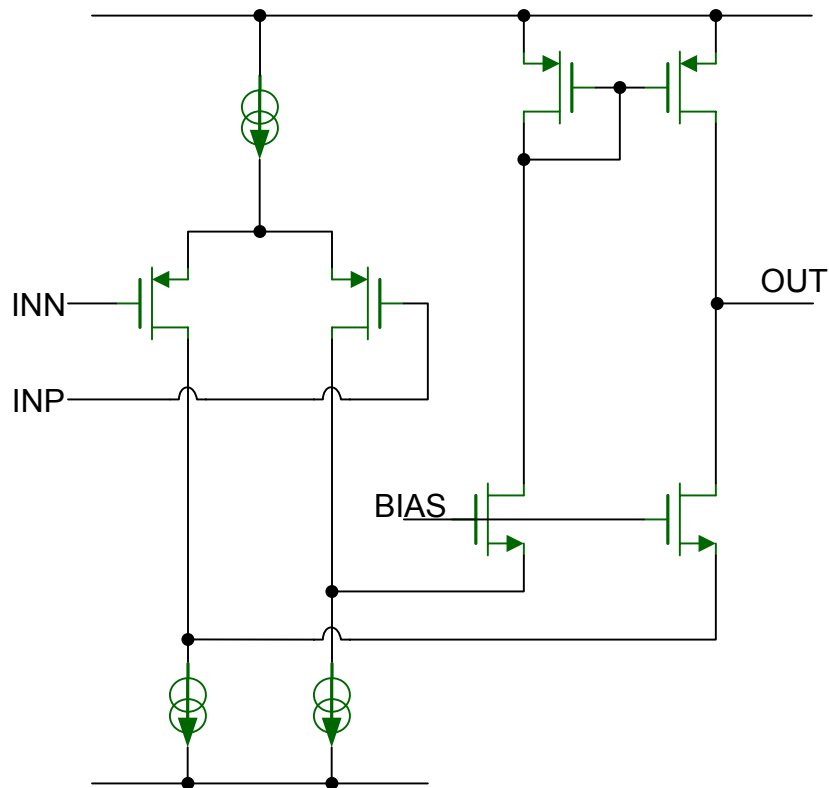
OTA based comparator with pre-amps



# Building Blocks – Error Amplifiers

## ■ Error Amplifiers

### ■ Folded-Cascode Error Amplifier



Good:

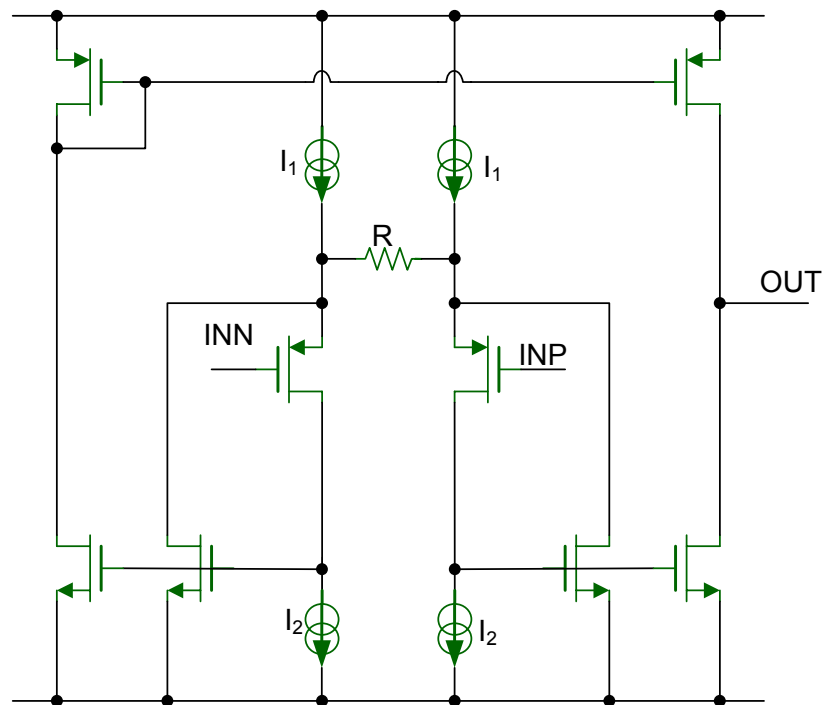
- Input Common Mode Down to Ground
- Smaller Input Offset than OTA

But:

- Difficult to get large  $G_m$

# Building Blocks – Error Amplifiers

## ■ Constant Gm Error Amplifier



Good:

- Constant Gm Defined by R
- Scalable Gm by Current Mirrors

But:

- Higher Input Offset due to Even More Current Mirrors
- Additional Gm Regulation Loop





# DC-DC Converter Design

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Acknowledgement:

Jian Zhou etc. for Review and Suggestions

Thank You For Your Attendance