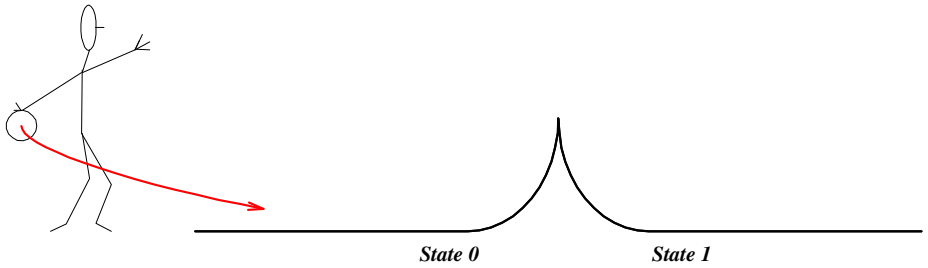
Metastability/Overview

- data storage elements: Flip-flops (FFs) and latches (D-FF, JK-FF, T-FF…)
- timing requirements of clocked flip-flops
- observation of metastability
- model of flip-flop/latch behaviour
- metastability analysis and characterisation
- synchronisers



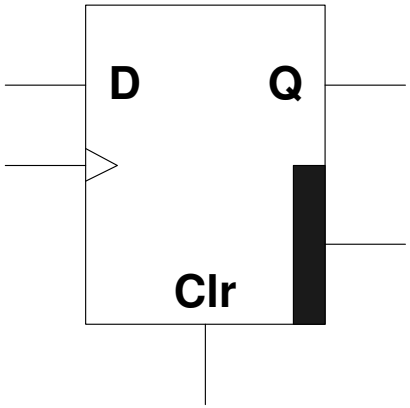
Metastability/Latches and Flip-Flops

Data Latches:

- Output follows input when latch input is asserted (level-triggered)
- Data is held while latch input is de-asserted

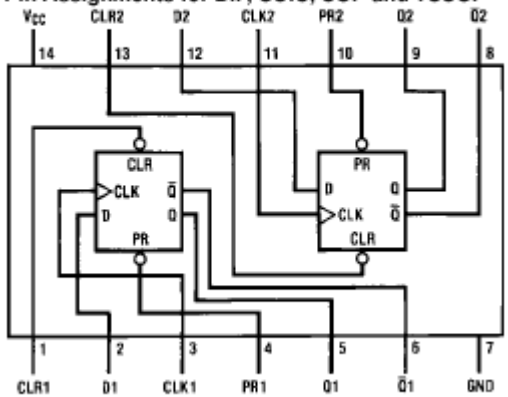
Data Flip-Flops:

- Output follows input when clocked (positive or negative edge)
- Data is held between clock events
- Commonly: Latches and FF's also provide asynchronous reset (and/or preset)
- Example synchronous FF: MM74HC74A (see below)



Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



TOP VIEW

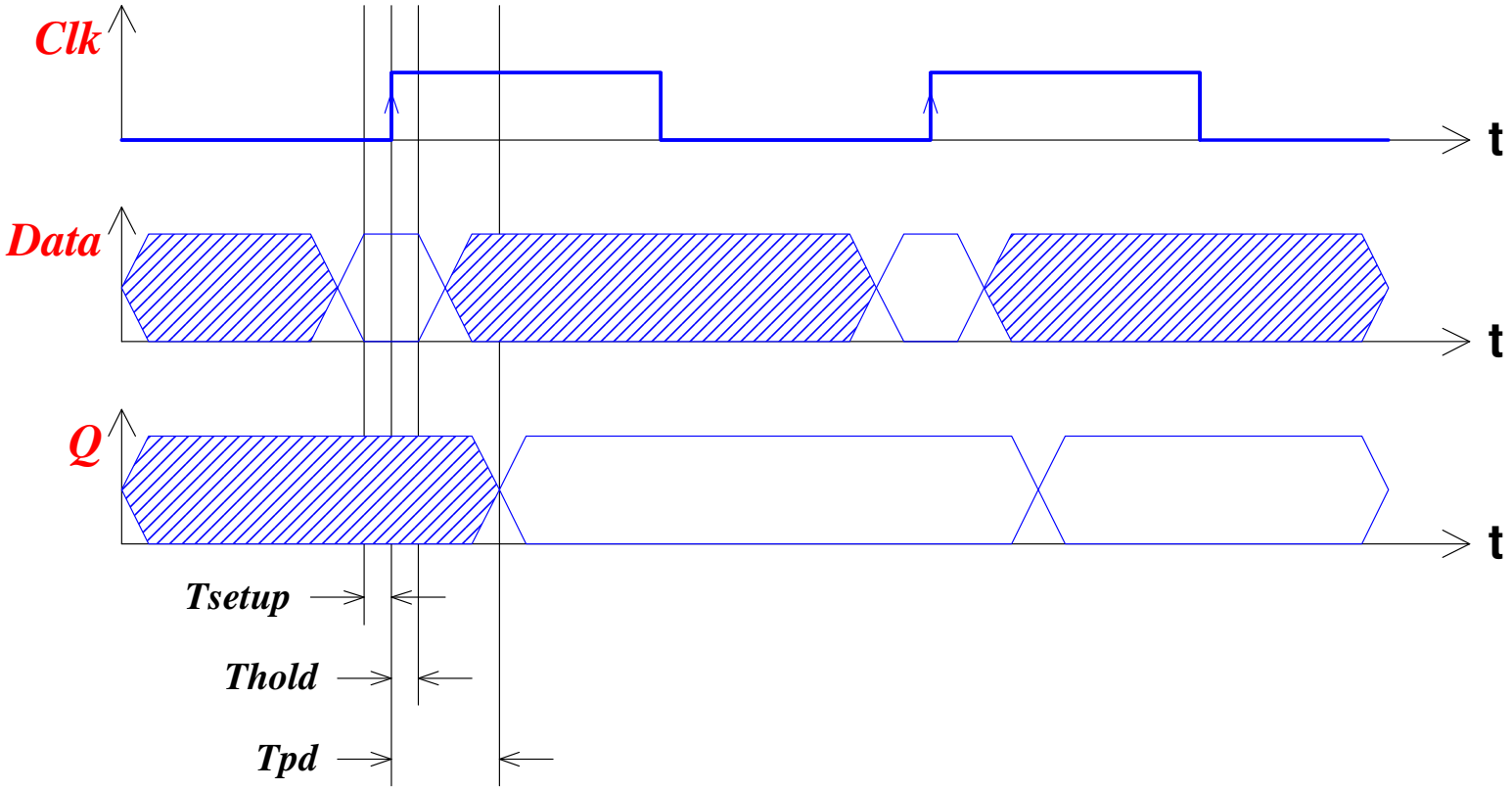
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$ 0

Note: Q0 = the level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Metastability/Timing Requirements of D-FF



Timing Characteristics of Data Flip-Flops:

- Data input has to stabilise before the clock event (data setup time **Tsetup**)
- Data input has to remain stable for some time after the clock event (data hold time **Thold**)
- Clock-to-output propagation delay **Tpd**

Data flip-flops work as expected as long as setup and hold time requirements are met...

Metastability/Timing Requirements of D-FF

AC Specification Data Flip-Flops:

- Example: MM74HC74A

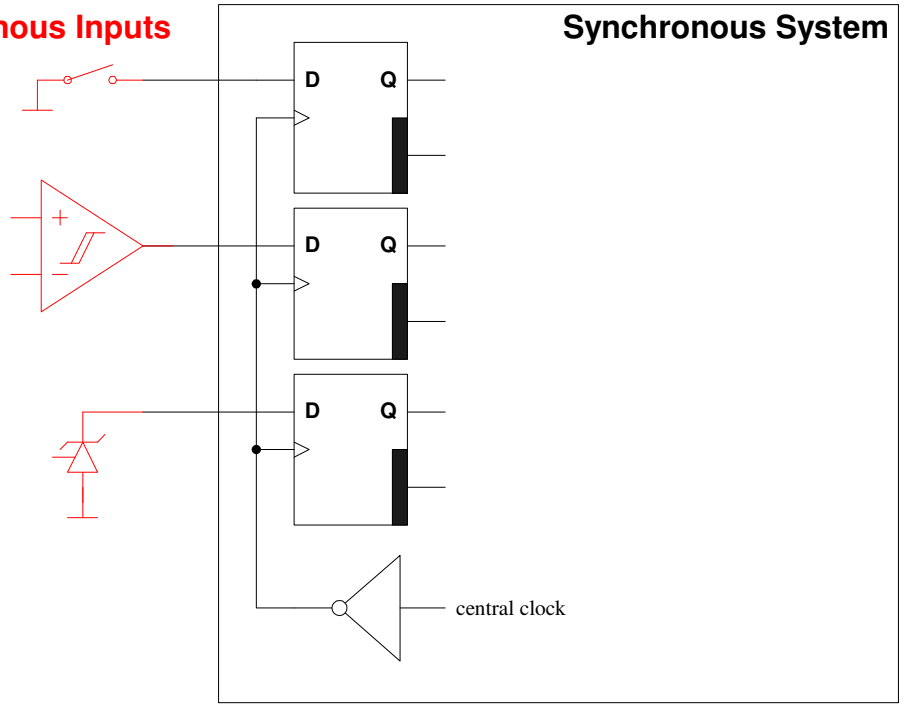
AC Electrical Characteristics

$C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	22	6	5	4	MHz
			4.5V	72	30	24	20	MHz
			6.0V	94	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	34	110	140	165	ns
			4.5V	12	22	28	33	ns
			6.0V	10	19	24	28	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V	66	150	190	225	ns
			4.5V	20	30	38	45	ns
			6.0V	16	26	33	38	ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V	20	50	65	75	ns
			4.5V	6	10	13	15	ns
			6.0V	5	9	11	13	ns
t_s	Minimum Setup Time Data to Clock		2.0V	35	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	17	20	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns

Metastability/Timing Requirements of D-FF

However: There are situations where there is no guarantee that setup and hold specs are complied with...



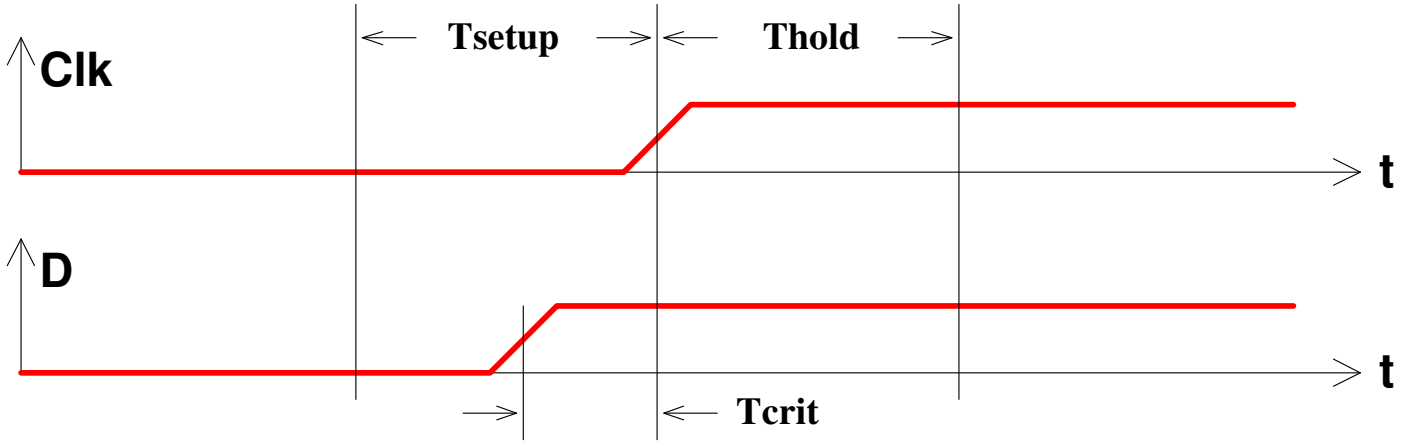
Potential violation of setup and hold requirements whenever asynchronous inputs[1] are clocked into synchronous systems.
Asynchronous inputs may change at any time without regard to internal synchronous clocks.

Is there a way to clock async signals into sync systems without violating flip-flop timing requirements? **No, there isn't...**

What happens to a flip-flop if setup and hold requirements are not met?

[1]A signal is considered asynchronous if it is not controlled by a clock, or if it is synchronised by a clock in a different clock domain

Metastability/Observation of Metastability



Observation:

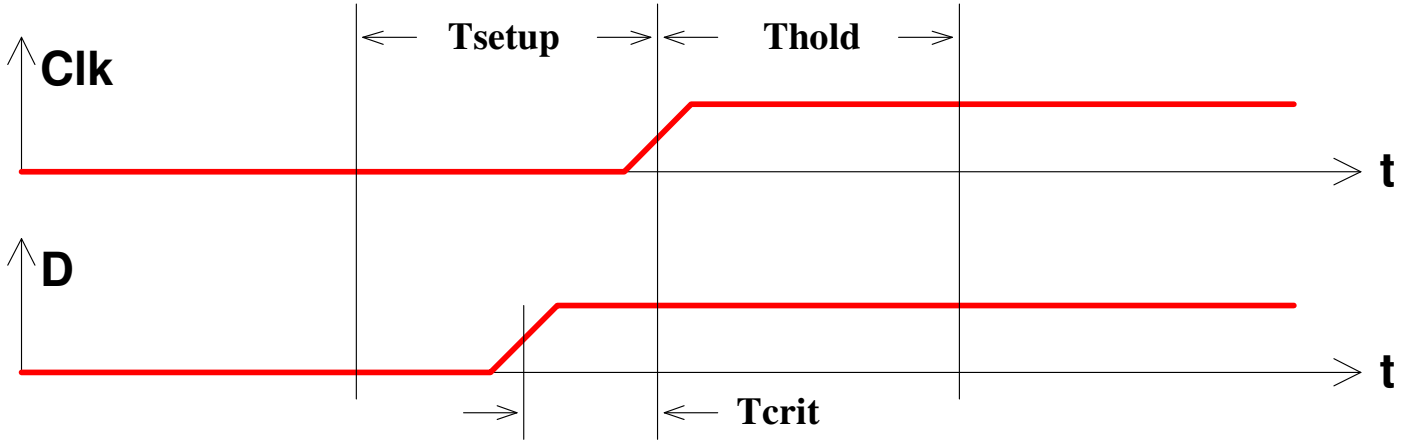
•Let the data input change state (low-to-high) during the “illegal” interval

•Relative to the clock edge there is a time Tcrit

- •If data arrives before Tcrit the output follows the input
- •If data arrives after Tcrit the output stays low.
- •(note that Tcrit may fall into Tsetup or Thold depending on FF technology)

A closer look reveals...

Metastability/Observation of Metastability



Observation of Metastability:

•As the data transition approaches the critical time Tcrit **the clock-to-output delay increases**

•For data transitions very close to Tcrit the clock-to-output delay is proportional to the logarithm of the time difference between data transition and Tcrit

Metastability = Increase of the clock-to-output delay due to violation of setup and hold timing requirements.

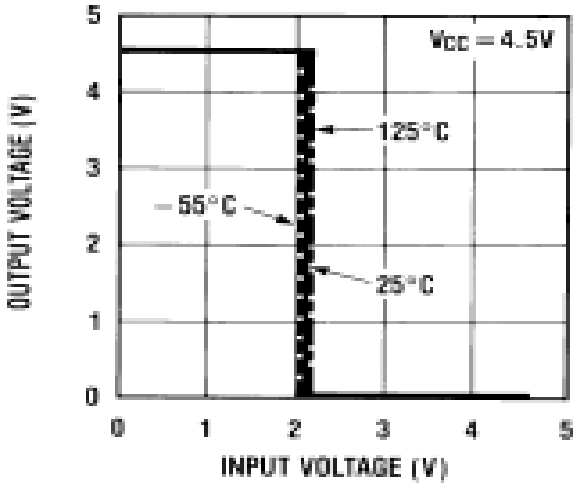
Metastability can cause excessive propagation delays and subsequent system failures.

ALL FFs (and latches) exhibit metastability. The problem cannot be eliminated. But it is possible to make metastability less likely to occur.

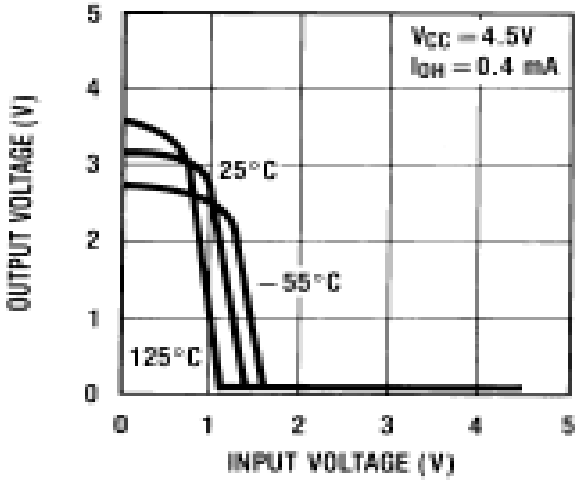
Metastability/Gain of Logic Gates

Digital Logic Gates:

- For small signals around their logic thresholds logic gates act like linear amplifiers
- Gates do provide high gains around the threshold (but note that the gain is not infinite!)
- TTL gates/unbuffered CMOS gates provide a relatively low gain (10..100)
- Buffered CMOS gates provide high gains (>1e3)
- In a few specific applications gate maybe used in their linear region (e.g. oscillators)



HCMOS



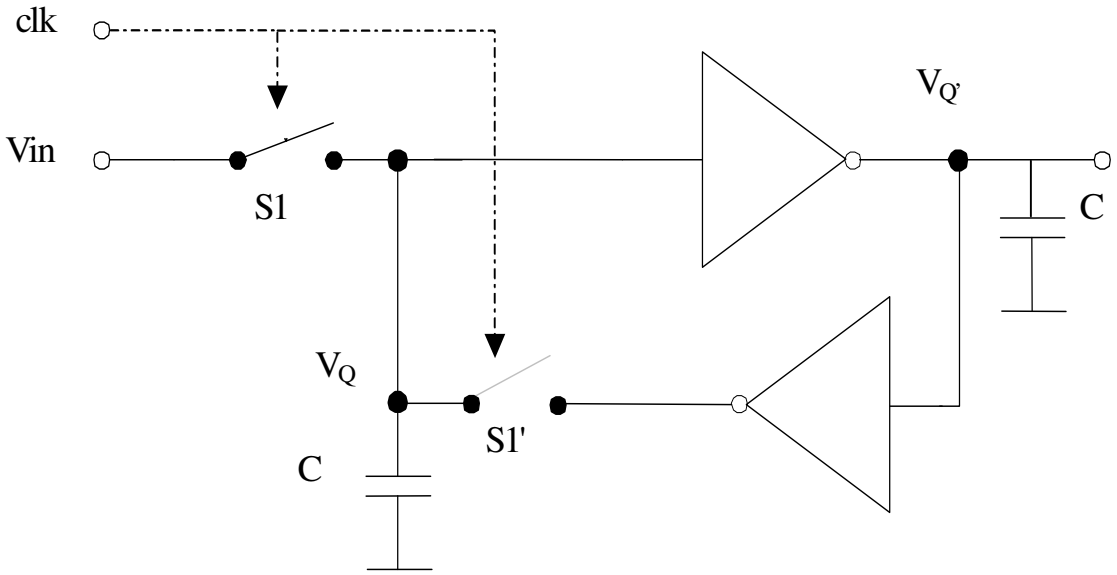
TTL (LS)

Metastability/FF & Latch Model

Model of FF's (and latches): in contrast to gates, FF's (and latches) behave like sampling amplifiers with positive feedback. They contain a *regenerative loop*.

At the clock event, input is sampled (S1 closed) and VQ' = D'.

After clock event (S1 open), the latch, once slewed into the correct position, merely holds the circuit in one state, VQ=D and output is disconnected from input.



At the clocking moment S1' opens for a short period. While open, S1 briefly pulses closed, charging capacitor C to the input voltage. When S1' closes again, ending the cycle, positive feedback through the regenerative loop forces the FF amplifiers to saturate either at the high or low state, and holding the output.

Metastability/Latch equations

- Solving differential equations describing the feedback loop and looking at t/τ »1

$$\Delta v_Q(t) \approx \frac{\Delta v}{2} exp\left(\frac{t}{\tau}\right) + \frac{V_{DD}}{2} \quad , \quad \Delta v = v_Q(0) - v_{Q'}(0)$$

Hence, metastability

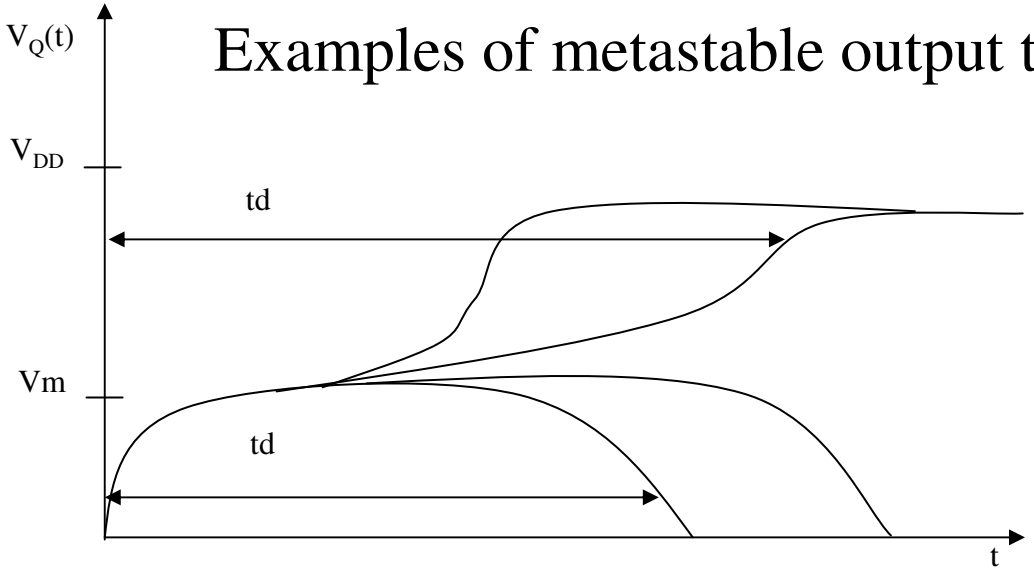
•occurs if the voltage difference at the input of the regenerative feedback loop is small (ie there is no signal to be amplified)

•It may then take a long time till the output reaches the level of one of the recognised output states

•The smaller the voltage difference at the start of this process, the longer the output hesitates

•The hesitation of the output to saturate is called the **metastable state**

Metastability/Analysis of Metastability



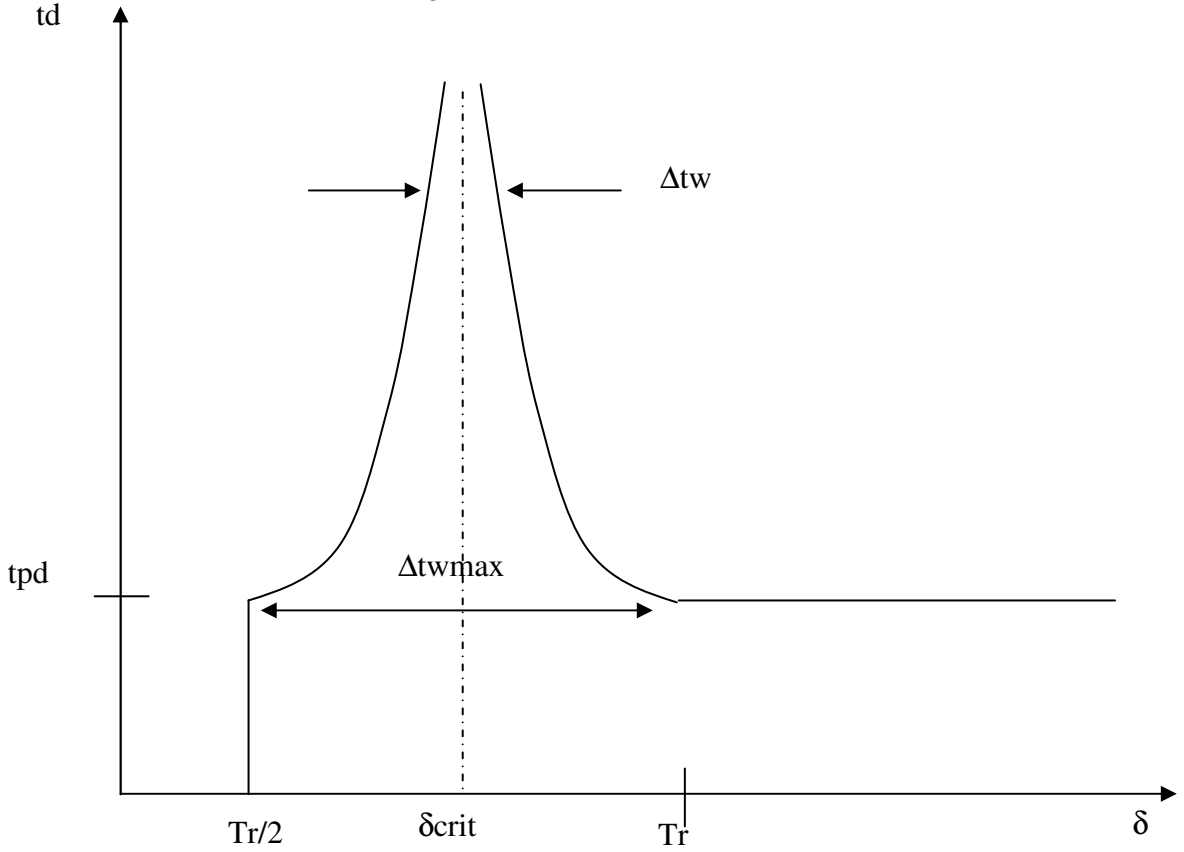
The metastable state resolution time in general is given by:

$$td = \tau ln(\frac{Tr/2}{2|\delta - \delta crit|})$$

$$\delta crit = \frac{3}{2}\left(\frac{Tr}{2}\right)$$

where Tr is the normal rise or fall time of the device and δ is the time between clock edge and data edge and the equation is valid for $Tr/2 < \delta < Tr$

Metastability/Metastable Window Model



If δ is in the interval from Tr/2 to Tr, it is in a ‘metastable window’ where the settling delay for the device (td) may be unpredictably long; the closer to δcrit, the longer the delay…..

Metastability/Metastable Window Model

- Rearranging the preceding equation, we find that for a given td>tpd, there exists a corresponding metastable window Δtw(td) given by:

$$\Delta t_w(\,td\,) = \Delta tw\,max\,exp(\,-\frac{td - tpd}{\tau}\,)\quad,\quad td \geq tpd$$

Where Δtwmax is the maximum size of the metastable window for the device (often set as |t_setup + t_hold|)

tpd is the normal propagation delay of the device

Metastability/Probability Analysis

To determine the *probability* of metastable events and hence get a handle on metastable failure *rates*, we need a model of input transitions.

A common model is the Poisson process, with λ the average rate of transitions:

Pr. (data edge in (t2-t1)) = $\alpha e^{-(t2-t1)\alpha}$

Pr. metastable failure ≈Pr. data edge in metastable window

$$= \lambda \Delta t_w(td) e^{-\lambda \Delta t_w(td)}$$

Noting that: $\lambda \Delta t_w(td) \ll 1$ and $\Delta twmax \geq \Delta tw(td)$ gives:

Pr. Metastable failure ≈ $\lambda \Delta t_{wmax} e^{-\frac{td-tpd}{\tau}}$

Metastability/Probability Analysis

- A more useful characterization is the mean failure rate (MFR) given by:

$$\lambda \Delta t_w(td) f_{clk}$$

Where fclk is the (mean) clock rate. This is valid because the occurrence of metastable failure is itself characterized by a Poisson process.

The Mean Time between Failure (MTBF) is then:

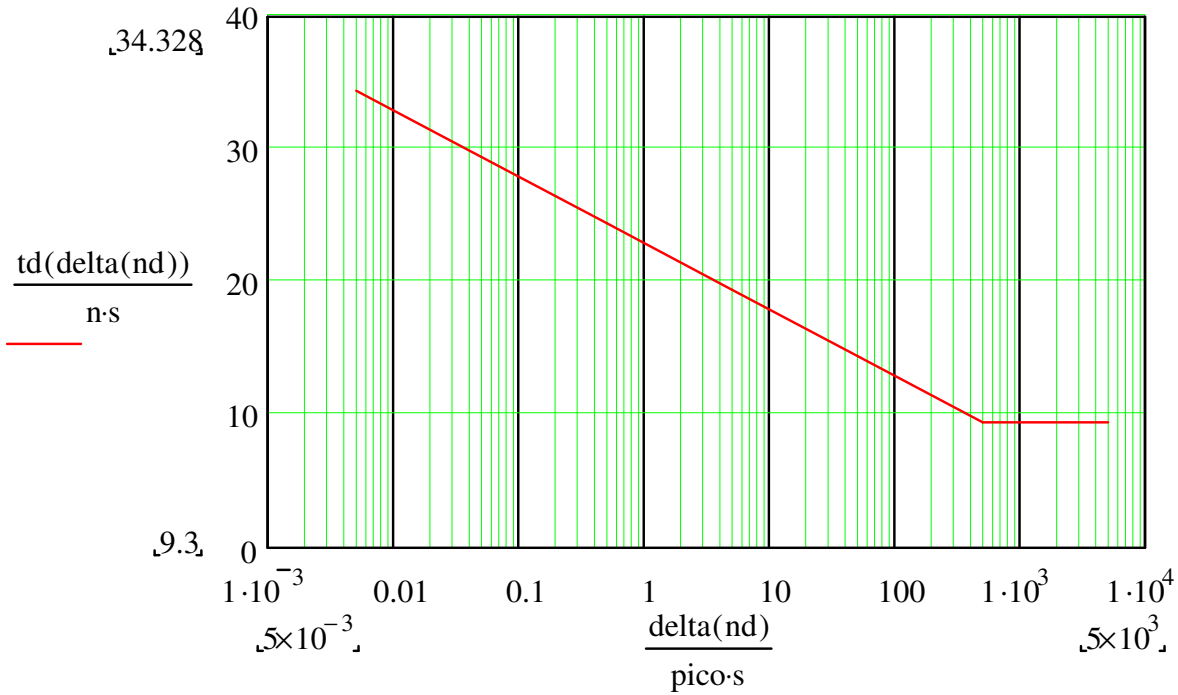
$$MTBF = \frac{T_{clk} e^{\frac{(td - tpd)}{\tau}}}{\lambda \Delta tw max}$$

where Tclk is the clock period and λ is the data rate

Metastability/Device Testing

Metastability

- Example: Actel ACT-1 gate array
- Clock-to-output delay vs $|\delta-\delta_{crit}|$



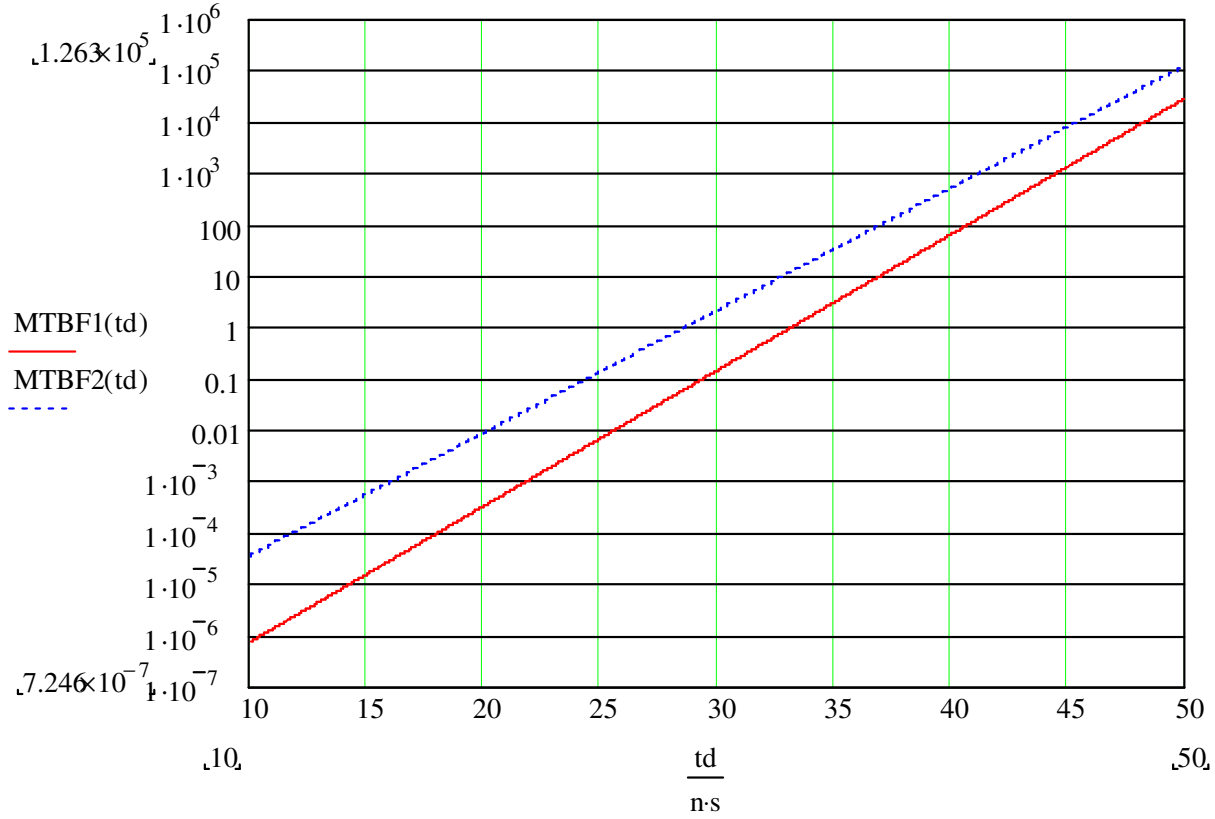
Note: Clock-to-output delay is proportional to the logarithm of *effective size of metastable window*

Metastability/Device Testing

- Formerly difficult: issues include how to detect metastable failure and how to ‘reliably’ trigger metastability
- Solutions for triggering : variable delay ring oscillator, precision pulse generators, two asynchronous signal generators
- Solutions for detection: variable delay circuit, now – high speed oscilloscopes

Metastability/Device Testing

Results often given (e.g. by manufacturers) in terms of MTBF



You can calculate the settling coefficient (τ) from the graph slope but extracting a realistic Twmax from the intercept is difficult…

Metastability/Device Testing

By fitting the following linear equation to the MTBF plot:

$$ln(y) = c + \left(\frac{1}{\tau}\right)t$$

Log10 can also be used but the parameters calculated will be even less ‘real’

Where y = MTBF.fclk.λ and ‘t’ measures clock to output delay

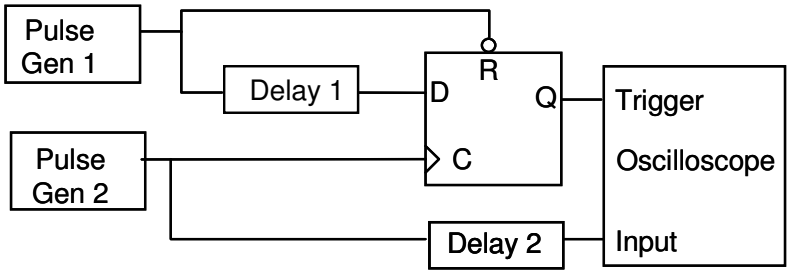
Note that this means that c = ln(1/Δtwmax)

Calculating the slope: (ln(y2)-ln(y1))/(t2-t1) gives 1/τ

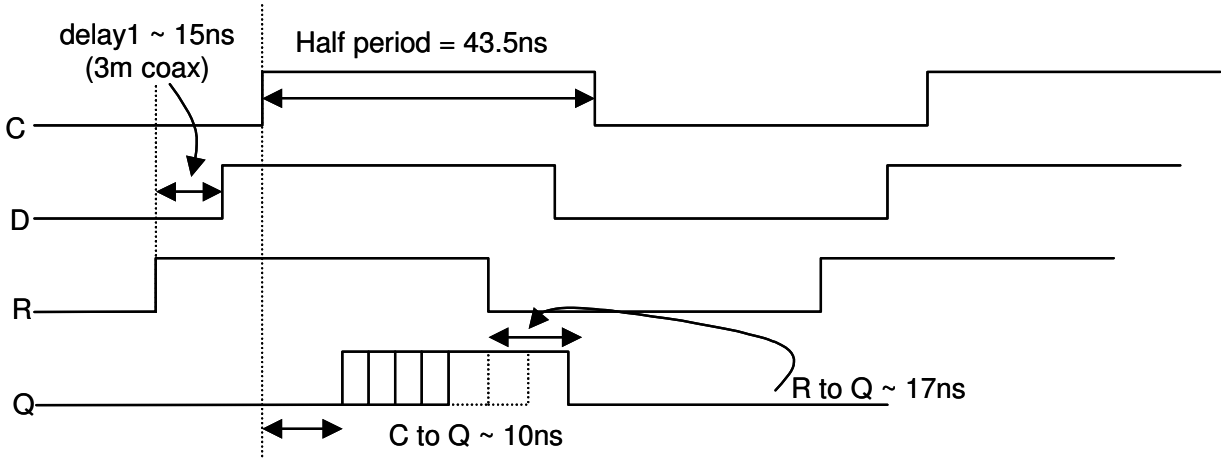
Calculating the intercept: ln(y) – (t/ τ) gives the natural logarithm of 1/ Δtwmax

Can include normal tpd of the device by using (t – tpd) instead of t

Metastability/Device Testing



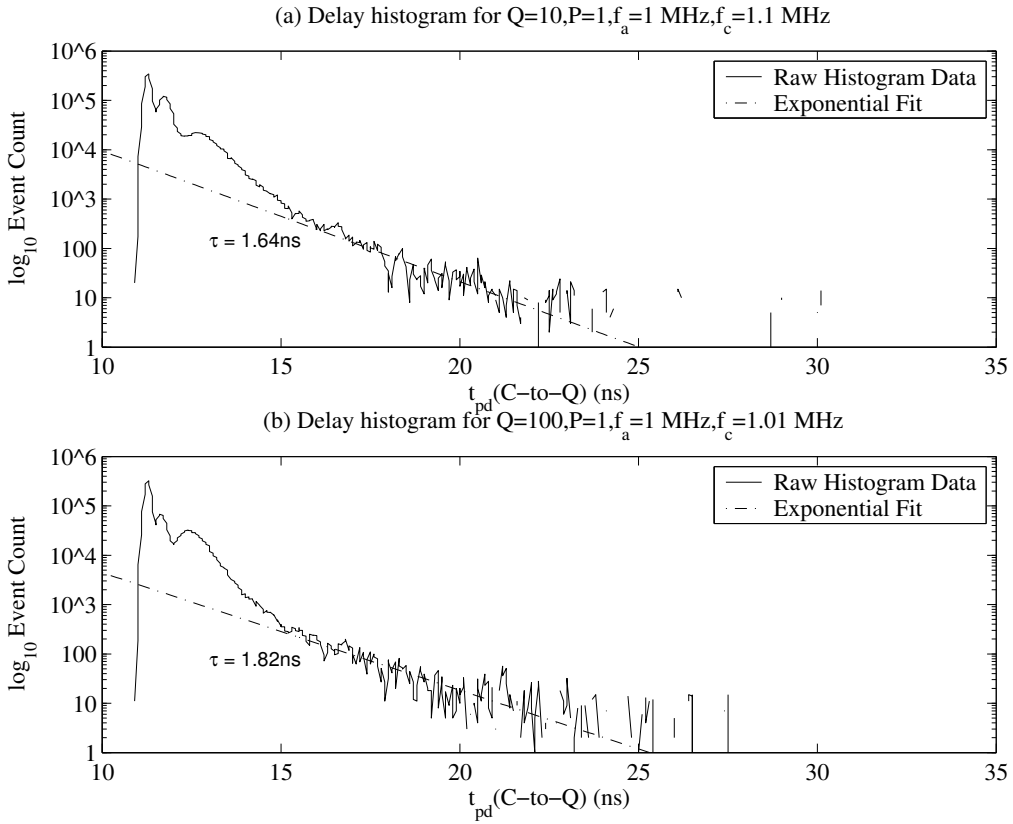
(a)



(b)

Metastability/Device Testing

Oscilloscope test method results:



Here finding Twmax intercept is difficult because y- axis is an event count

Metastability/General Recommendations

Metastability cannot be avoided at the boundary between asynchronous and synchronous systems.
However - the propability that metastable states are encountered can be significantly reduced:

•Use synchronisers
•Use faster flip-flops (narrower metastable window *Tw*)
•Use metastable-hardened flip-flops (designed for very high bandwidth and reduced sampling times – optimised for clock domain input circuitry)
•Cascade flip-flops in synchronisers (two or more). A chain of N flip-flops has a propability of P^N where P is the chance of metastable failure for one flip-flop
•Reduce sampling rate
•Avoid input signals with low dV/dt

Special completion detection circuits can detect metastable states… (however circuitry following the completion detection circuits must be asynchronous…)

Metastability/Synchronisers

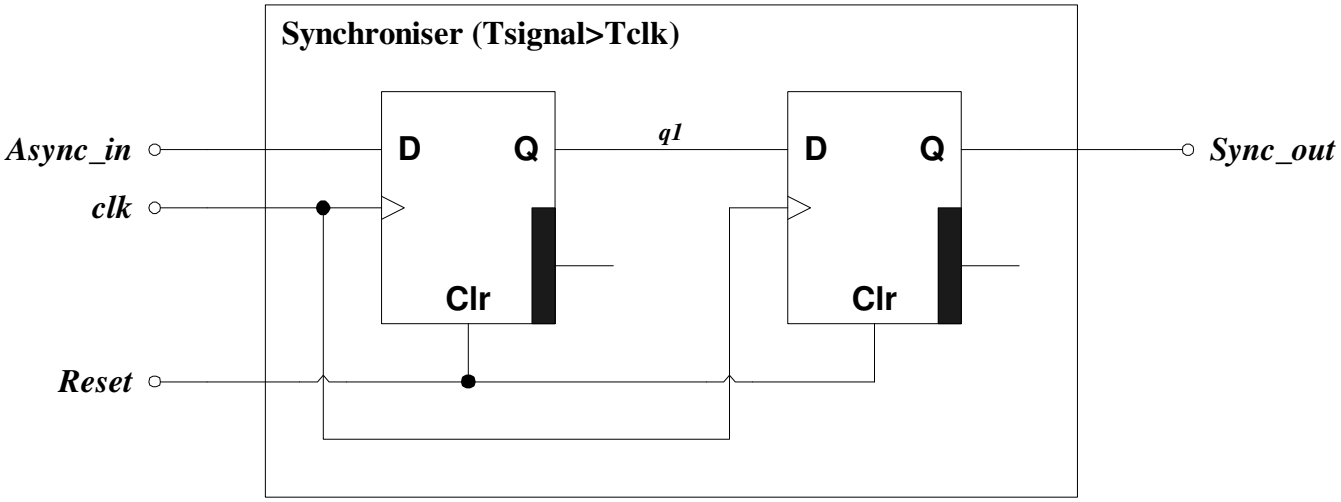
Synchronisers

We have shown: Mean time between failures of a circuit with an asynchronous input is exponentially related to the time available for recovery from a metastable condition. **Use synchronisers to create a time buffer for recovering from a metastable event!**

BUT: A single asynchronous. signal should never be synchronised by more than one synchroniser! *(to do so would risk having the outputs of multiple synchronisers produce different signals)*

Synchroniser A

•Use synchroniser A if expected pulse width of async. input is larger than the clock period



Metastability/Synchronisers

Synchroniser A Operation

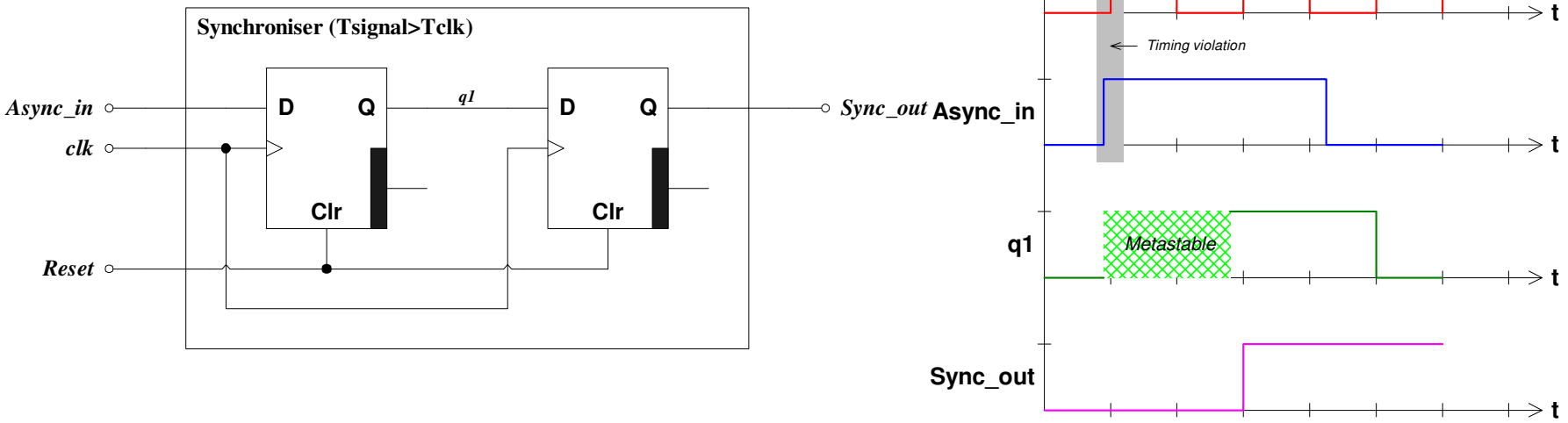
•If the async. input reaches a stable condition outside the setup interval, it will be clocked through with a latency of two clock cycles

•Otherwise, FF1 may enter metastability

•If metastability is resolved in less than one clock cycle, FF2 will have a stable input

•Price paid: Latency

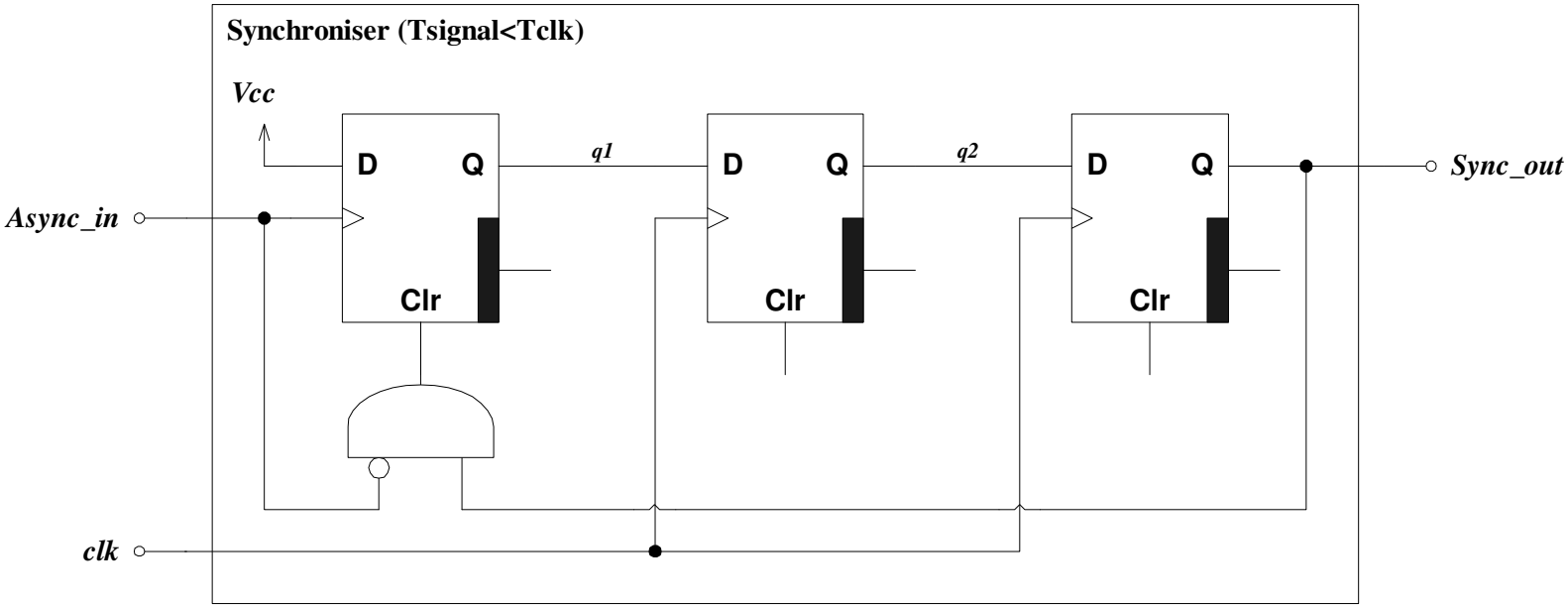
•Scheme can be improved by deeper cascade (3..)



Metastability/Synchronisers

Synchroniser B

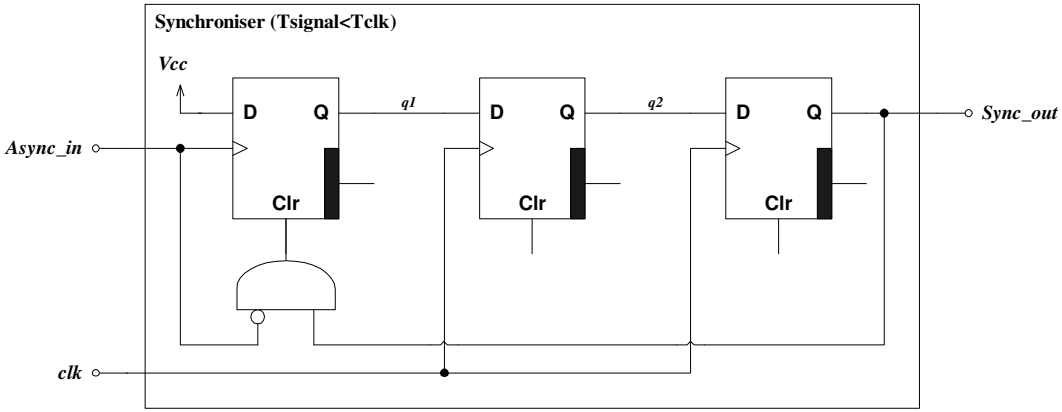
•Use synchroniser B if expected pulse width of async. input is smaller than the clock period

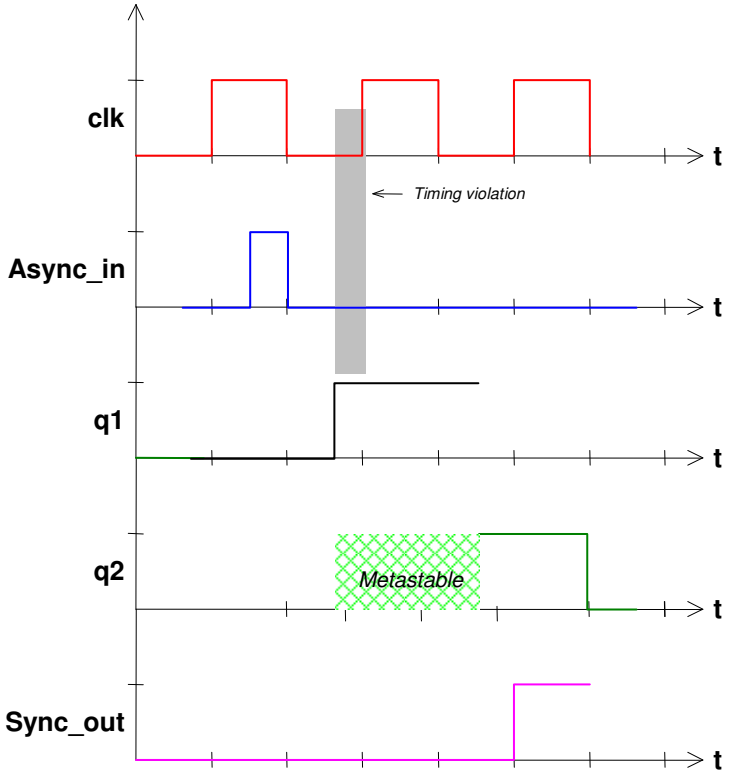


Metastability/Synchronisers

Synchroniser B Operation

- Note that D input of first FF is connected to Vcc, while async input clocks the FF
- Remaining two FF's are clocked by system clock (clk)
- A short pulse will drive q1 high
- High will propagate to Sync_out after two clk edges
- Asynchronous reset of FF1





Metastability/Synchronisers

Synchronisers at boundaries of clock domains

•Use synchronisers when a signal must cross a boundary between clock domains

•If clk1<clk2 use synchroniser A at the input of clock domain #2

•Otherwise use synchroniser B