UNIVERSITY OF MARYLAND

Incorporating Temperature-Leakage Interdependency into Dynamic Voltage Scaling

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Outline

- Basics on dynamic voltage scaling
- Motivation of the current work
- Modeling temperature-leakage interdependency
- DVS scheduling for total energy minimization
- Experiments and results

DVS for Dynamic Power Reduction

- What is dynamical voltage scaling?

  A technique that varies the operating voltage (and thus clock frequency) at run time based on the computation load of the application in order to perform the computation with the minimal energy consumption.

- How DVS provides power/energy saving?

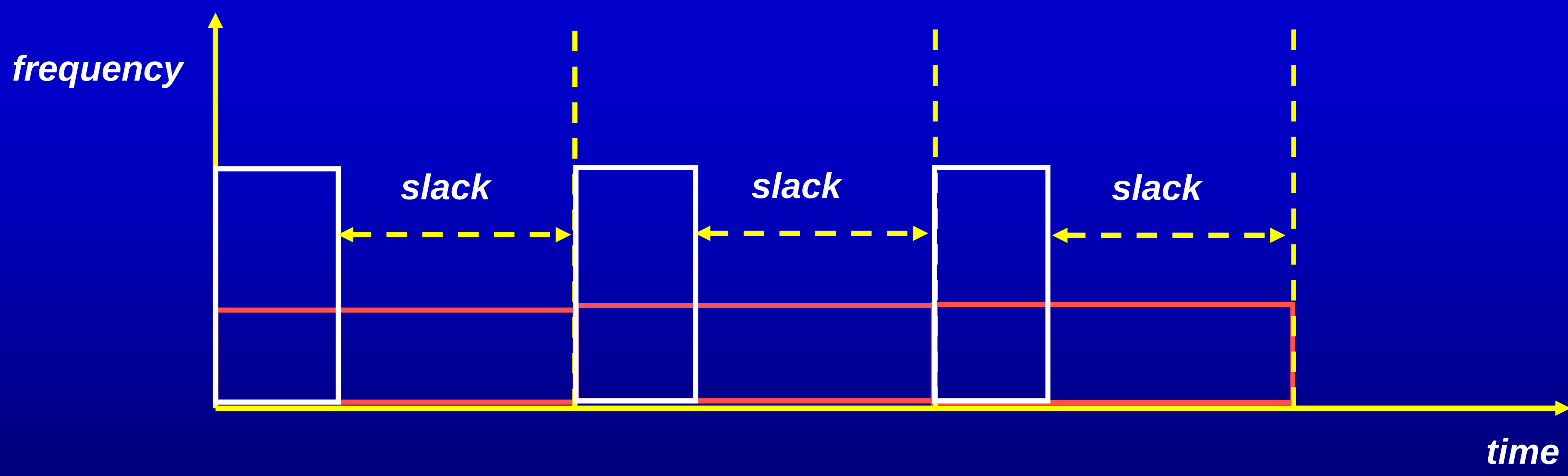
$$P \propto C\, V^2 f$$

  - Reducing V gives a reduction on power P
  - It also gives about linear reduction on clock frequency f
  - Reducing V gives a quadratic saving on energy E

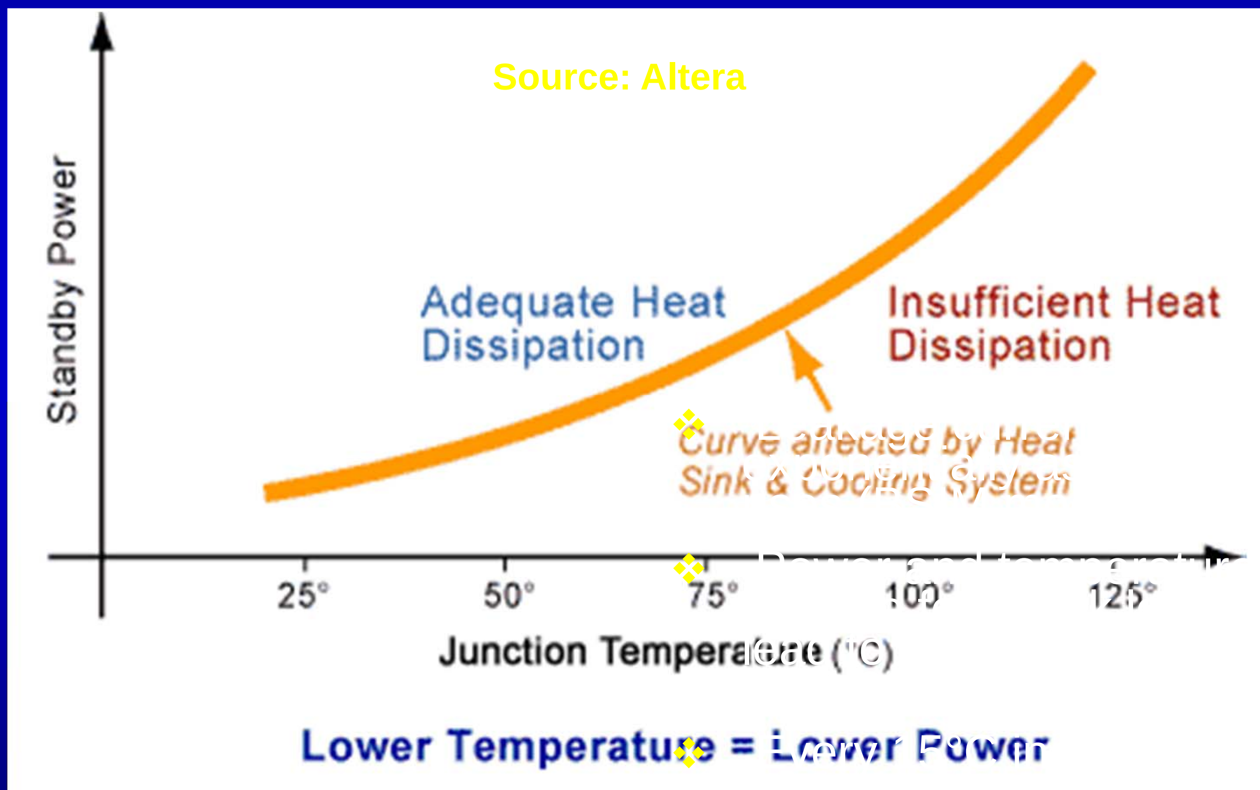
$$E_{dyn} \propto V^2$$

DVS for Real-Time Applications

- Suppose that a data sample comes every 1 ms
- Requires processing time of 250 μs at 600MHz
- DVS: reduce voltage such that clock slows down to 150MHz

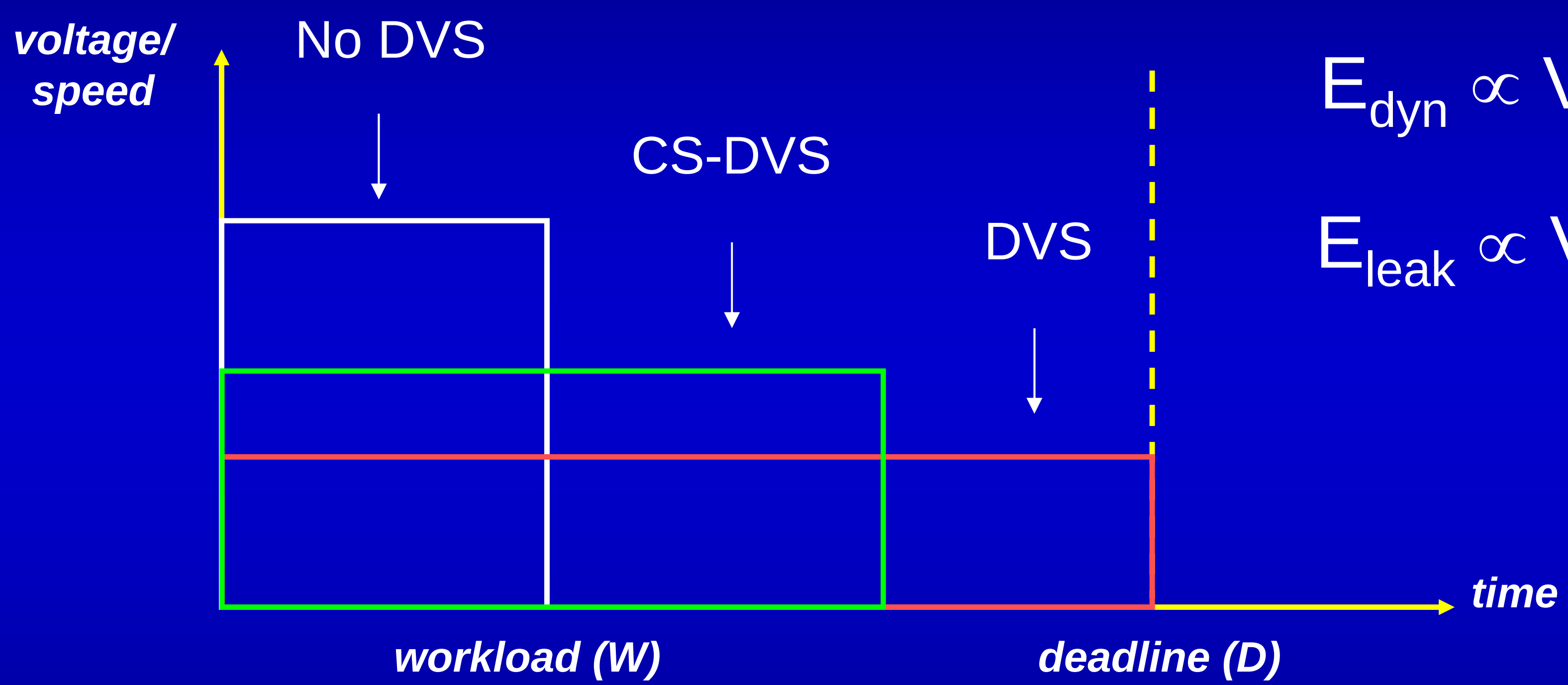


Why Leakage and Temperature



- ...es ...perature
- ...can form a ...at may ...(He et al.
- ...ally causes a delay or slew to increase roughly 10 to 15% (www.edn.com 2005)

Leakage Aware DVS



$E_{dyn} \propto V_{dd}^2$

$E_{leak} \propto V_{dd}, t$

DVS: Yuan et al. TCAD'05; Aydin et al. RTSS'01; Hong et al. RTSS'98

CS-DVS: Jejurikar et al. DAC 2004

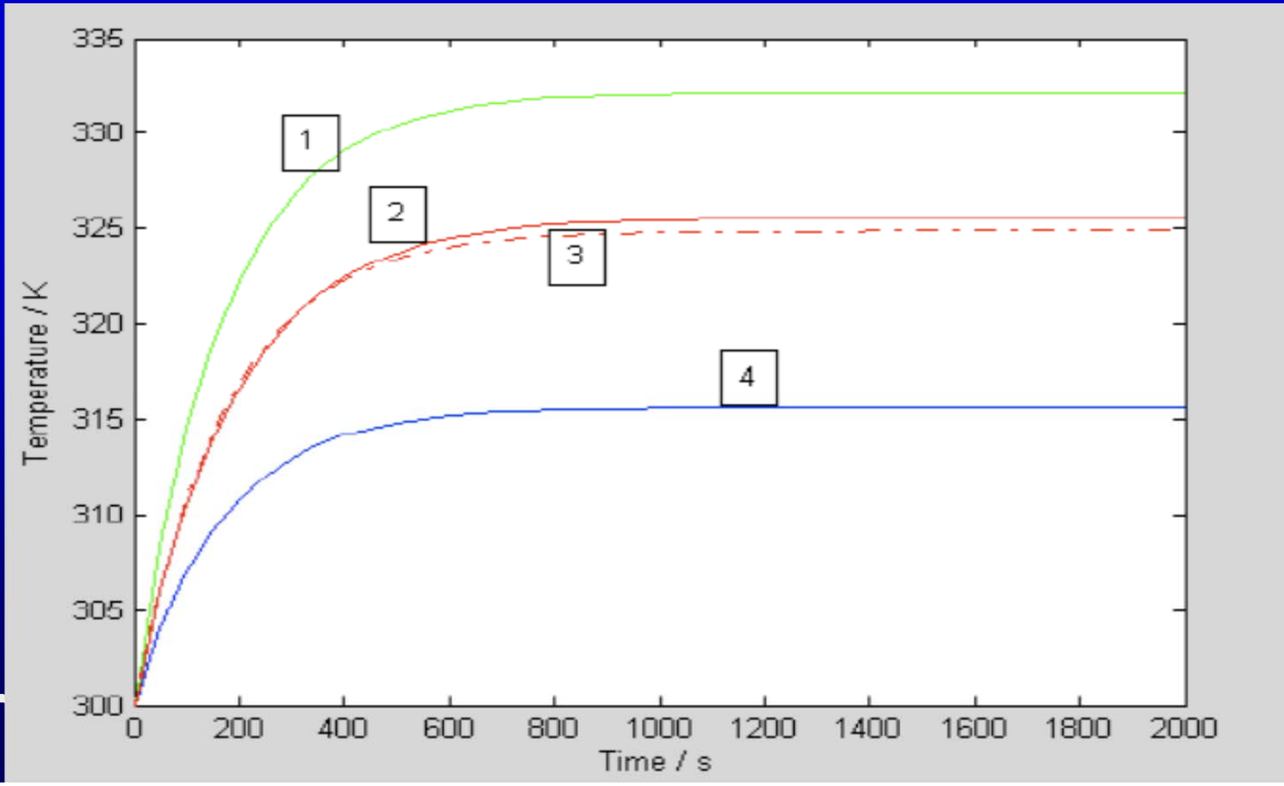
Temperature Modeling

- Model on-chip heat transfer as an RC circuit

$$C\frac{dT}{dt} + \frac{T - T_{amb}}{R} = P$$

  - Challenge: $P = P_{dyn} + P_{leak}$ and P_{leak} depends on T

2: numerical solution
1: $T = T_{max}$
4: $T = T_{amb}$
3: our solution



Temperature Modeling

- Model on-chip heat transfer as an RC circuit

$$C\frac{dT}{dt} + \frac{T - T_{amb}}{R} = P$$

  - Challenge: $P = P_{dyn} + P_{leak}$ and P_{leak} depends on T
- Leakage current model:

$$I_{leak} = I_0 \cdot (A \cdot T^2 \cdot e^{\frac{\alpha V_{dd} + \beta}{T}} + B \cdot e^{\gamma V_{dd} + \delta}) \cdot N_{gate}$$

  - Quadratic approximation
- Analytical solution exists

$$\frac{dT}{dt} = a_1 \cdot T^2 \cdot e^{a_2/T} + a_3 \cdot T + a_4$$

Simulation Validation of the Model

- Initial temperature: 300K, 330K, 370K
- Voltage: 0.8V, 0.9V, 1.0V
- Mean Absolute Error on temperature estimates against numerical sampling

		P_{dyn}	300K	370K	our model
300	0.8	15.25	4.42	3.27	0.14
300	0.9	24.70	7.28	3.11	0.31
300	1.0	37.35	12.40	1.44	1.08
330	0.8	15.25	4.54	3.14	0.17
330	0.9	24.70	7.44	2.93	0.33
330	1.0	37.35	12.68	1.65	0.75
370	0.8	15.25	4.70	2.99	0.38
370	0.9	24.70	7.71	2.70	0.54
370	1.0	37.35	13.04	1.24	0.92
average MAE			8.25	2.50	0.51

Optional DVS for a Single Task

- Problem: how to complete a single task by its deadline with the minimal total energy?

Lemma 1. When the system can complete the execution of the single task at a given V_{dd} in time $x < d$, and the system is not allowed to go to idle mode during the execution, the total energy will be minimized with the following scheduling: idle during $[0, d-x]$; run at V_{dd} during $[d-x, d]$.

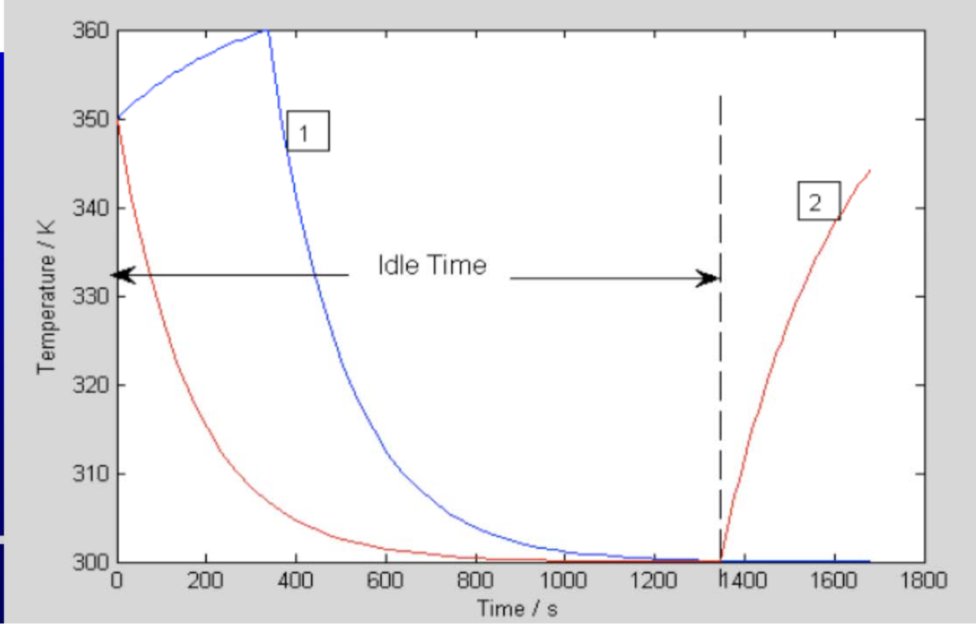
Lemma 2. To complete w units of computation, leakage energy during the execution time $E_{leak} = \int_0^{t_{active}} P_{leak}(t)dt$ increases as V_{dd} increases.

Optional DVS for a Single Task

Theorem. Let v^* by the lowest voltage to complete the task by the deadline d and x^* by the execution time to complete the task under the lowest available voltage v_{min}, the total energy is minimized by the following scheduling:

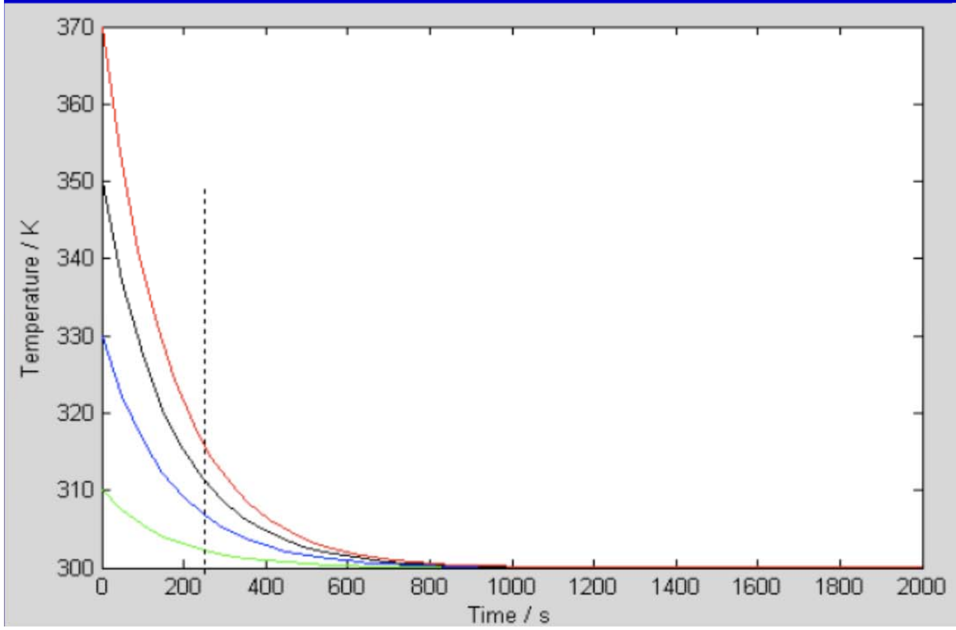
- if $v^* \geq v_{min}$, execute the task at v^* during $[0, d]$.
- if $v^* < v_{min}$, idle during $[0, d - x^*]$; run at v_{min} during $[d - x^*, d]$.

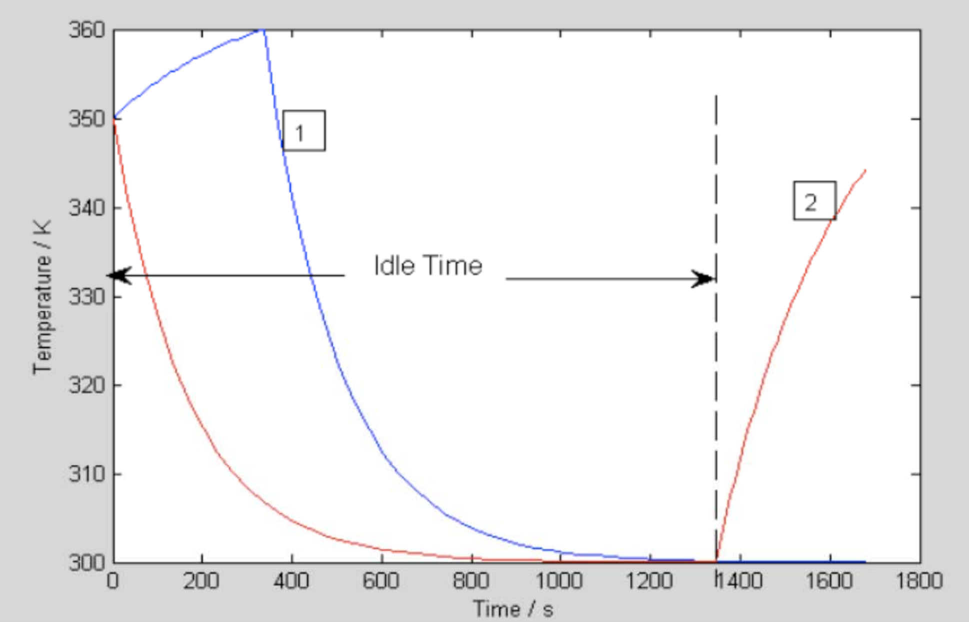
- This (2) is different from traditional DVS (1) or the best known CS-DVS solution.
  - run at low temperature to save leakage power



Online DVS for Multiple Tasks

- Why cannot combine the optimal solution for each single task?
  - Problem: high starting temperature for next task
  - Solution: leave a small idle time to cool system down, longer idle time will not cool temperature down that much, better to use for DVS.





Simulation Setup

- Thermal parameters

R	$1.2^oC/Watt$
C	$140.45mJ/^oC$
T_{amb}	$300K$
T_{worst}	$370K$
V_{dd_ref}	$1.0V$
V_{dd}	$0.8 \sim 1.0V$
f_ref	$2.08GHz$
P_{dyn_ref}	$37.35W$
P_{sleep}	$50\mu W$
V_{th}	$0.3V$

- Task sets

Taskset	Task Number	Utilization Factor
1	5	23.76%
2	11	40.41%
3	8	31.86%
4	6	33.44%
5	5	26.45%
6	11	29.20%
7	15	27.13%
8	8	22.84%
9	11	33.87%
10	9	21.41%
average	8.9	29.04%

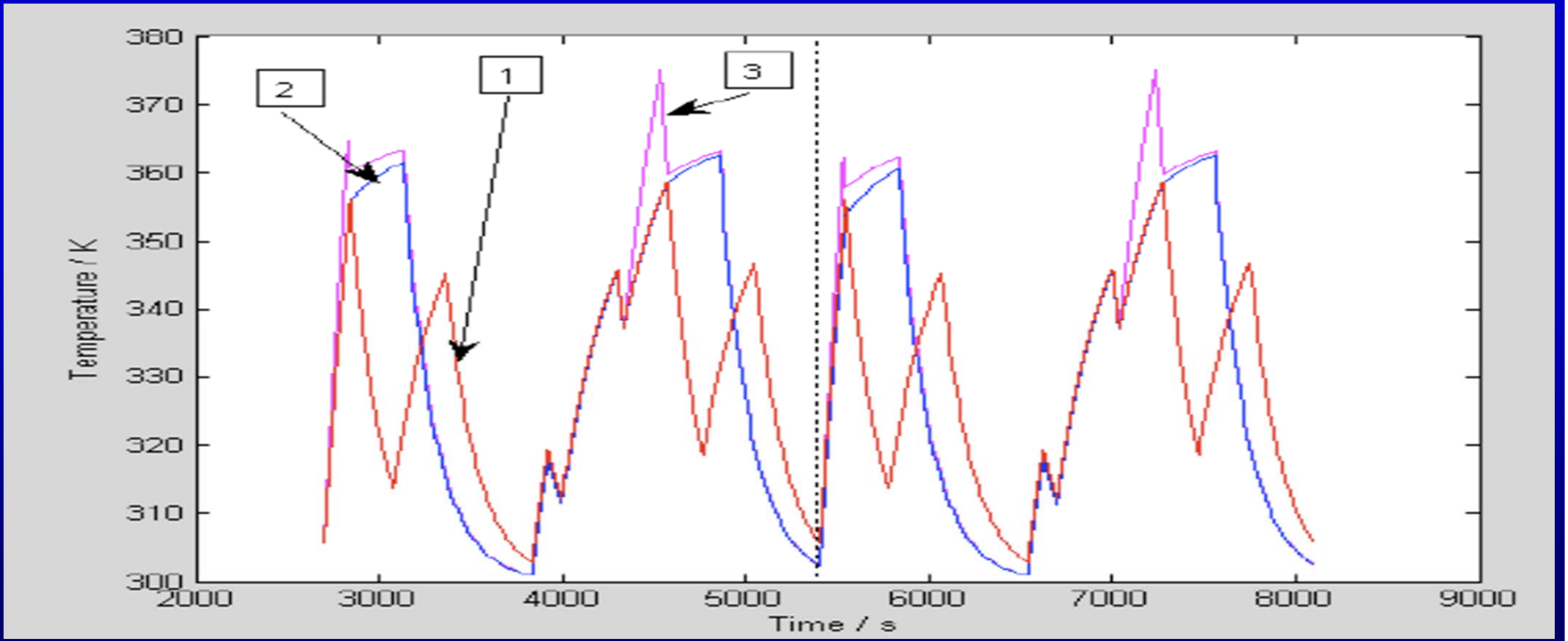
Simulation Results

- Total energy savings over DVS, CS-DVS, and non-DVS

Taskset	$E_{TDVS}(10^4 J)$	dE_{DVS}	dE_{CSDVS}	dE_{NONDVS}
1	41.4	5.27%	10.87%	69.81%
2	154.6	4.72%	12.24%	70.64%
3	105.8	4.66%	5.05%	69.98%
4	64.14	8.32%	14.35%	65.96%
5	46.66	4.82%	4.82%	69.74%
6	162.9	6.03%	7.13%	83.43%
7	192.2	4.96%	7.59%	78.11%
8	110.6	5.81%	9.95%	79.63%
9	149.4	10.59%	11.01%	94.16%
10	123.1	6.84%	9.32%	83.31%
average	-	6.16%	9.23%	76.48%

Simulation Results

- Temperature of our approach (1), DVS (2), and CS-DVS (3). Clearly, our approach has the system running at lower temperature



Thank You