Advanced Digital Phase-Locked Loops

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Outline of Talk

- **Digital Phase-Locked Loops**
- **Integer-N Synthesis**
- **Fractional-N Synthesis**
- **Direct Frequency Modulation**
- **Practical Implementation**

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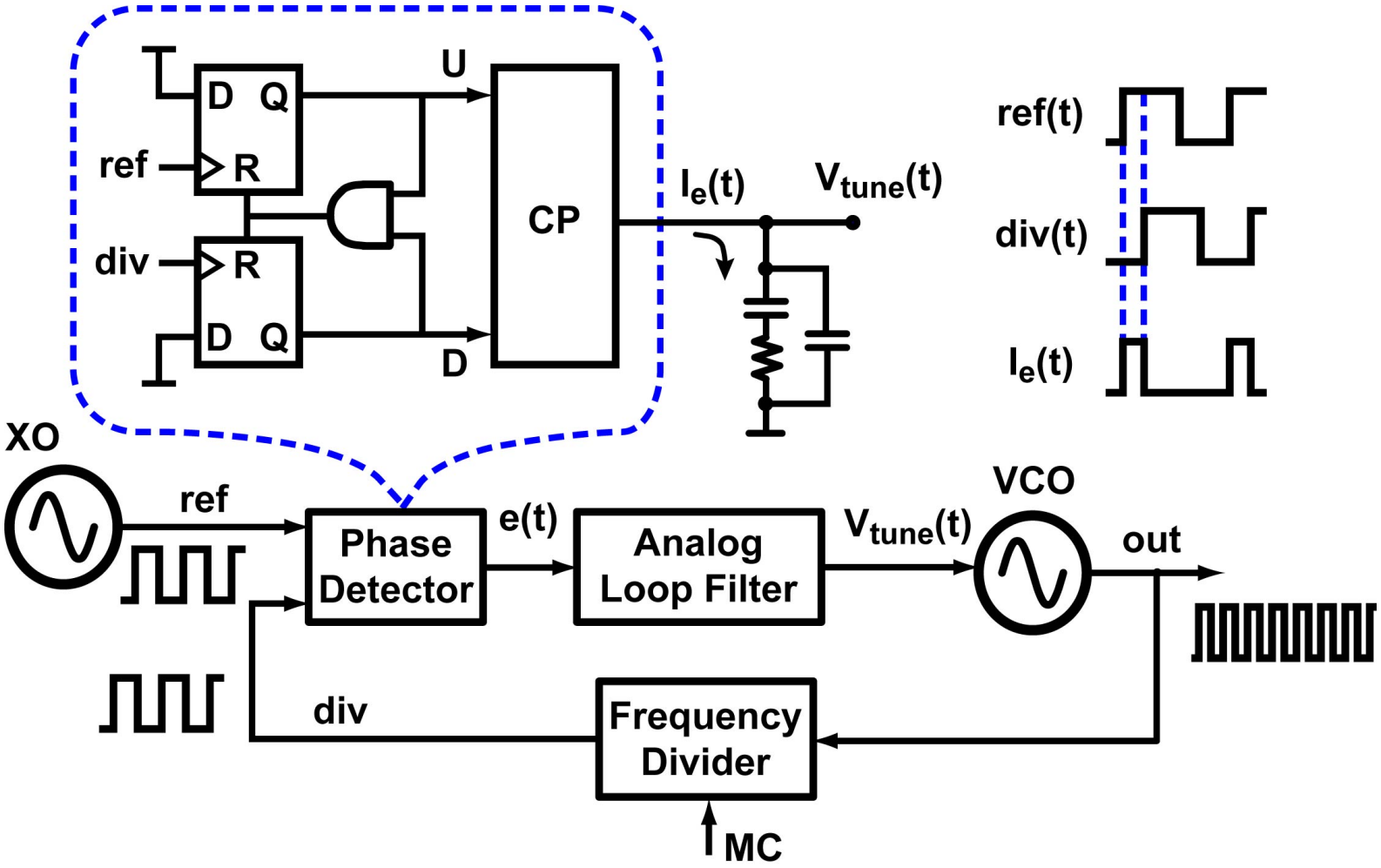
Analog Charge-Pump PLLs



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Motivation to Investigate Digital PLLs

- **LO phase noise limits *wireless applications***
- **Clock jitter limits *digital applications***
- **Analog PLLs do not scale down as process**
- **Spur/noise cancellation techniques are hardly implemented in analog PLLs**

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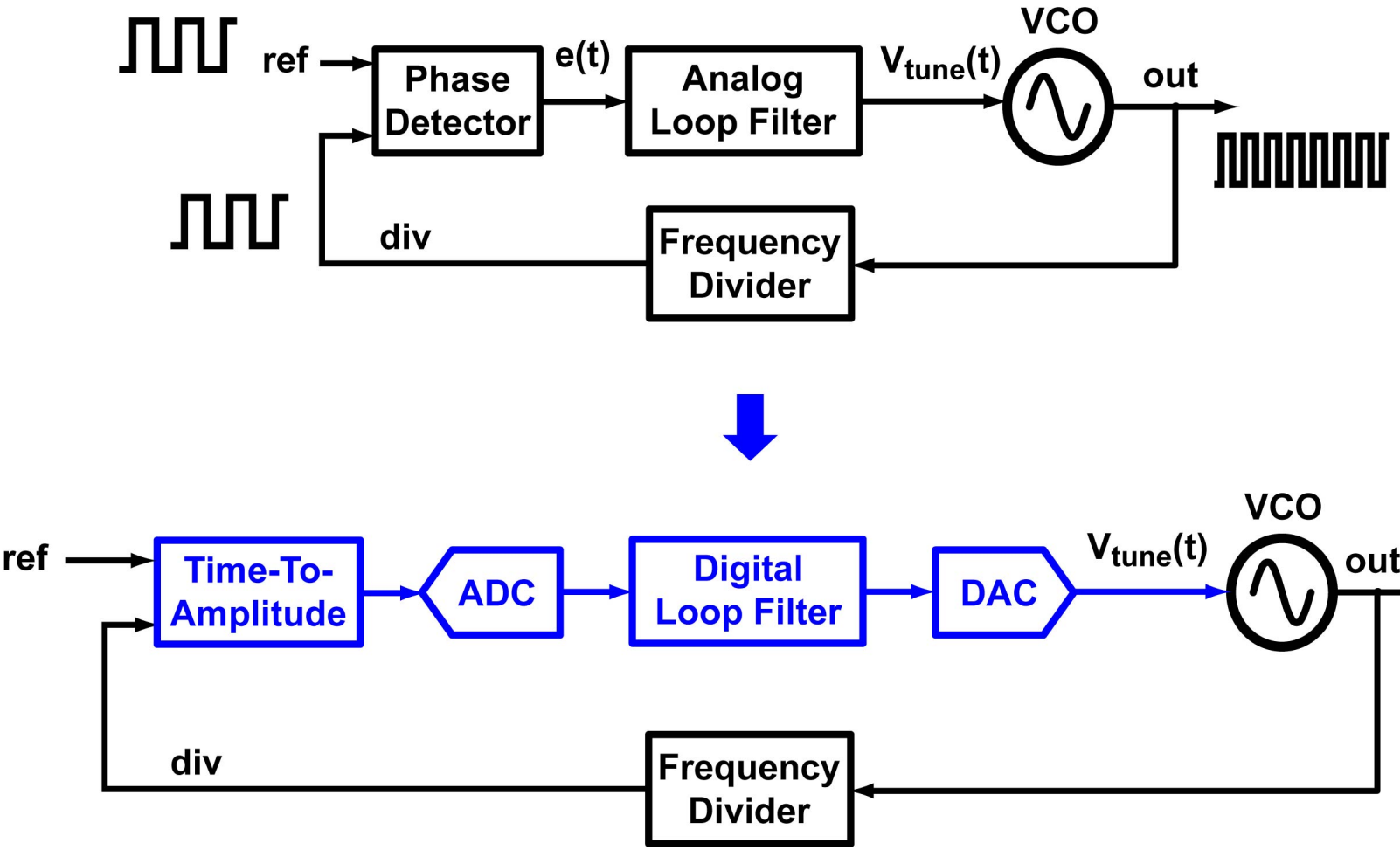
From Analog to Digital PLL



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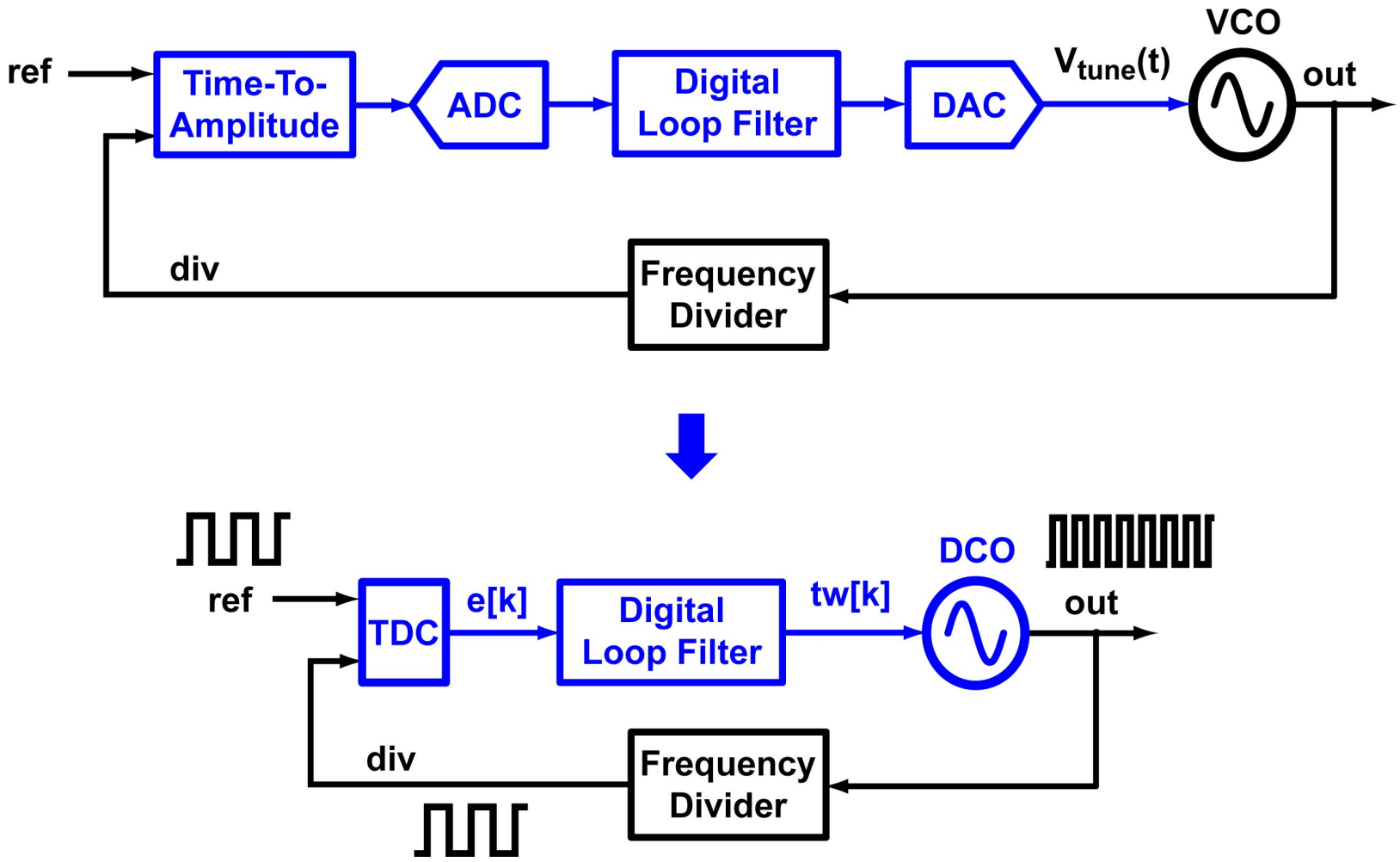
More-Digital PLL



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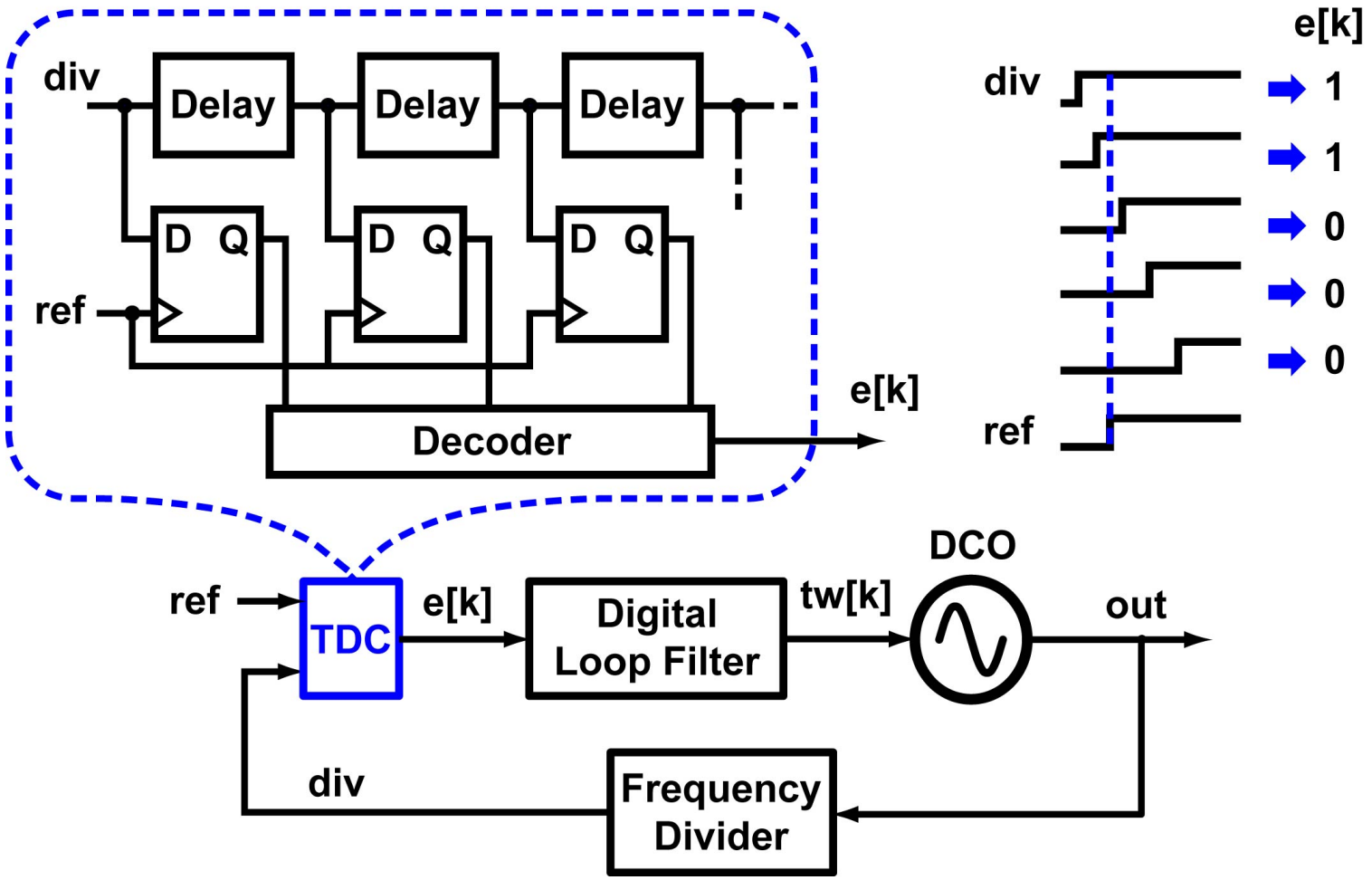
Time-To-Digital Conversion



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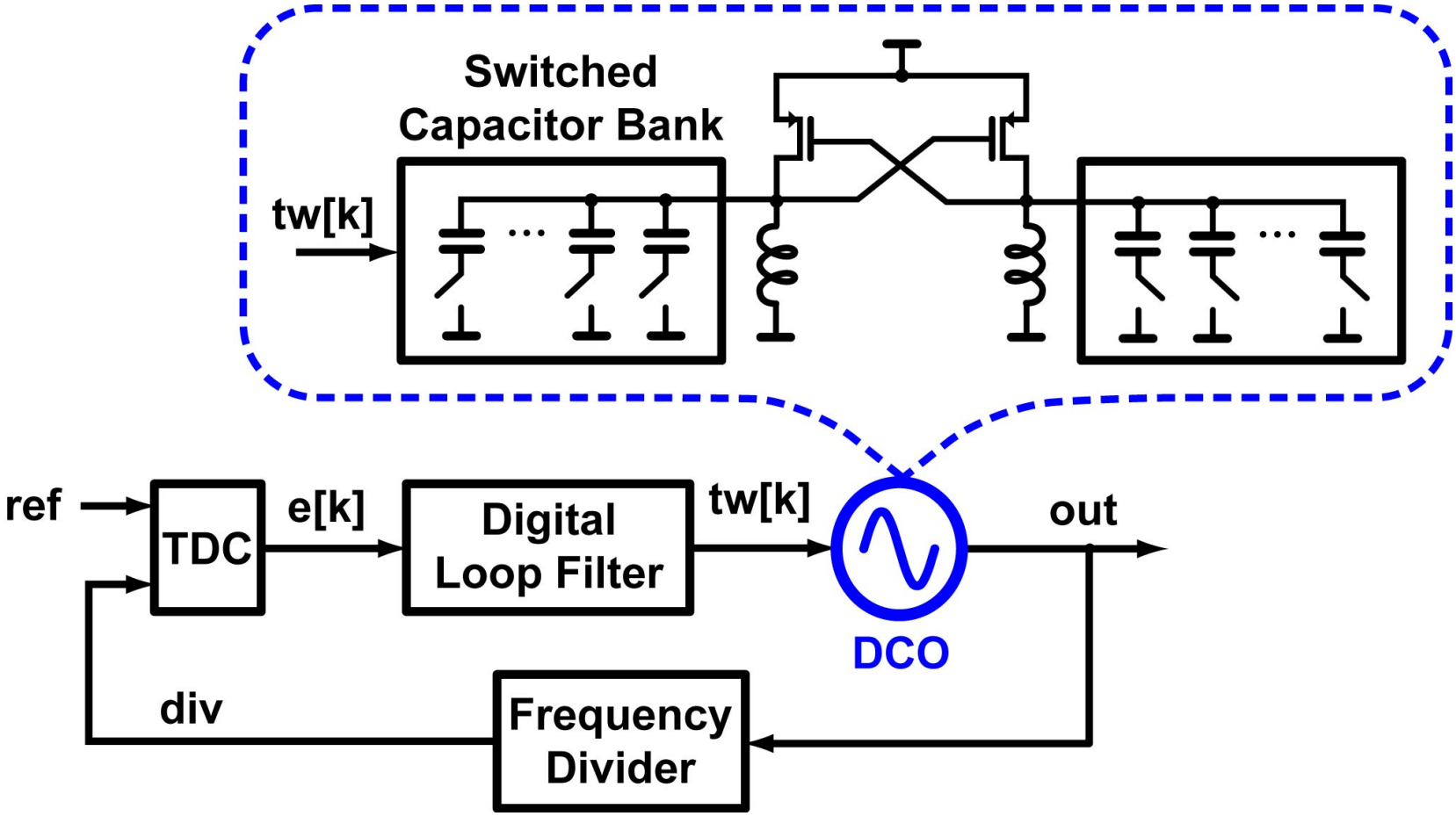
Digitally-Controlled Oscillator



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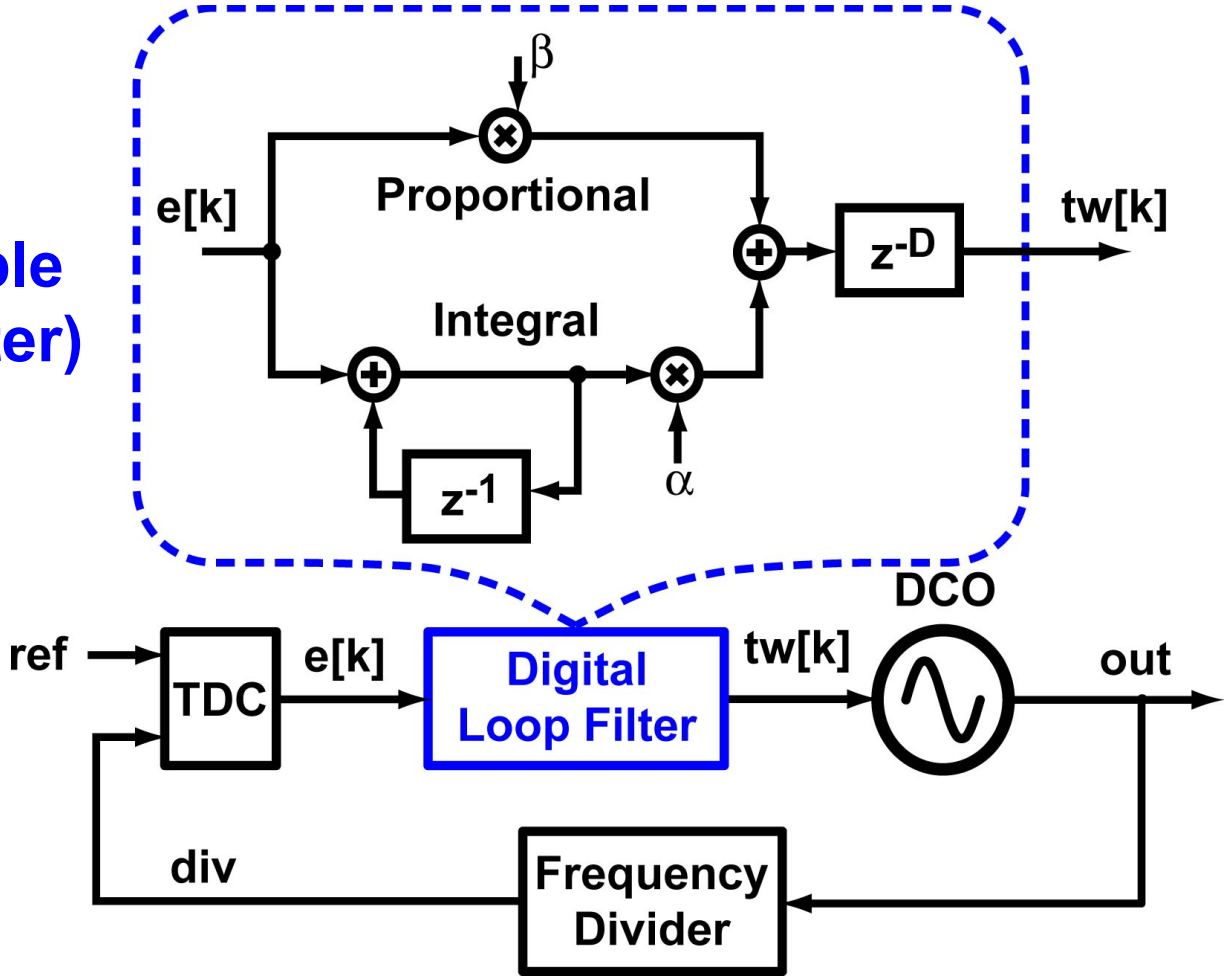
Digital Loop Filter

Example (FIR filter)



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Integer-N Frequency Synthesis

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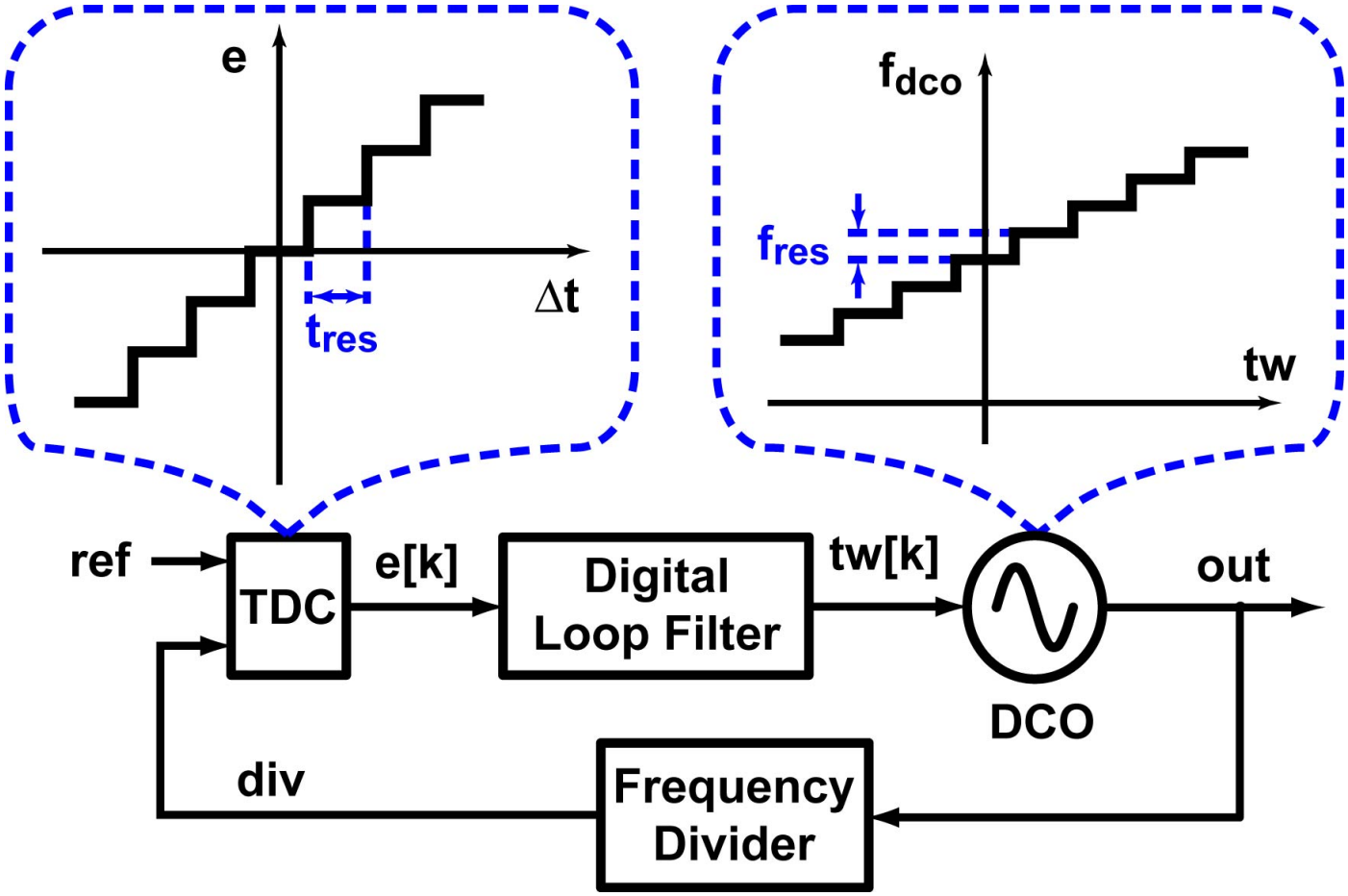
TDC and DCO Quantization

Mid-tread Quantizer



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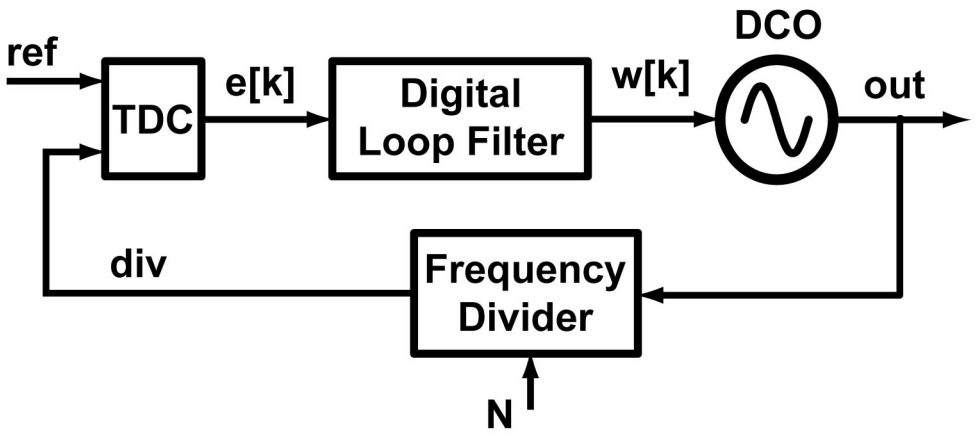
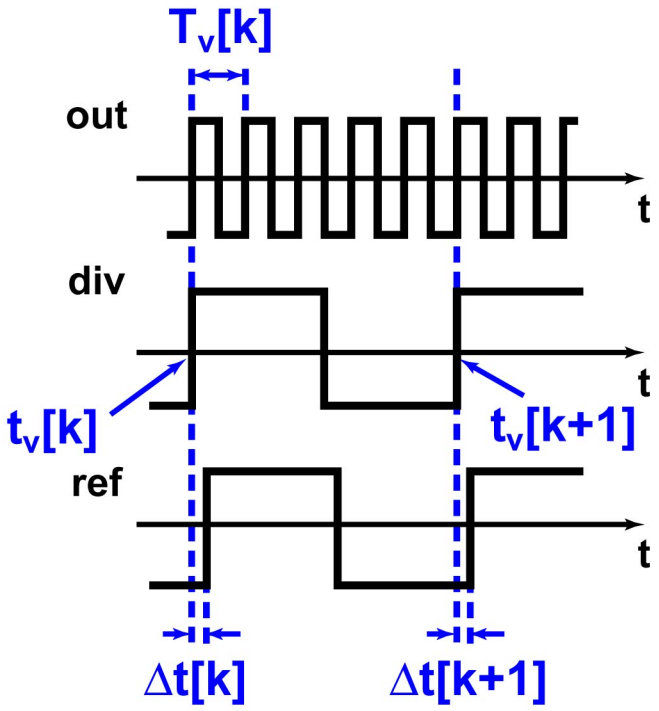
Deriving a Model at Reference Rate





$$T_v[k] = T_{v0} + K_T \cdot w[k]$$

$$t_v[k+1] - t_v[k] = N \cdot T_v[k] = NT_{v0} - NK_T \cdot w[k]$$

Discrete-Time Integrator

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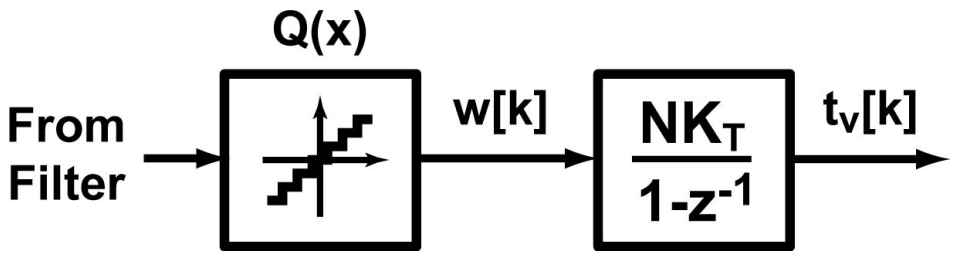
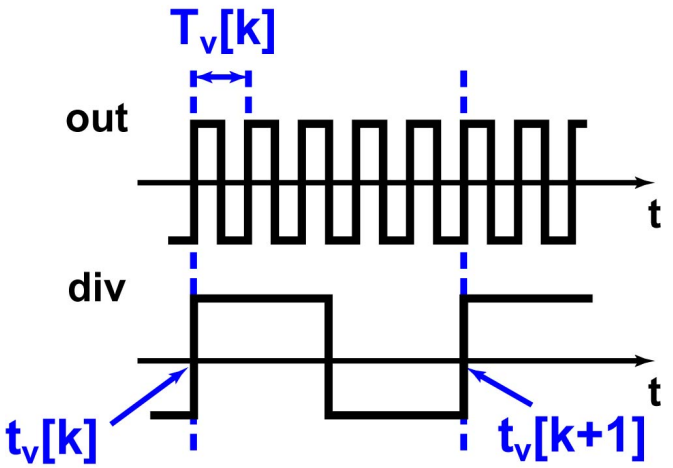
DCO and Divider Model at Reference Rate





Example:

$f_{v0} = 3.6$ GHz

$T_{v0} = f_{v0}^{-1} = 278$ ps

$f_{res} = 12$ kHz/unit cap

$K_T = T_{v0}^2 f_{res} = 0.92$ fs/unit cap (DCO resolution)

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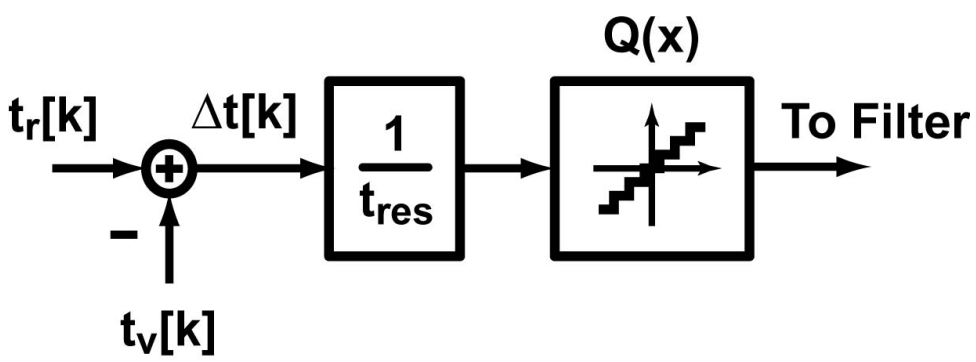
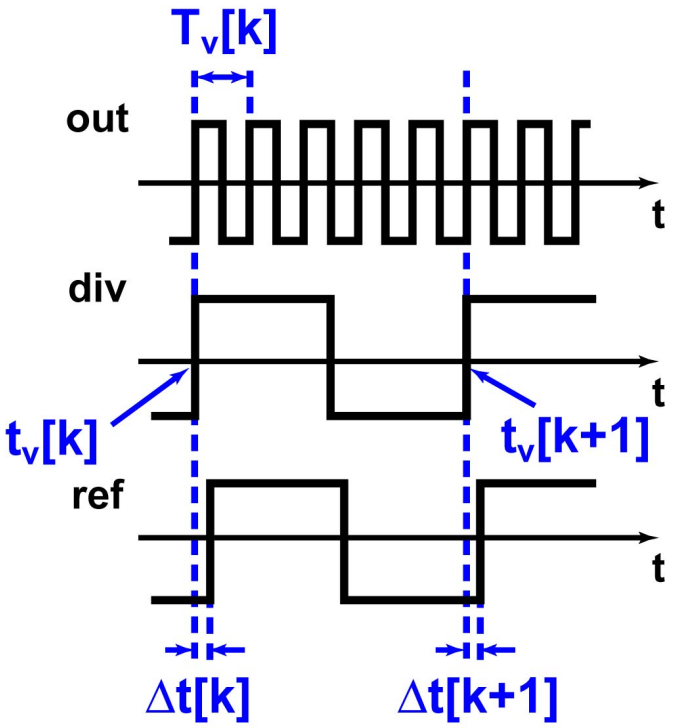
TDC Model





Example:

$t_{res} = 20$ ps (TDC resolution)

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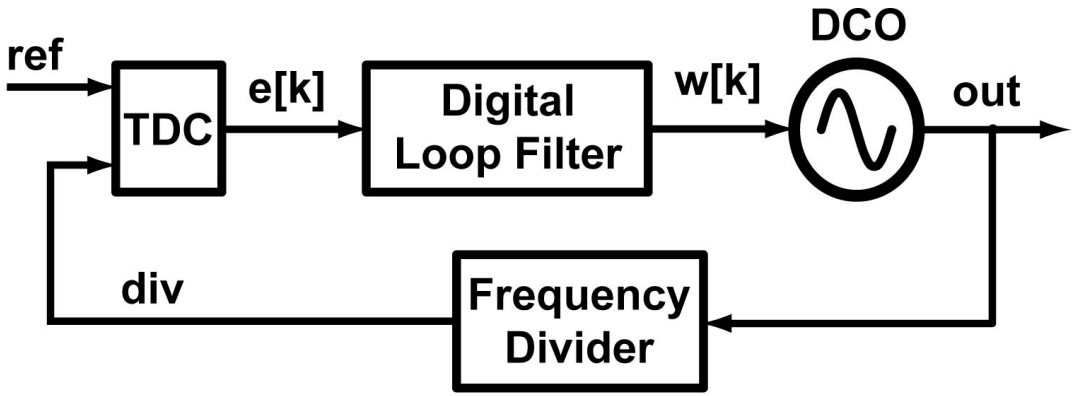
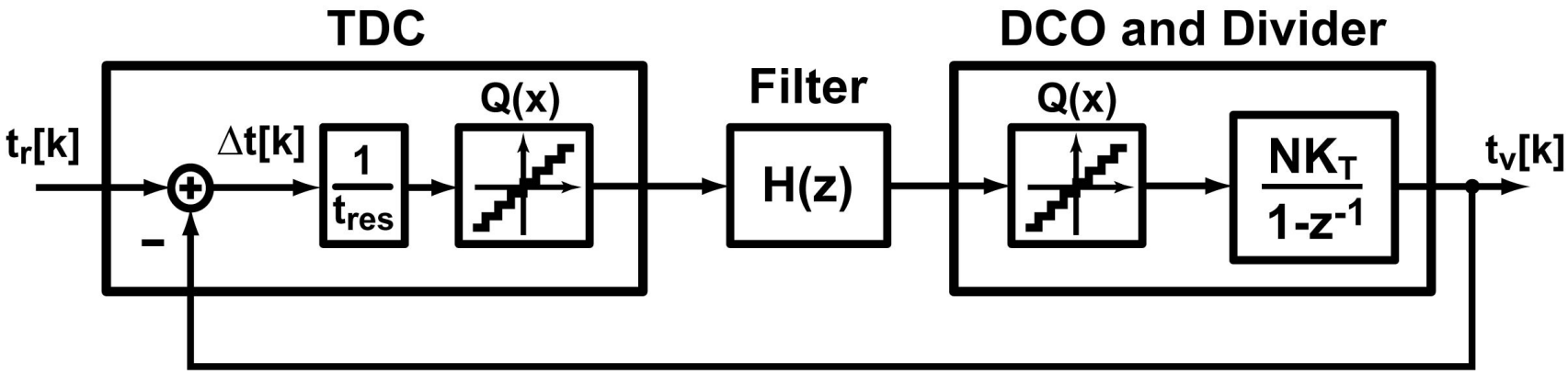
DPLL Model





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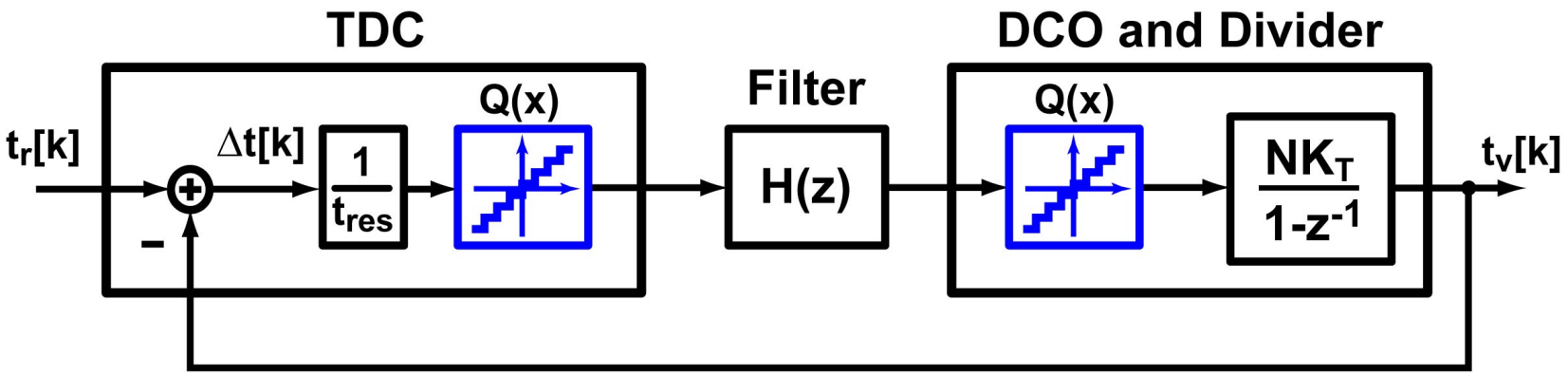
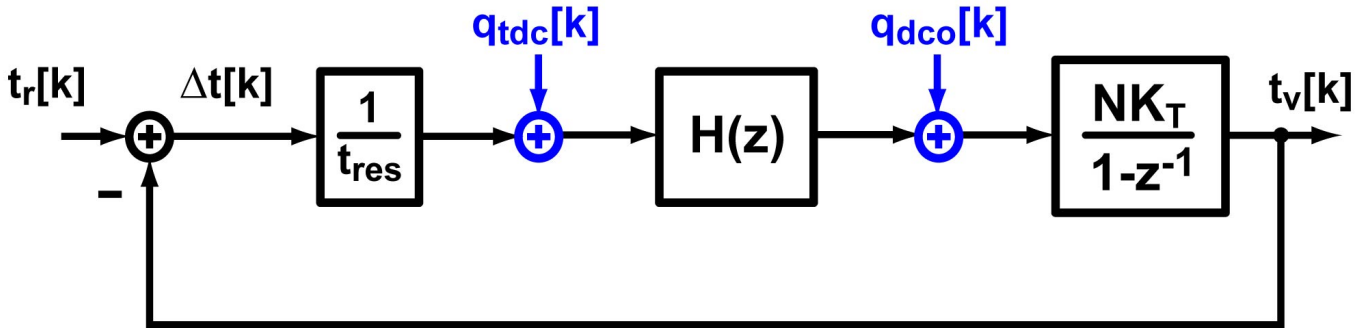
Conventional Simplification for Analysis



Linearized Model:



Under what condition the system acts as a linear one?

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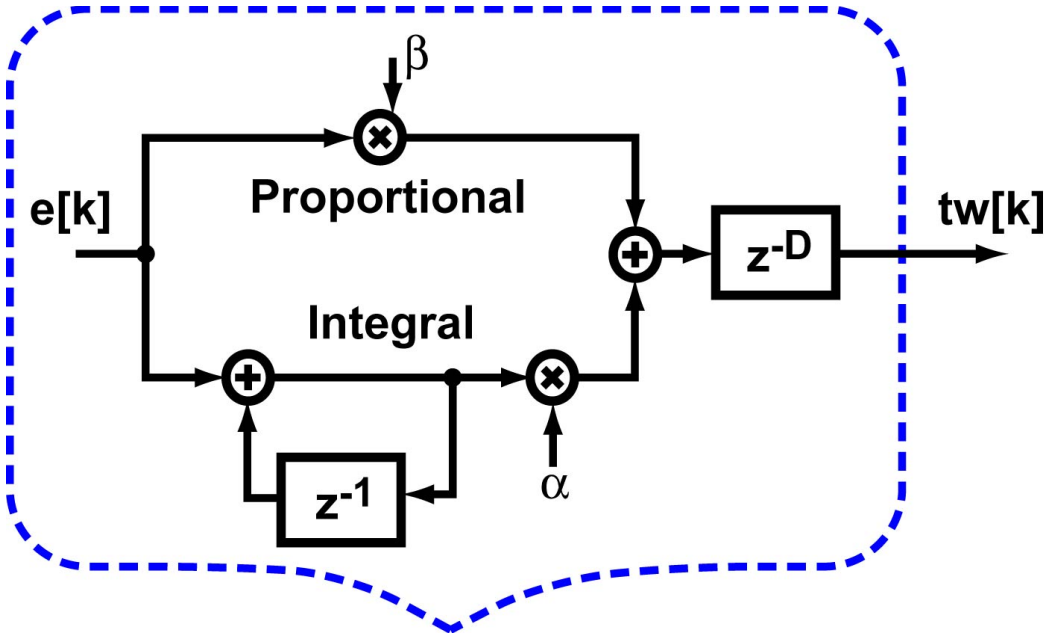
Loop Filter for a Second-Order DPLL



$$H(z) = \left(\frac{\alpha}{1 - z^{-1}} + \beta \right) \cdot z^{-D} = K \cdot \frac{1 - b_1 z^{-1}}{1 + z^{-1}} \cdot z^{-D}$$

where $K = \alpha + \beta, \quad b_1 = \dfrac{\beta}{\alpha + \beta}$

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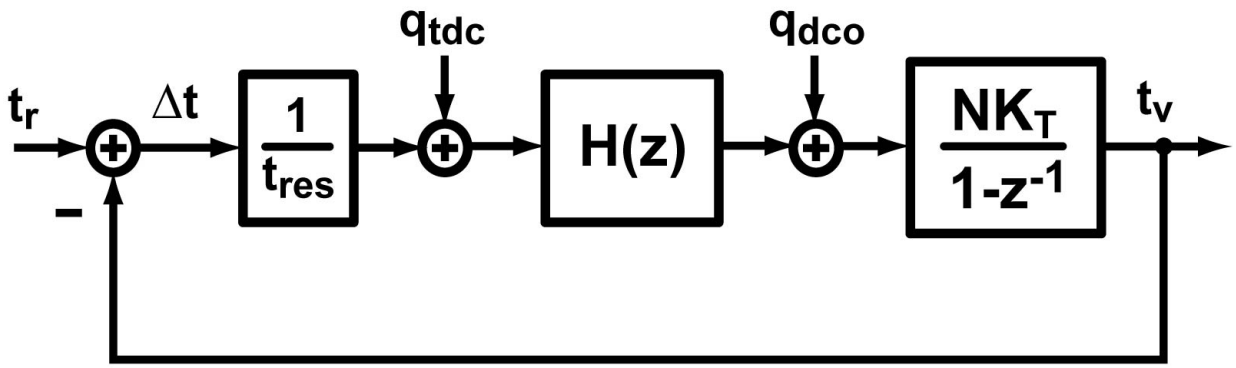
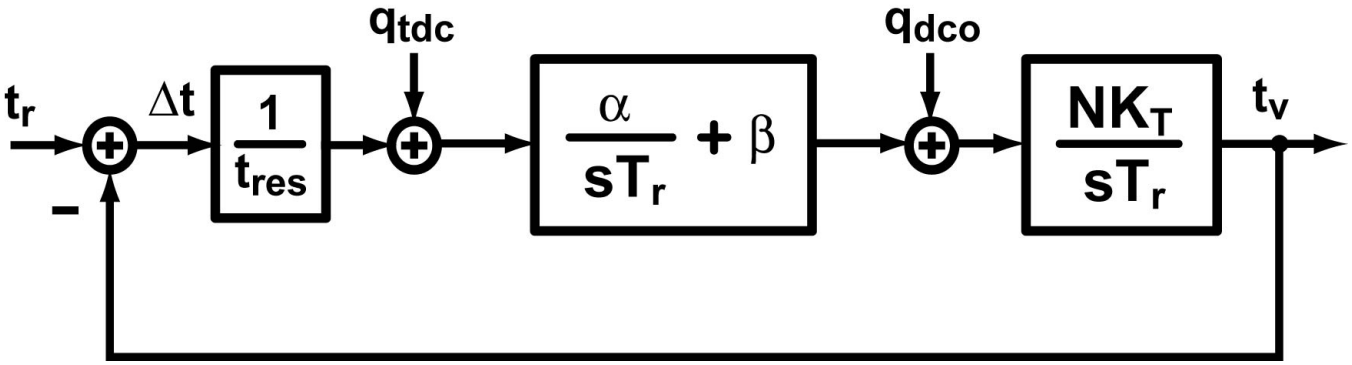
Second Simplification for Analysis



Narrowband approximation

$$z^{-1} = e^{-sT_r} \cong 1 - sT_r$$



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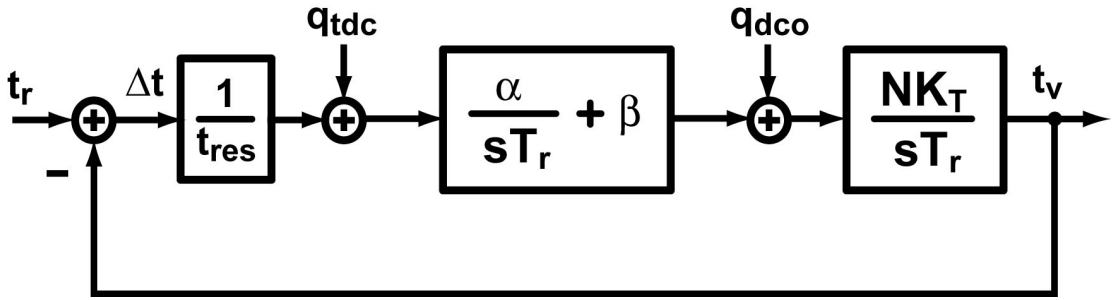
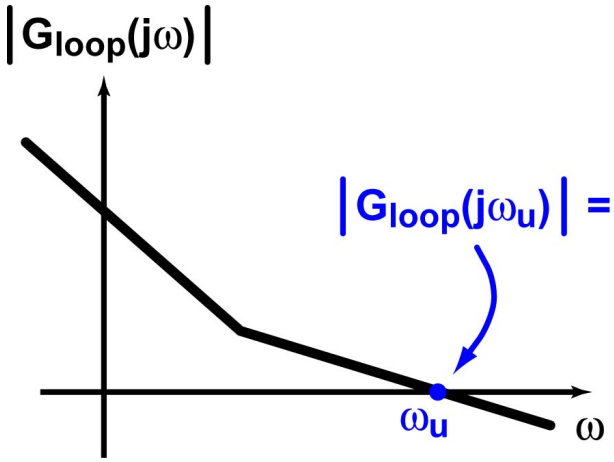
Loop Bandwidth



$$G_{loop}(s) = \left(1 + \frac{\alpha}{\beta}\frac{1}{sT_r}\right) \cdot \frac{N\beta K_T}{sT_r t_{res}}$$



$$\omega_u \cong \frac{N\beta K_T}{T_r t_{res}}, \qquad \omega_z = \frac{\alpha}{\beta} \cdot \frac{1}{T_r}$$

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Narrow Bandwidth Design

Example:

$f_{v0} = 3.6$ GHz

$f_r = 1/T_r = 50$ MHz $\Rightarrow$ $N = 72$

$K_T = 0.92$ fs/unit cap (DCO resolution)

$t_{res} = 20$ ps (TDC resolution)

$f_u = 100$ kHz, $f_z = 10$ kHz

$$\beta = \frac{\omega_u T_r t_{res}}{N K_T} = 4.5, \qquad \alpha = \beta \cdot \omega_z T_r = 5.6 \cdot 10^{-3}$$

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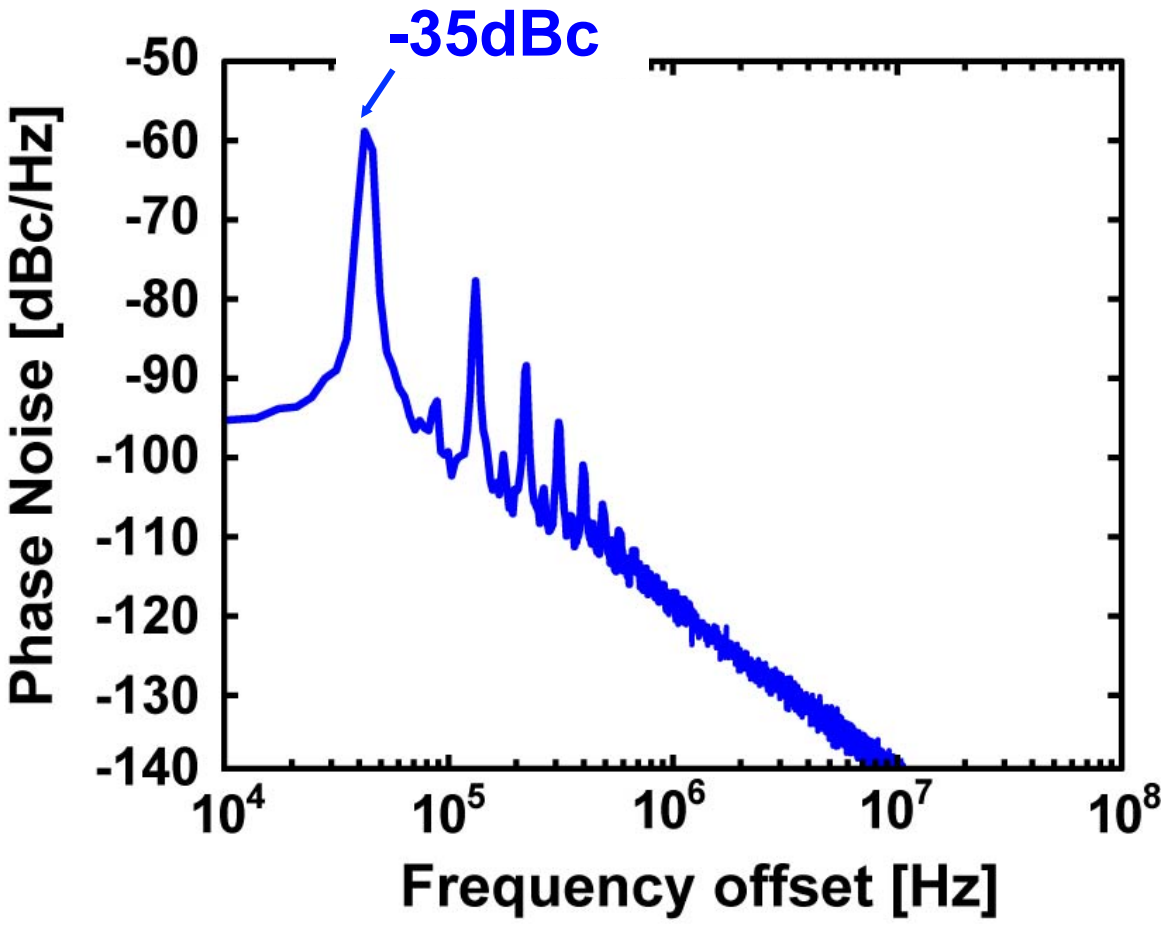
Simulated Spectrum (No Random Noise)



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Adding Random Noise

- With negligible random noise, quantization noise $q_{tdc}[k]$ is periodic
- Adding random noise of same variance, $q_{tdc}[k]$ becomes a white random process
- Output in-band noise is approximated by:

$$\mathcal{L}_{q,tdc} = N^2 \cdot \left(2\pi f_r\right)^2 \cdot \frac{t_{res}^2}{12 f_r} = \frac{2\pi^2}{3} \cdot N^2 t_{res}^2 f_r$$

$$\mathcal{L}_{q,tdc} = -92 \text{ dBc/Hz}$$

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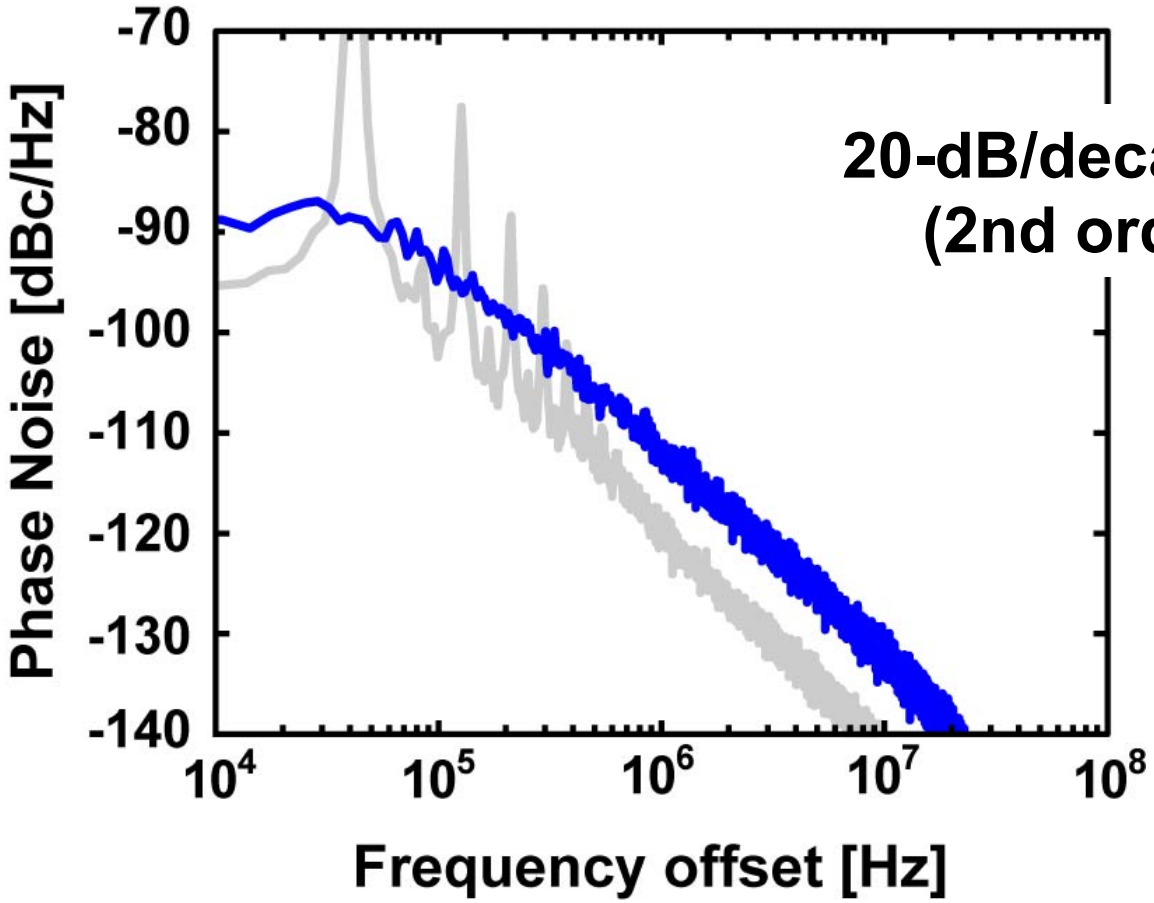
Simulation of Second-Order DPLL



20-dB/decade roll-off (2nd order PLL)

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Wideband Design

(From slide #19)

$$\omega_u \cong \frac{N\beta K_T}{T_r t_{res}}$$

- **Wider BW** (relative to $1/T_r$) would require either to **increase** βK_T or **reduce** t_{res}
- **Larger** βK_T (DCO frequency granularity) increases truncation noise at DCO input
- Wider BW at **same** t_{res} (same quantization noise level) may violate phase-noise mask

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Wideband Design Example

- **In conventional DPLL, wider bandwidth demands for better TDC resolution**

Example:

$t_{res} = 2$ ps ➡ $\mathcal{L}_{q,tdc} = -115$ dBc/Hz

$f_u = 1$ MHz, $f_z = 100$ kHz

⬇

$$\beta = \frac{\omega_u T_r t_{res}}{N K_T} = 4.5, \qquad \alpha = \beta \cdot \omega_z T_r = 5.6 \cdot 10^{-3}$$

Same filter coefficients

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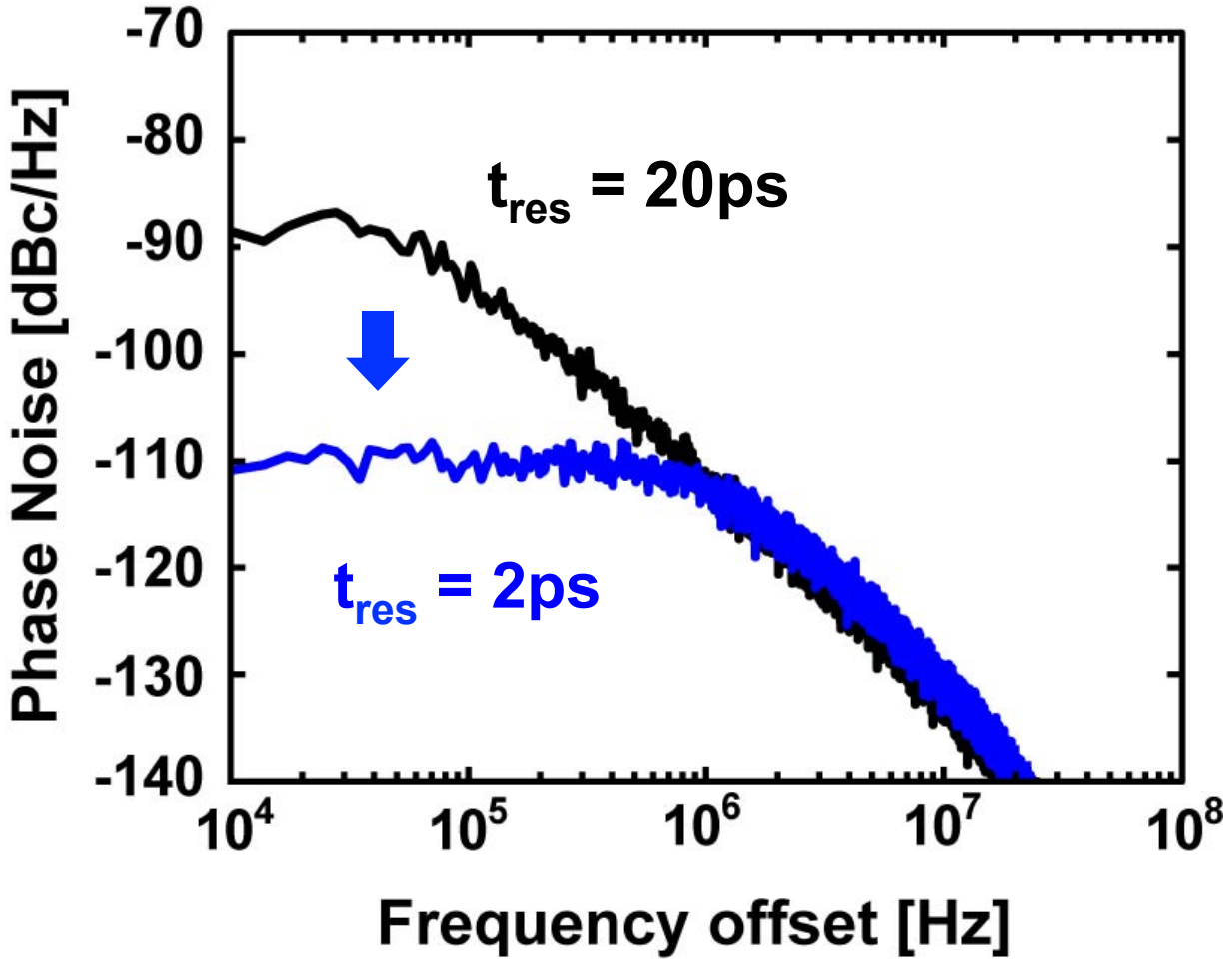
Simulation of Wideband Second-Order DPLL



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Conclusion

- In the conventional DPLL scheme, in-band noise is limited by TDC resolution
- Typically, if the system requirements demand for wider PLL bandwidth, TDC resolution must be improved
- In wireless applications, ps or sub-ps TDC resolution may be required

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Integer-N Frequency Synthesis with Bang-Bang TDC

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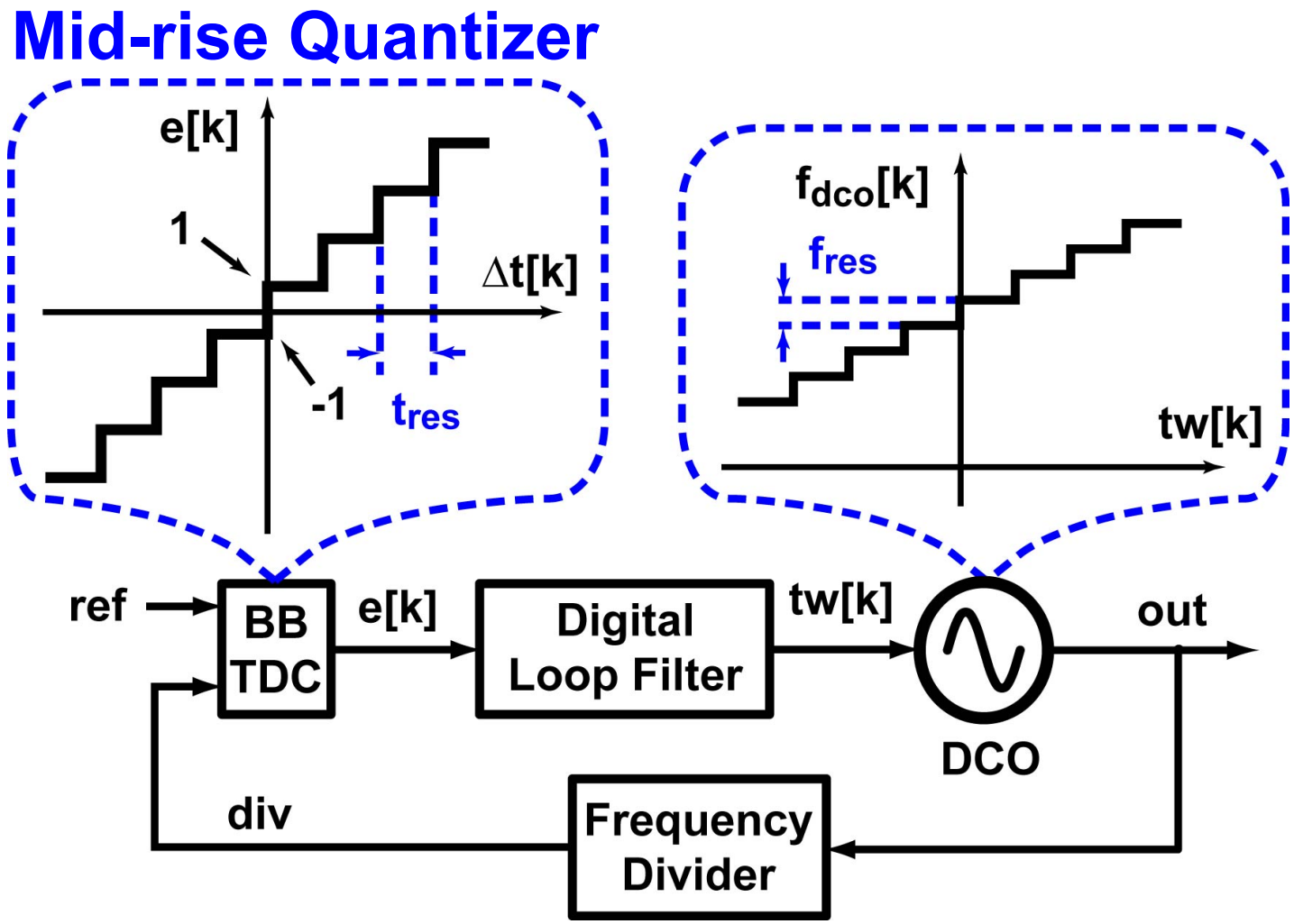
Mid-rise TDC or Bang-Bang Phase Detect



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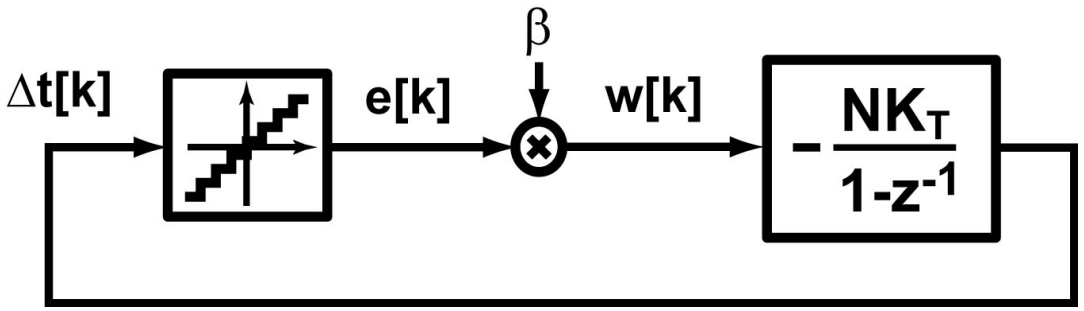
Model of First-Order DPLL with Quantization

- **Proportional filter (gain β) and no latency**
- **No truncation at DCO input**
- **No random noise**



$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$

$$\text{where} \quad T_0 = NT_{v0} - T_r$$

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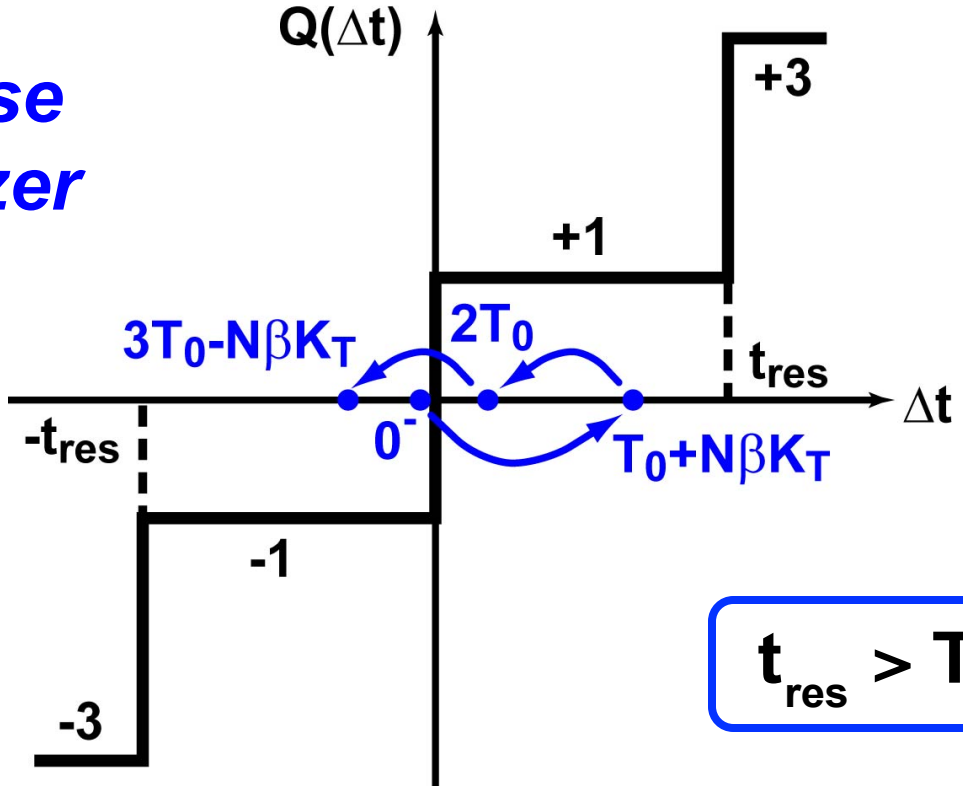
Behavior of 1st-Order Bang-Bang DPLL

$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$

Mid-Rise Quantizer



$$t_{res} > T_0 + N\beta K_T$$

[For reference, see N. Da Dalt, *TCAS-I*, 2005]

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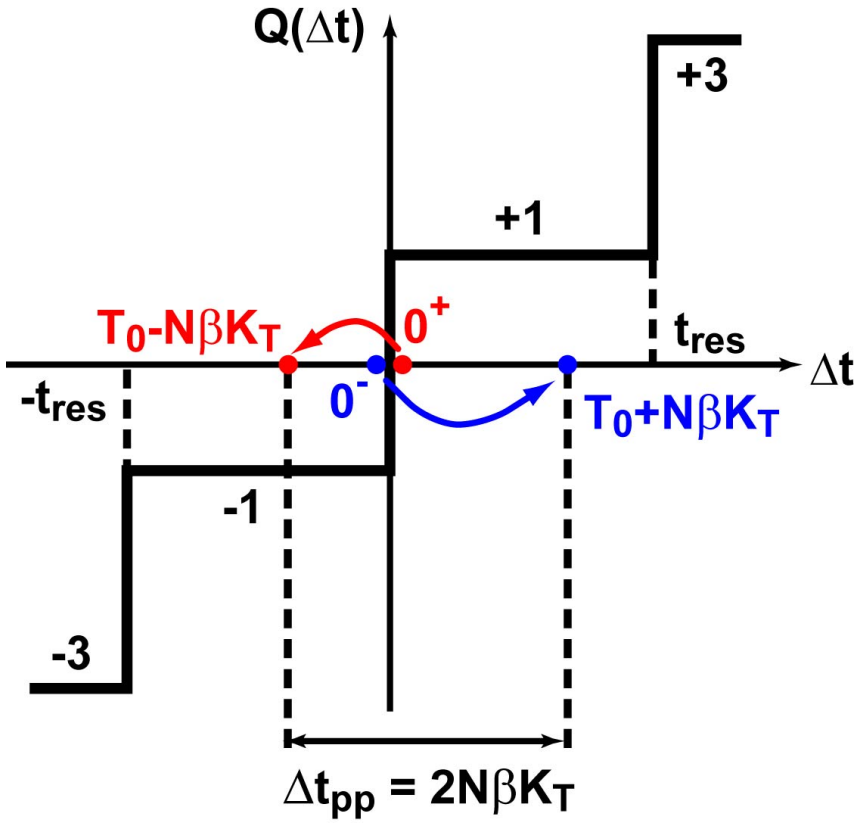
1st-Order Bang-Bang DPLL (Continued)

$$\Delta t[k+1] - \Delta t[k] = T_0 - N\beta K_T \cdot Q\left(\Delta t[k]/t_{res}\right)$$



Irrational ($T_0/N\beta K_T$)

⇓

p(Δt) is uniform

⇓

$$\sigma_{\Delta t} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{N\beta K_T}{\sqrt{3}}$$

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2nd-Order Bang-Bang DPLL

- PI digital loop filter with latency D
- No truncation at DCO input
- No random noise

Quantization-induced Jitter

$$\sigma_{\Delta t} = \frac{\Delta t_{pp}}{\sqrt{12}} = \frac{(1+D)}{\sqrt{3}} \cdot N\beta K_T$$

[N. Da Dalt, *TCAS-I*, 2005]

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Quantization Noise in Bang-Bang DPLL

(From previous slide)

$$\sigma_{\Delta t} = \frac{(1+D)}{\sqrt{3}} \cdot N\beta K_T$$

- **Loop quantization no more limited by t_{res} (TDC), but only by βK_T (DCO granularity)**
- **Quantization increases as filter latency D (number of clock cycles)**

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Example of 2nd-Order Bang-Bang DPLL

Example:

$f_{v0} = 3.6$ GHz

$K_T = 0.92$ fs/unit cap

$f_r = 50$ MHz $\Rightarrow$ $N = 72$

$t_{res} = 20$ ps

$\beta = 4.5, \quad \alpha = 5.6 \cdot 10^{-3}, \quad D = 1$

$$\sigma_{\Delta t} = \frac{(1+D)}{\sqrt{3}} \cdot N\beta K_T = 344 \text{ fs}_{rms}$$

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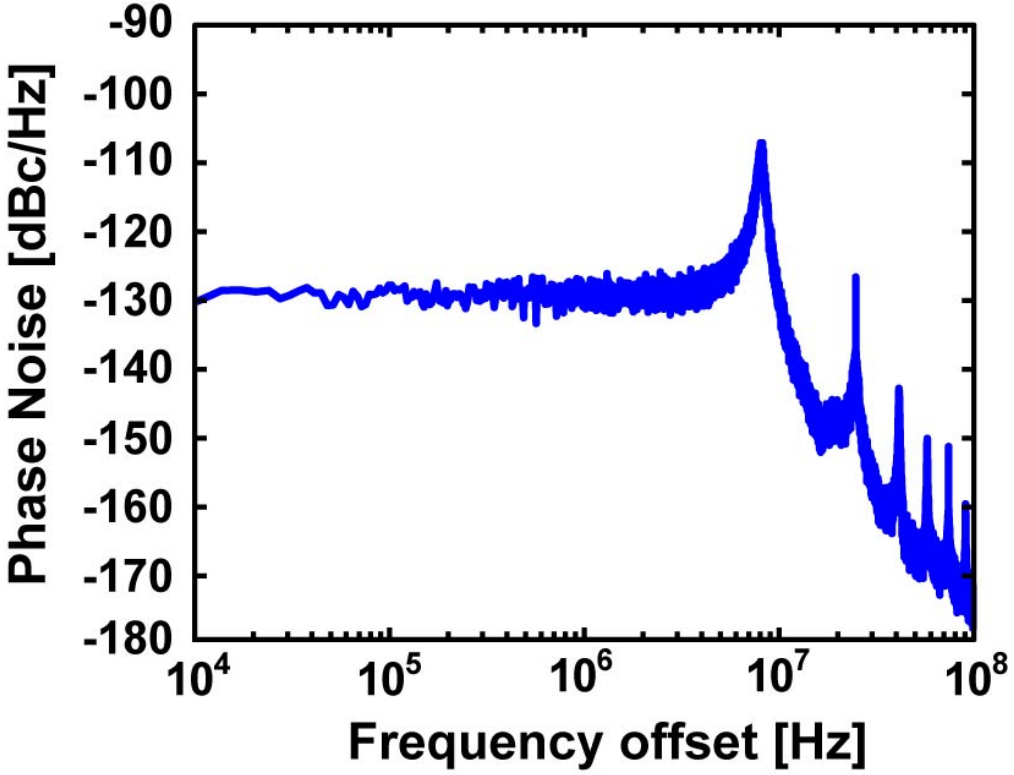
Simulation (No Random Noise)



- **The system converges to a limit cycle**
- **Quantization noise is periodic**

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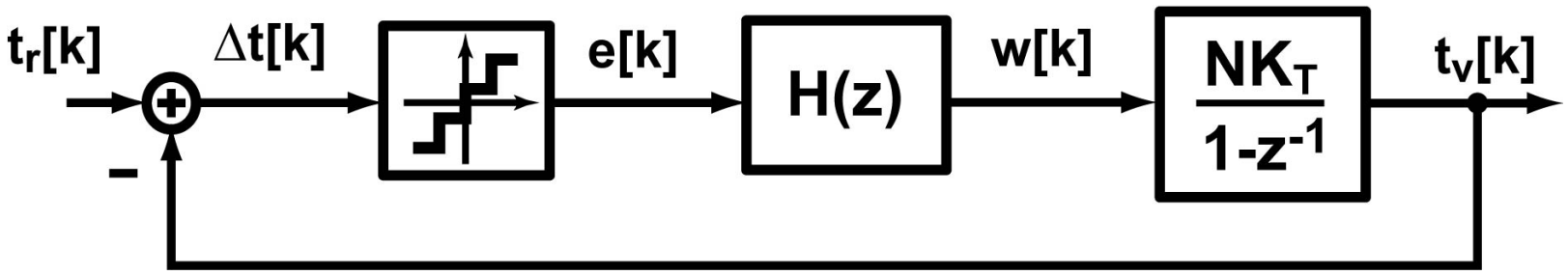
Adding Random Noise



- **Periodicity can be broken only relying on true random noise**
- **If random noise deviation is lower than t_{res}, e[k] will be ±1**
- **The average of e[k] will be proportional to Δt as in a linear phase detector**

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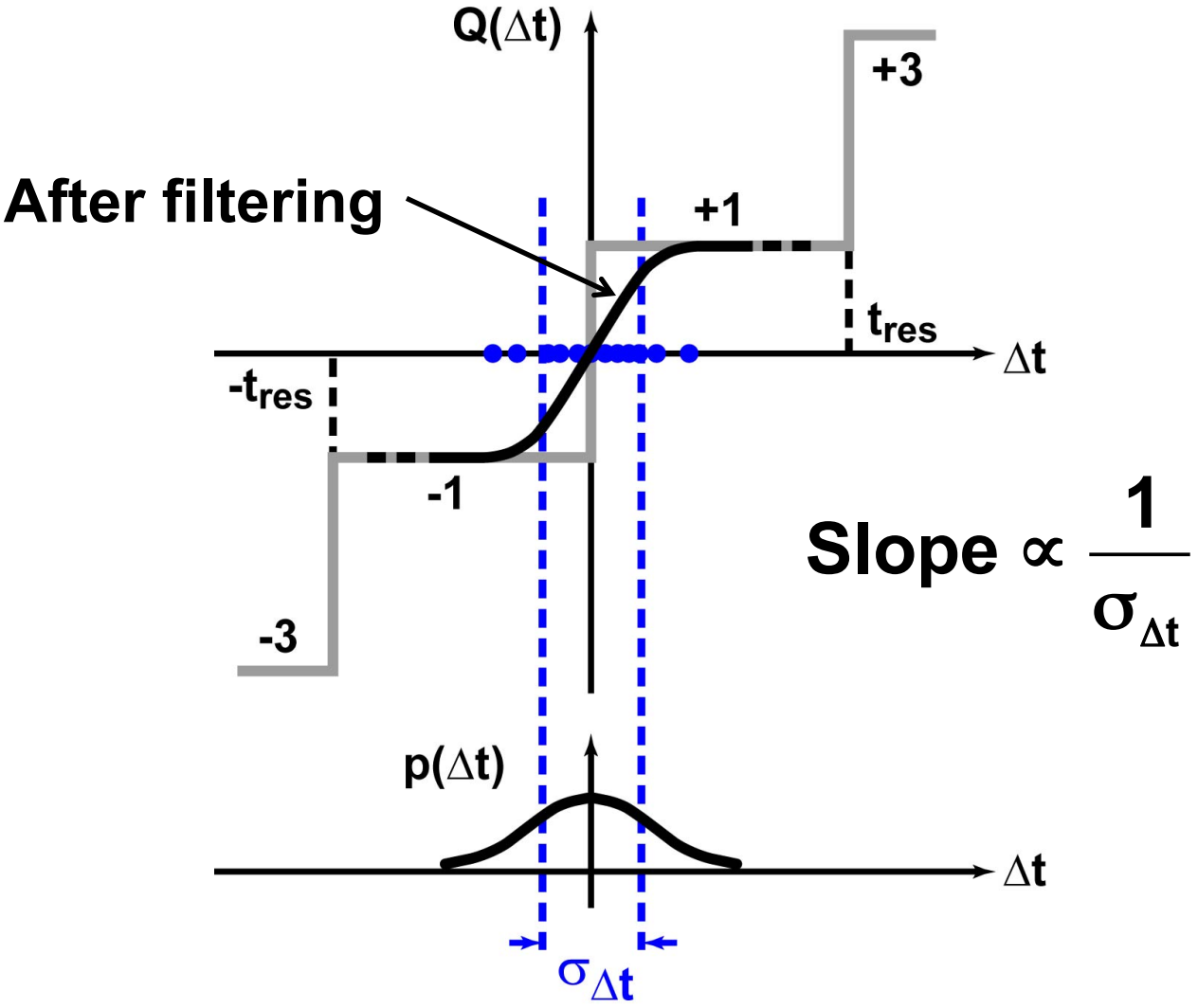
Phase Detect Characteristic is Smoothed



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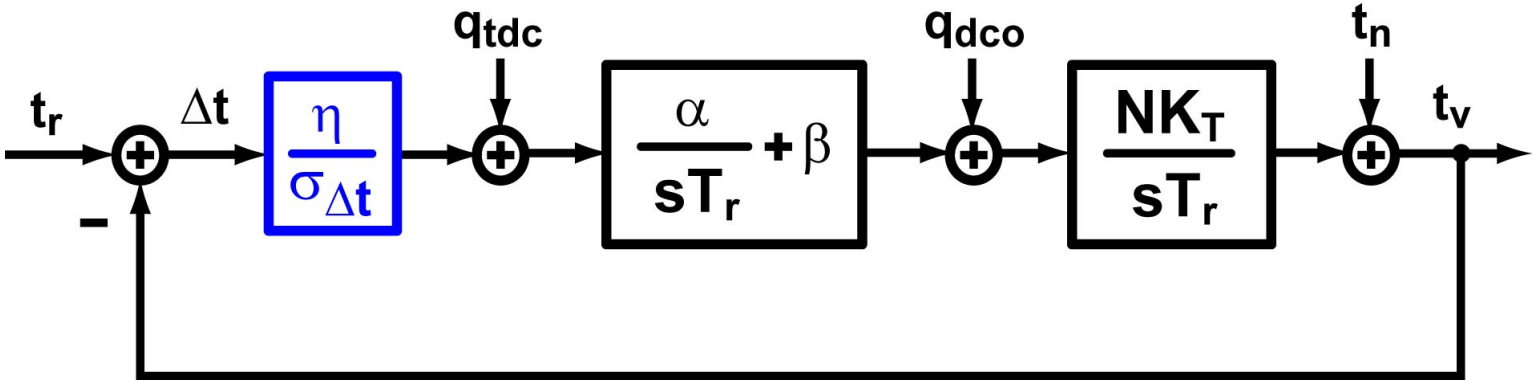
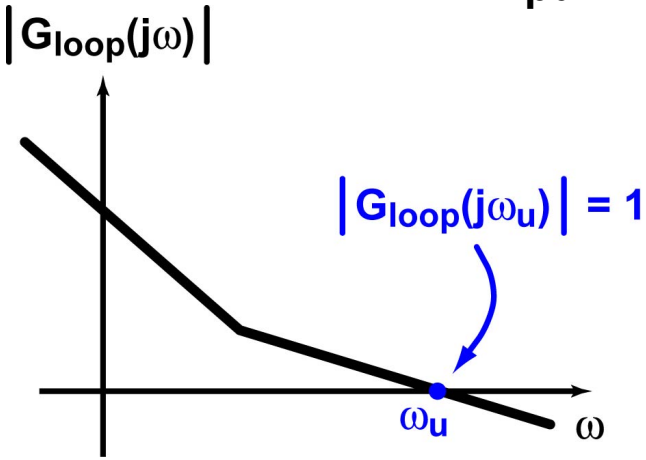
Model Simplification: Linearization



$$K_{pd} = \frac{\eta}{\sigma_{\Delta t}}, \qquad \text{where} \quad \eta = \sqrt{\frac{2}{\pi}}$$



$$\omega_u \cong \frac{\eta N \beta K_T}{T_r \sigma_{\Delta t}}, \qquad \omega_z = \frac{\alpha}{\beta} \cdot \frac{1}{T_r}$$

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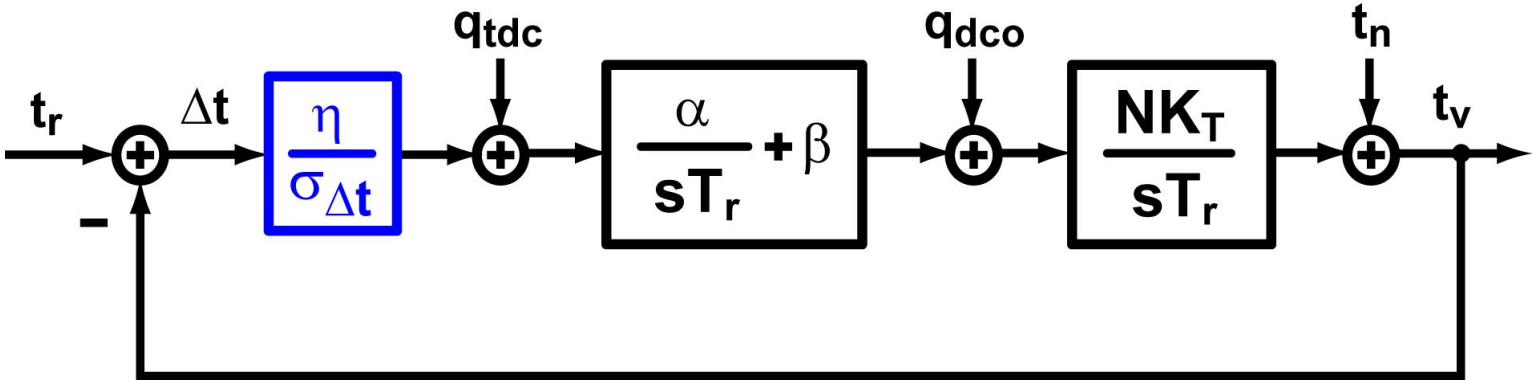
Computation of Random Noise



$$\sigma_{\Delta t}^2 = 2 \cdot \int_0^{\infty} \frac{S_{t_r}(f) + S_{t_n}(f)}{\left|1 + G_{loop}(f)\right|^2} df$$

$$\mathcal{L}(f) = (2\pi f_{v0})^2 \cdot S_{t_n}(f)$$

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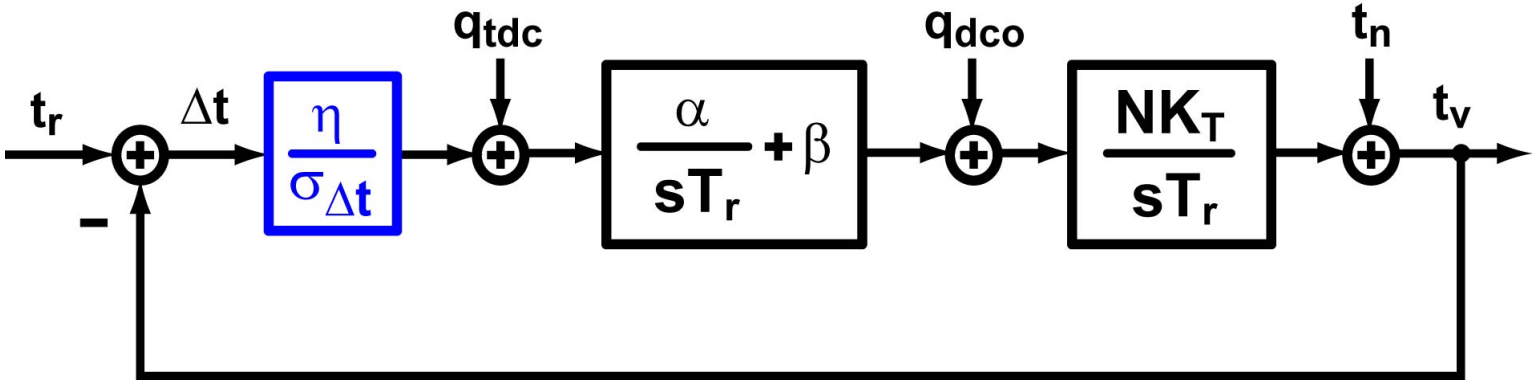
Adding White Noise



$$S_{t_r}(f) = \frac{\sigma_{t_r}^2}{f_r}, \qquad S_{t_n}(f) = 0$$

$$f_{bw} << f_r$$

$$\sigma_{\Delta t}^2 = 2 \cdot \int_0^{\infty} \frac{S_{t_r}(f) + S_{t_n}(f)}{\left|1 + G_{loop}(f)\right|^2} df \cong \sigma_{t_r}^2$$

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Bang-Bang DPLL with Random Noise

Random-noise-induced Jitter

$$\sigma_{\Delta t} \cong \sigma_{t_r}$$

must be greater or equal to quantization-induced jitter

$$\sigma_{t_r} \geq \frac{(1+D)}{\sqrt{3}} \cdot N\beta K_T \quad \Rightarrow \quad \beta K_T \leq \frac{\sqrt{3}}{N(1+D)} \cdot \sigma_{t_r}$$

[M. Zanuso et al., TCAS-II, 2009]

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Design Example

$$\mathcal{L}(f) = N^2 (2\pi f_r)^2 \cdot \frac{\sigma_{t_r}^2}{f_r} = 4\pi^2 N^2 f_r \sigma_{t_r}^2$$

Example:

$\mathcal{L}(f) = -118\,\text{dBc/Hz}$ **White reference noise**

$f_{v0} = 3.6\,\text{GHz}, \quad \sigma_{t_r} = 344\,\text{fs}_{\text{rms}}$

$\Downarrow \quad D = 1, \quad N = 72$

$$\beta K_T = \frac{\sqrt{3}}{N(1+D)} \cdot \sigma_{t_r} = 4.1\,\text{fs}$$

Maximum DCO granularity

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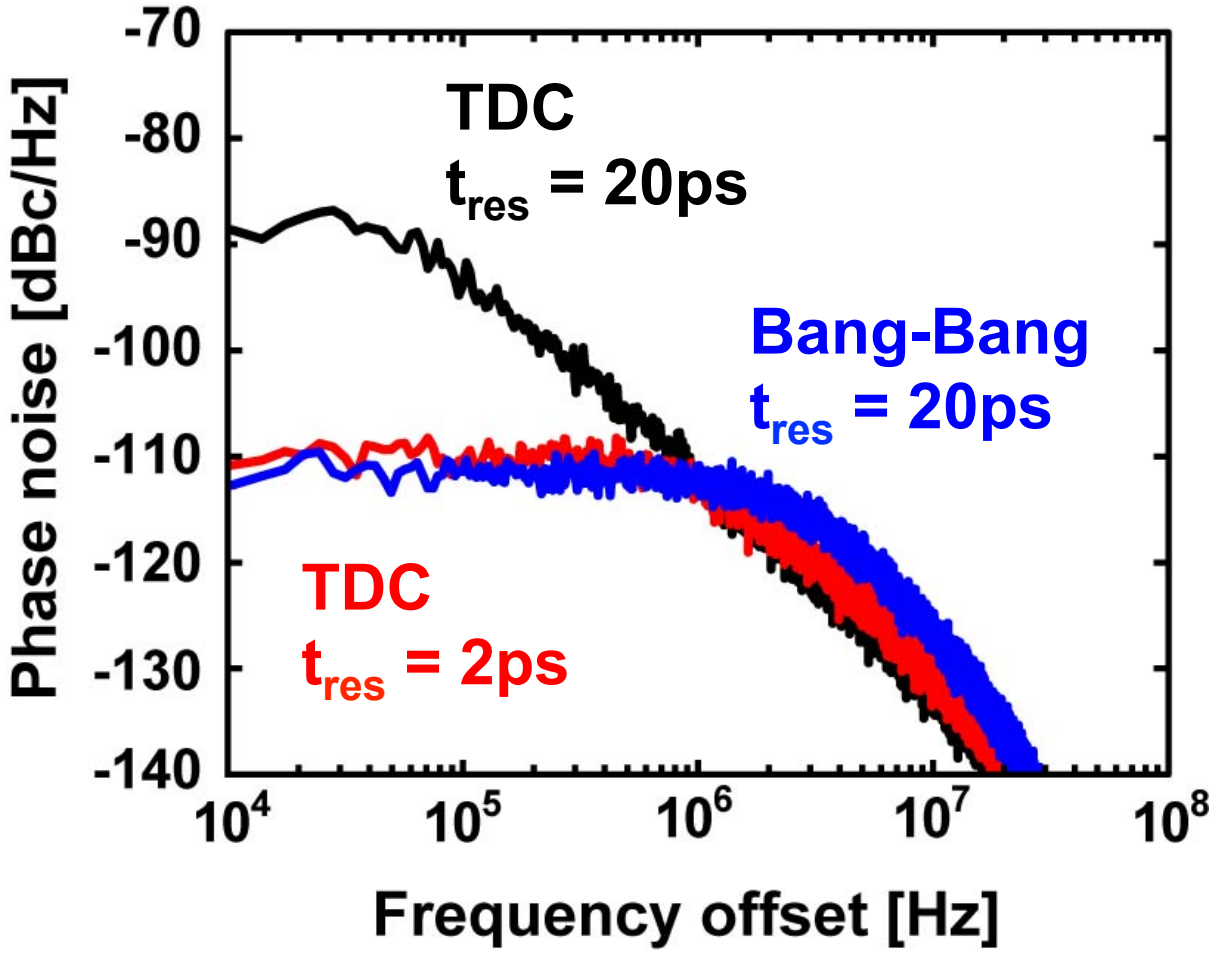
Simulation of 2nd-Order Bang-Bang DPLL



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Conclusions

- **DPLLs with bang-bang detectors (i.e. coarse TDCs with mid-rise quantization) allows same phase noise performance as those employing high-resolution TDCs**
- **Thus, at wide loop bandwidths, BBPLLs show much higher efficiency (noise/power trade-off) than conventional DPLLs**
- **In practice, fine resolution is only required to the DCO, which can be improved leveraging oversampling techniques**

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Fractional-N Frequency Synthesis

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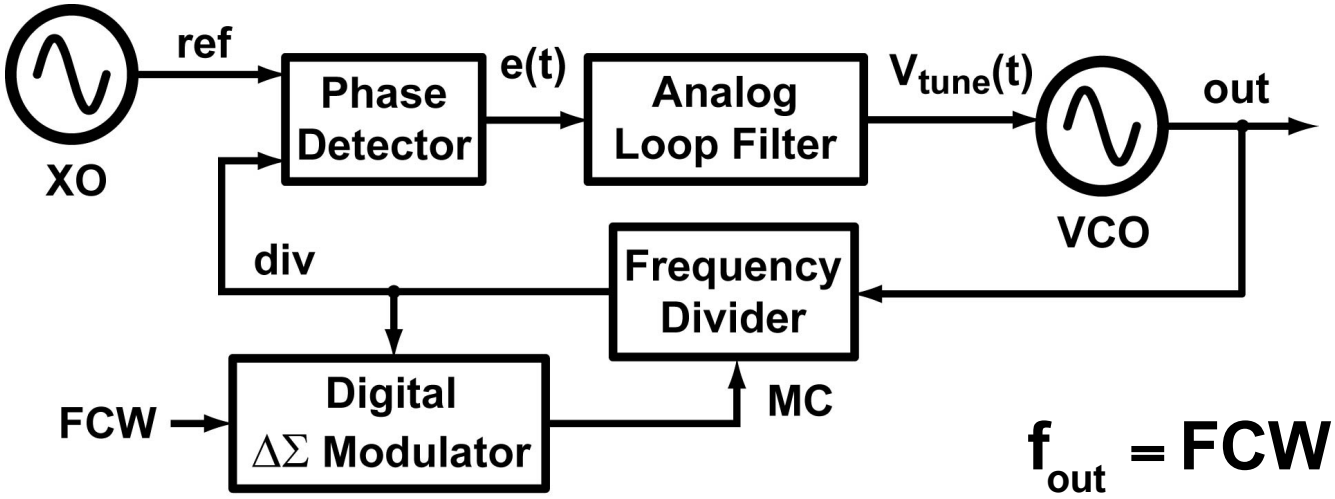
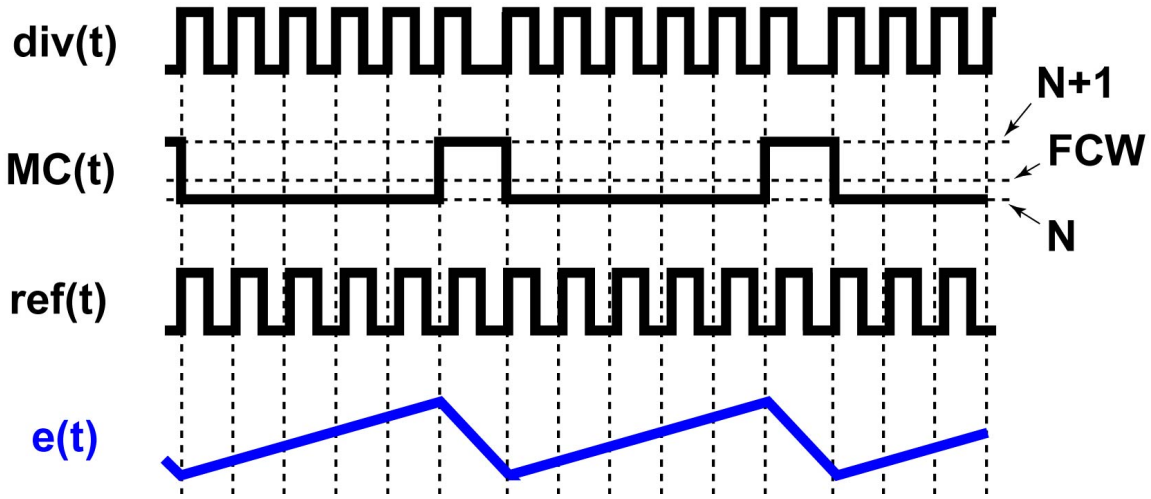
ΔΣ Fractional-N Analog PLL



$$f_{out} = FCW \cdot f_{ref}$$



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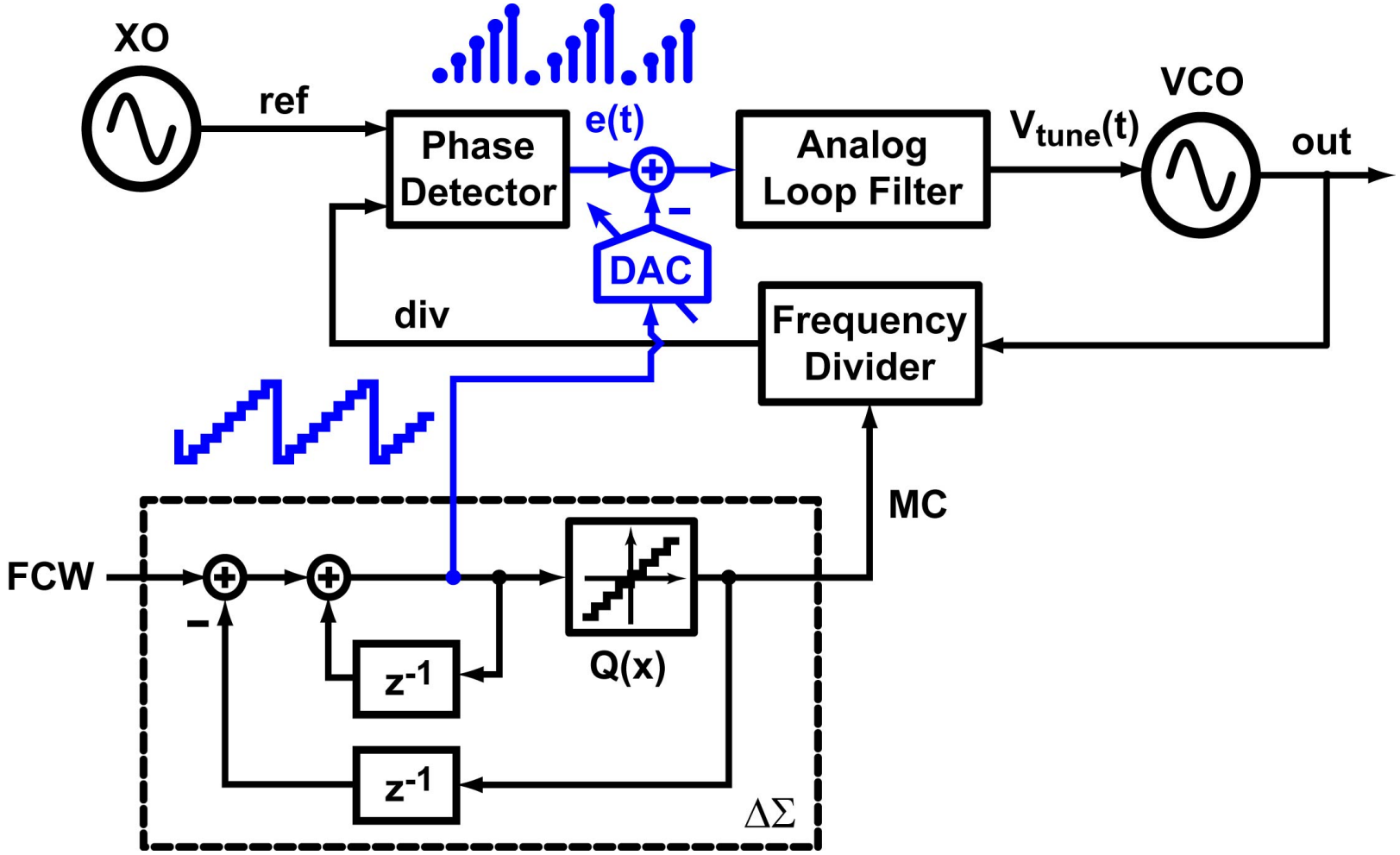
Digiphase Technique to Cancel ΔΣ Noise



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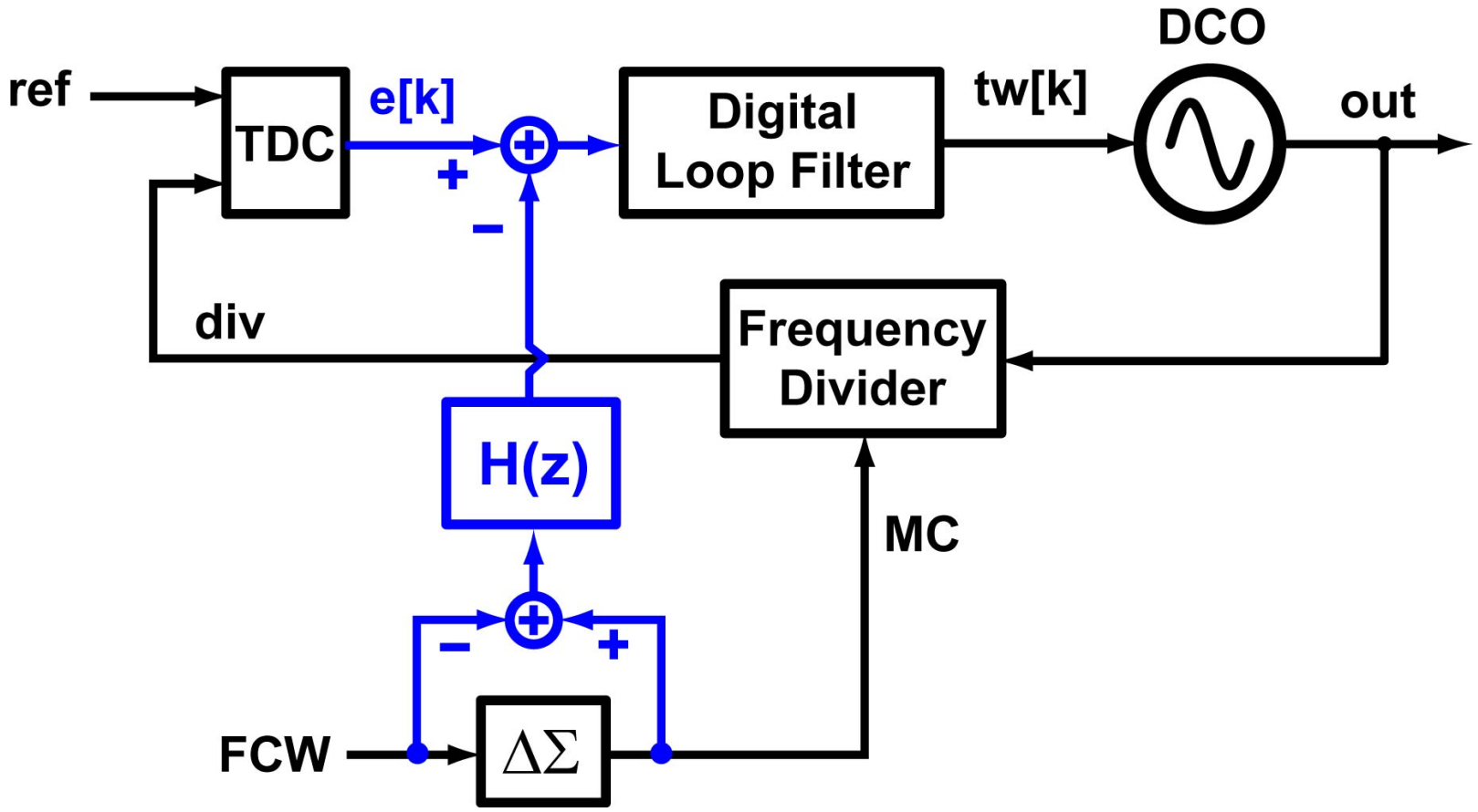
From Analog to Digital Fractional-N PLL



- How do we build an adaptive filter H(z)?

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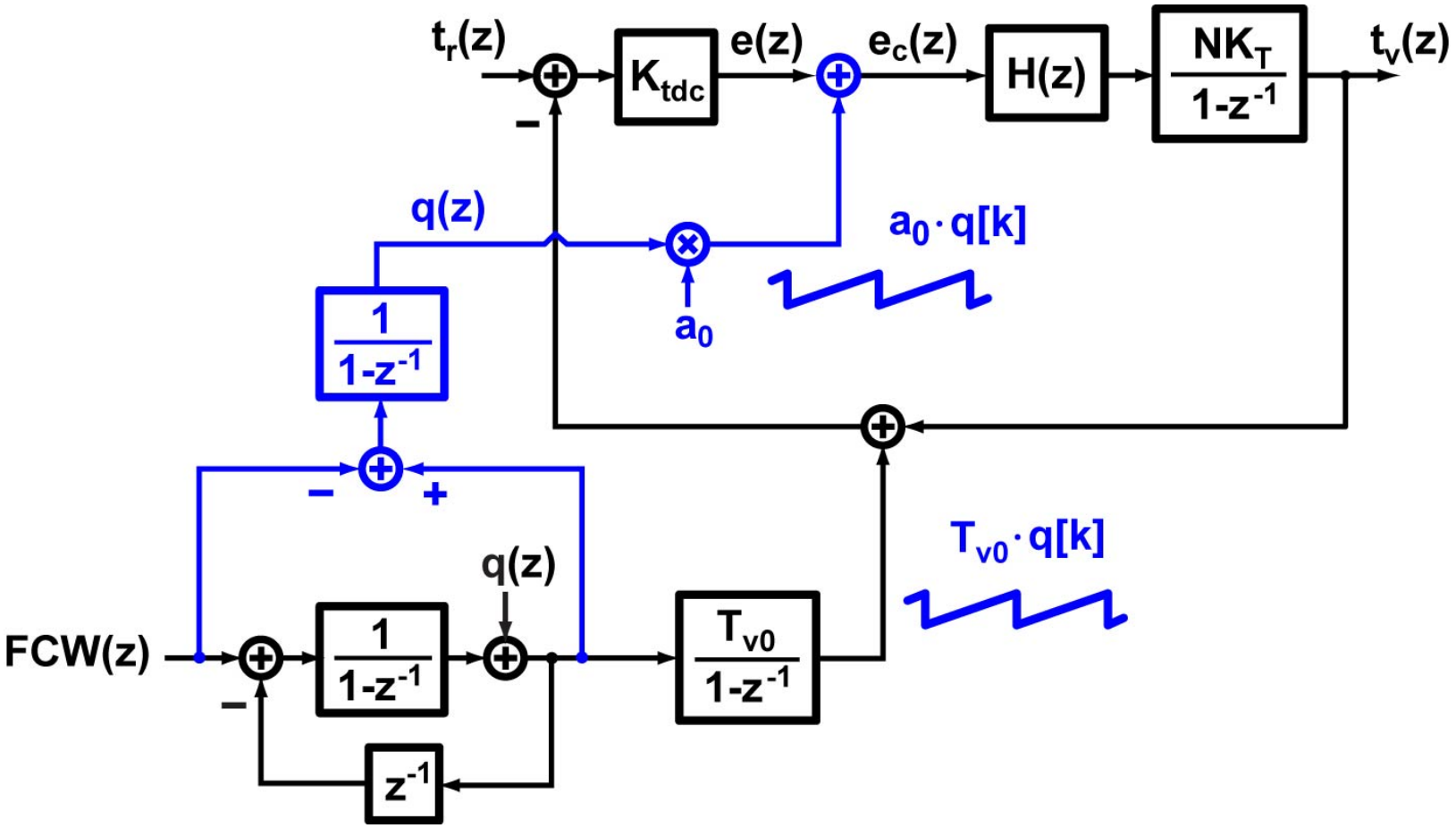
Time-Domain Model



- $q(z)$ is cancelled out if $a_0 = T_{v0}$

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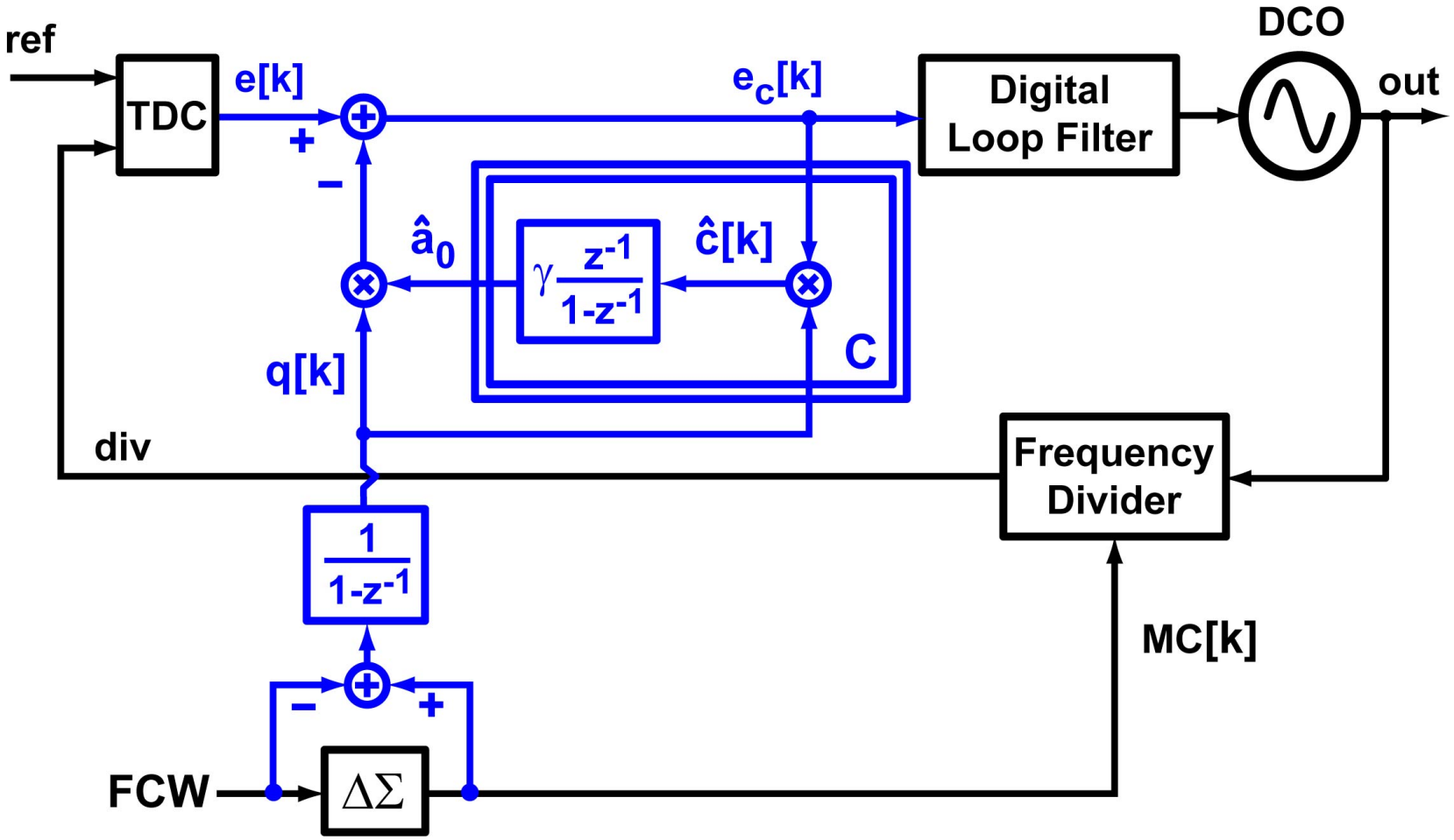
Automatic Background Regulation of a_0



[C.-M. Hsu et al., *ISSCC*, 2008]

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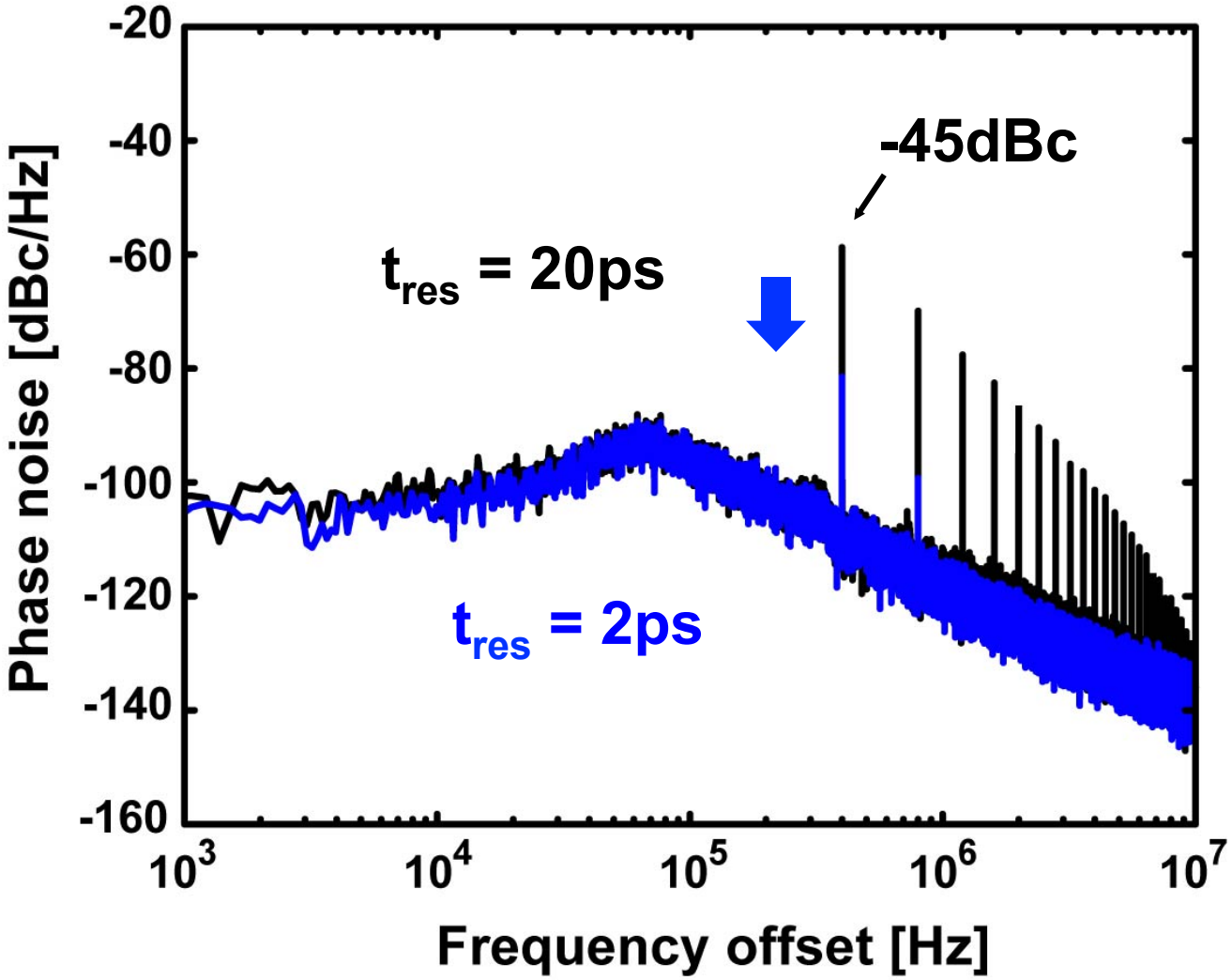
Effect of Limited TDC Resolution



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Conclusion

- Fractional-N DPLLs over their analog counterparts allow simple implementation of digiphase technique
- Automatic calibration of cancellation algorithm relies on digital adaptive filtering
- However, in the conventional DPLL scheme, the fractional spur level is limited by TDC resolution
- In wireless applications, a 10b-to-12b TDC is typically required

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Fractional-N Frequency Synthesis with Bang-Bang TDC

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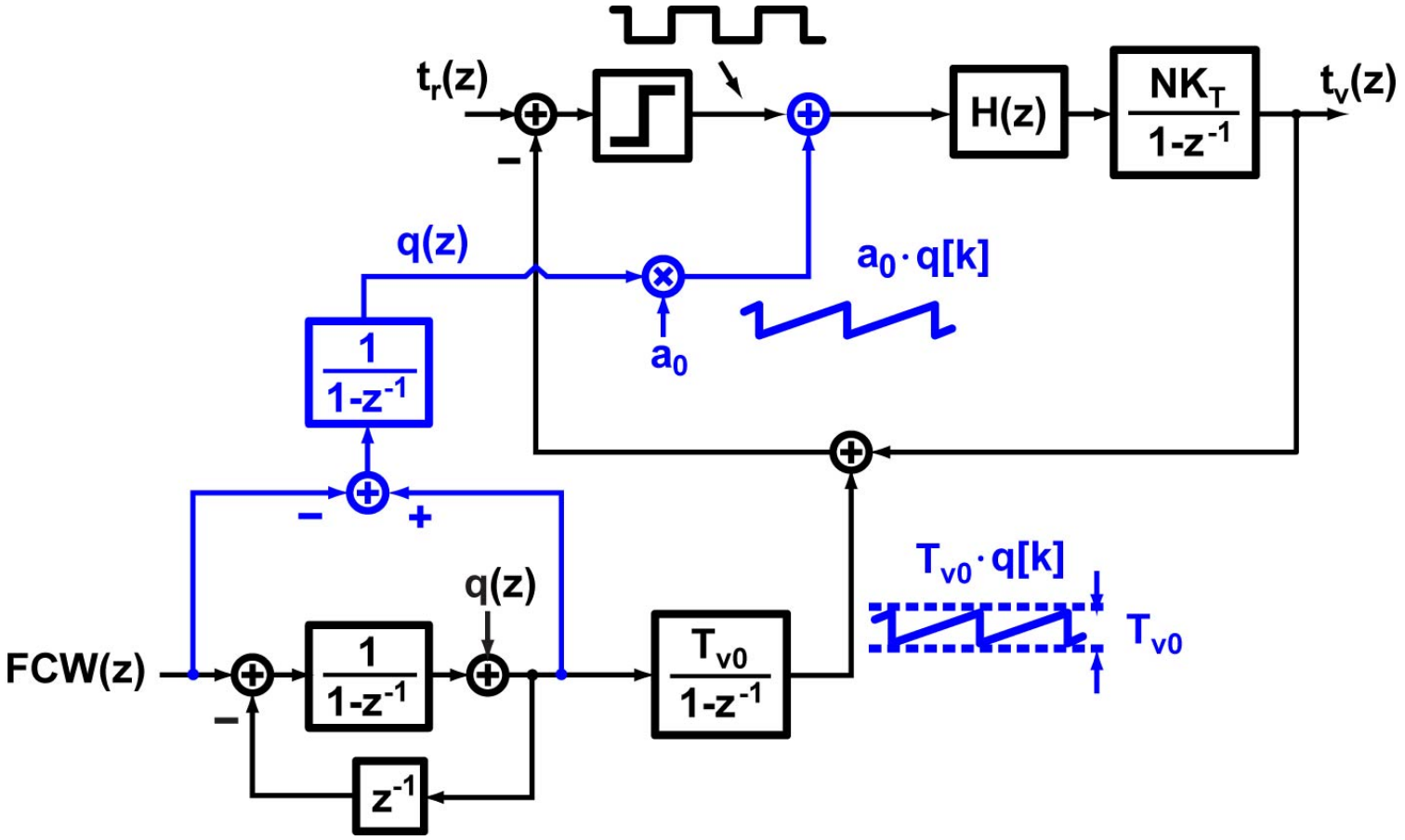
Digiphase Technique with Bang-Bang TDC



- **ΔΣ quantization error exceeds linear range of the Bang-Bang Phase Detector**

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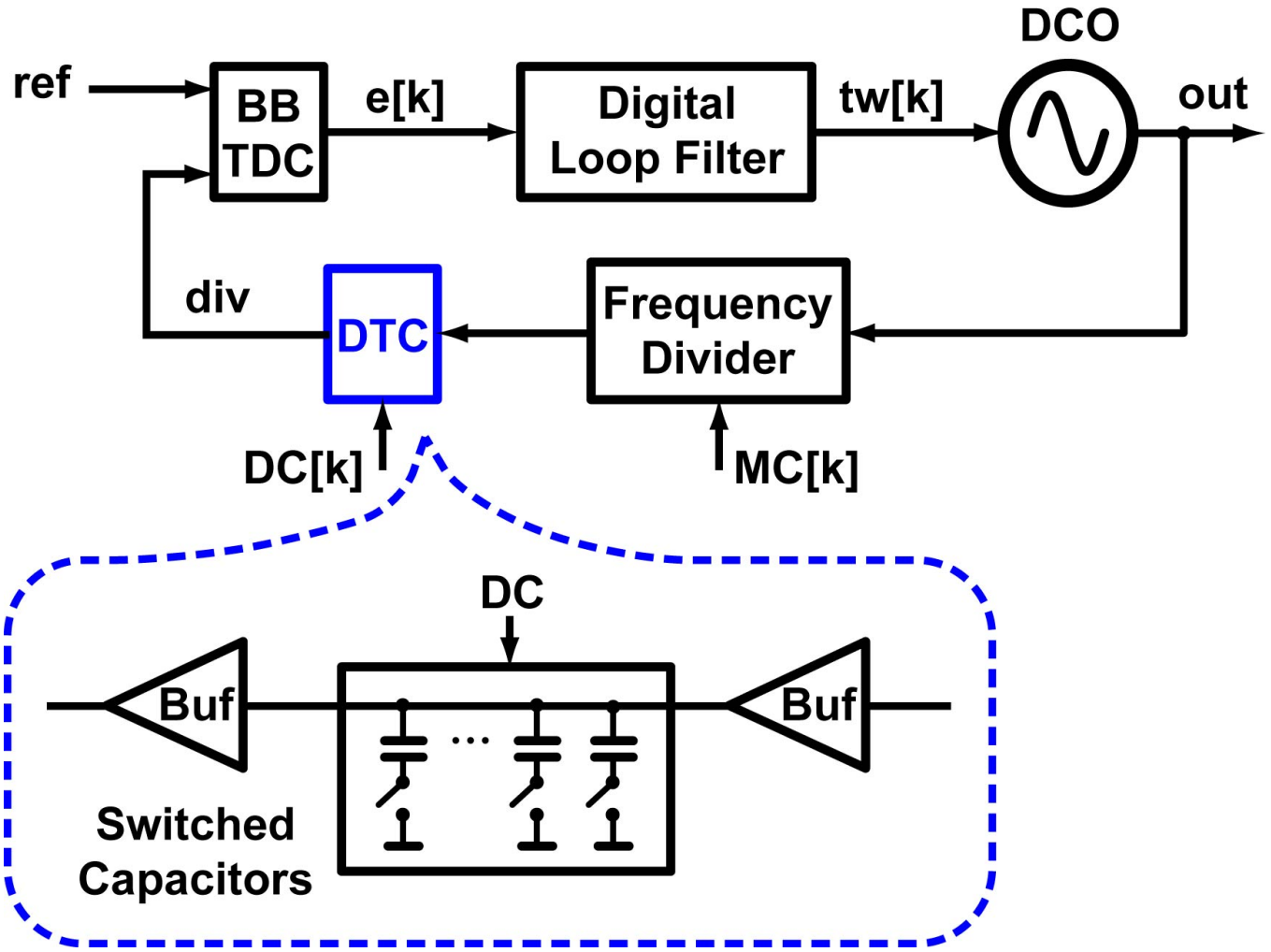
Solution: Digital-To-Time Converter (DTC)



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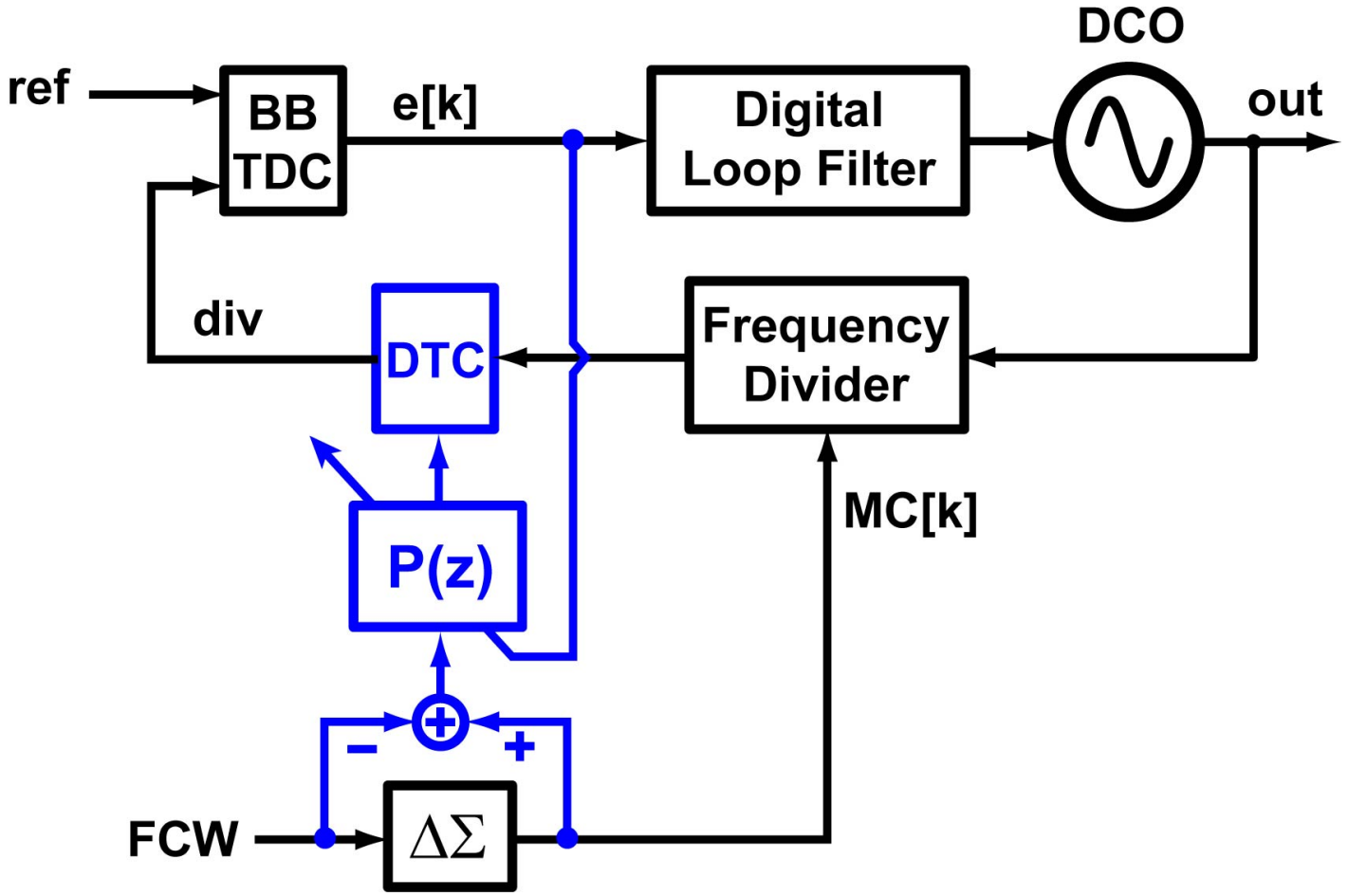
Bang-Bang Fractional-N DPLL



- **ΔΣ noise is cancelled out via DTC**

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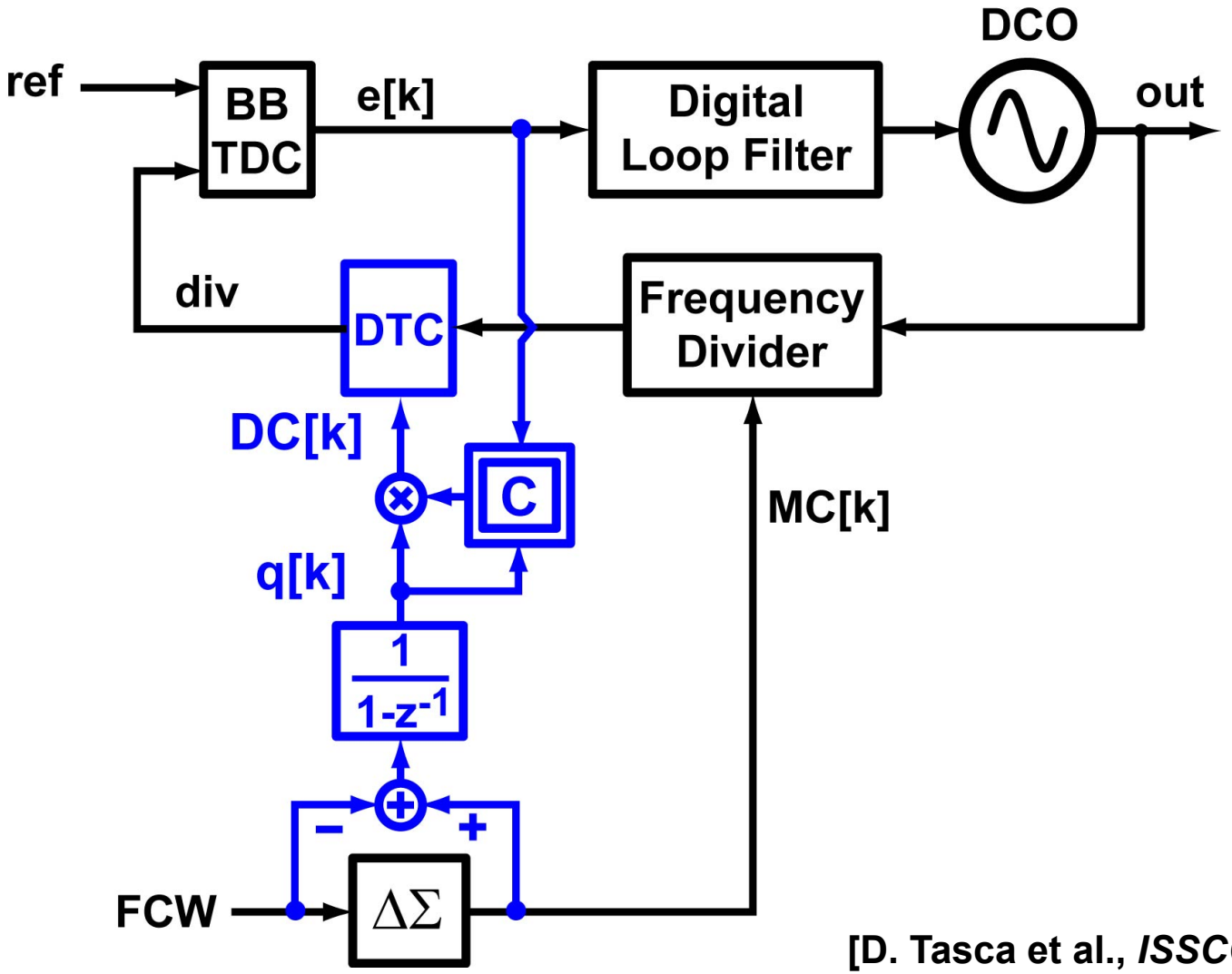
Automatic Regulation of DTC Characteristic



[D. Tasca et al., *ISSCC*, 2011]

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Conclusion

- DPLLs with bang-bang detectors (i.e. coarse TDCs with mid-rise quantization) can be employed even in fractional-N frequency synthesis
- In practice, they require a DTC block with fine resolution, which can be improved leveraging oversampling techniques
- DTCs are easier to be designed than TDCs
- Fractional-N BBPLLs maintain the superior efficiency (noise/power trade-off) over conventional DPLLs

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Direct FM Modulation

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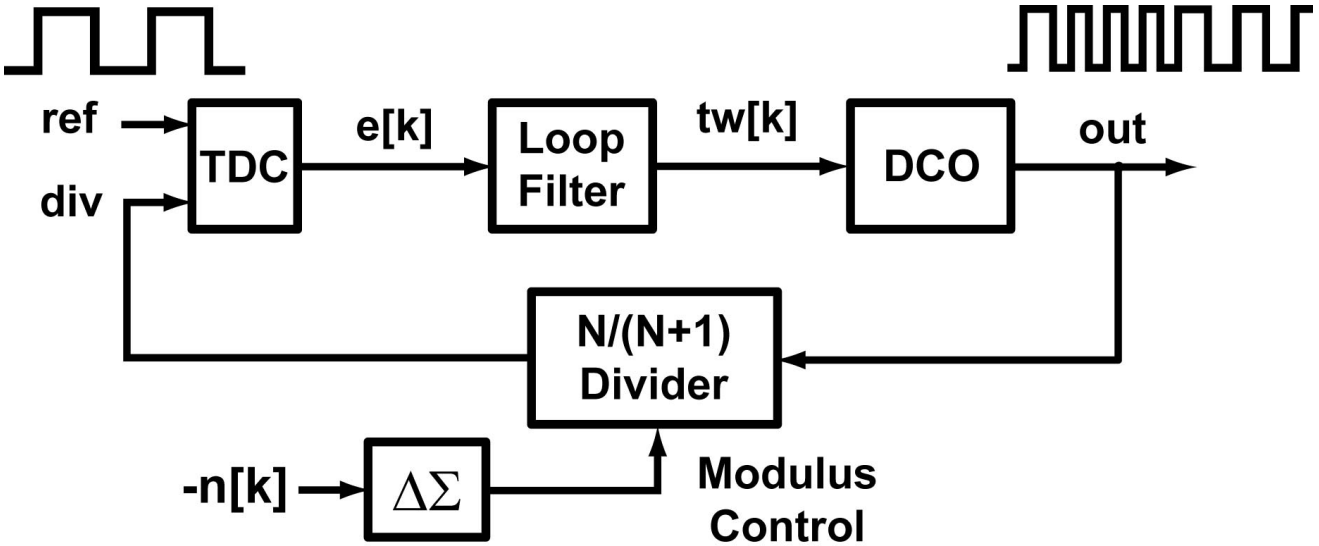
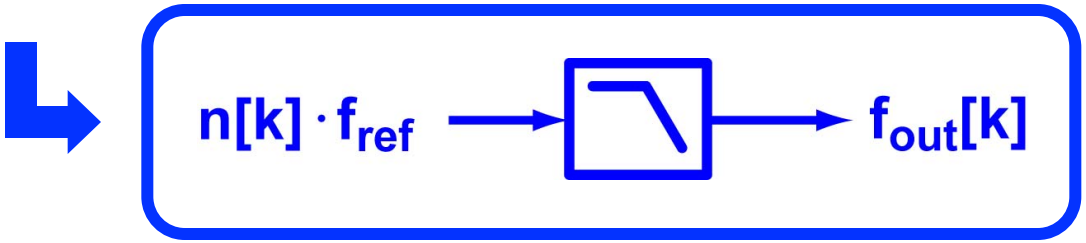
Direct-FM of a Digital PLL





- **Modulation rate is limited by loop BW**

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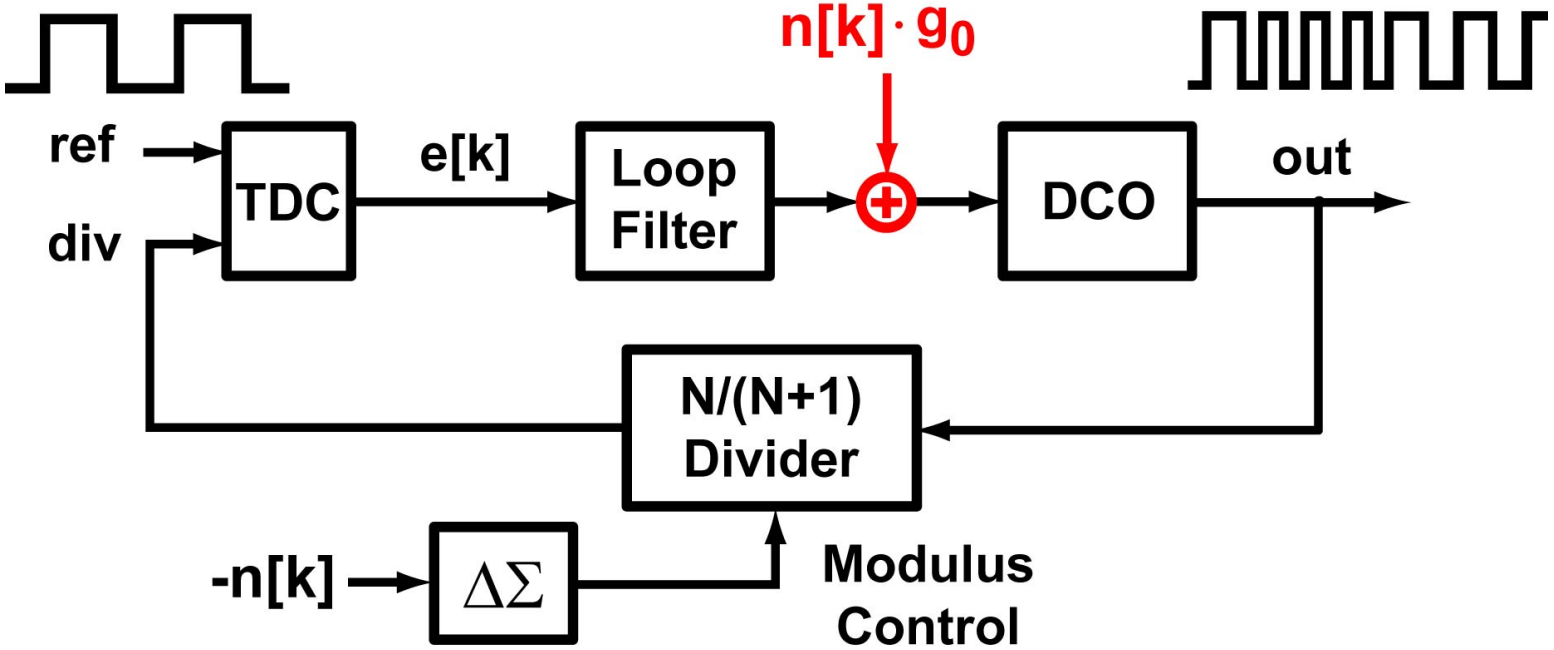
Two-Path Injection of Modulation Signal



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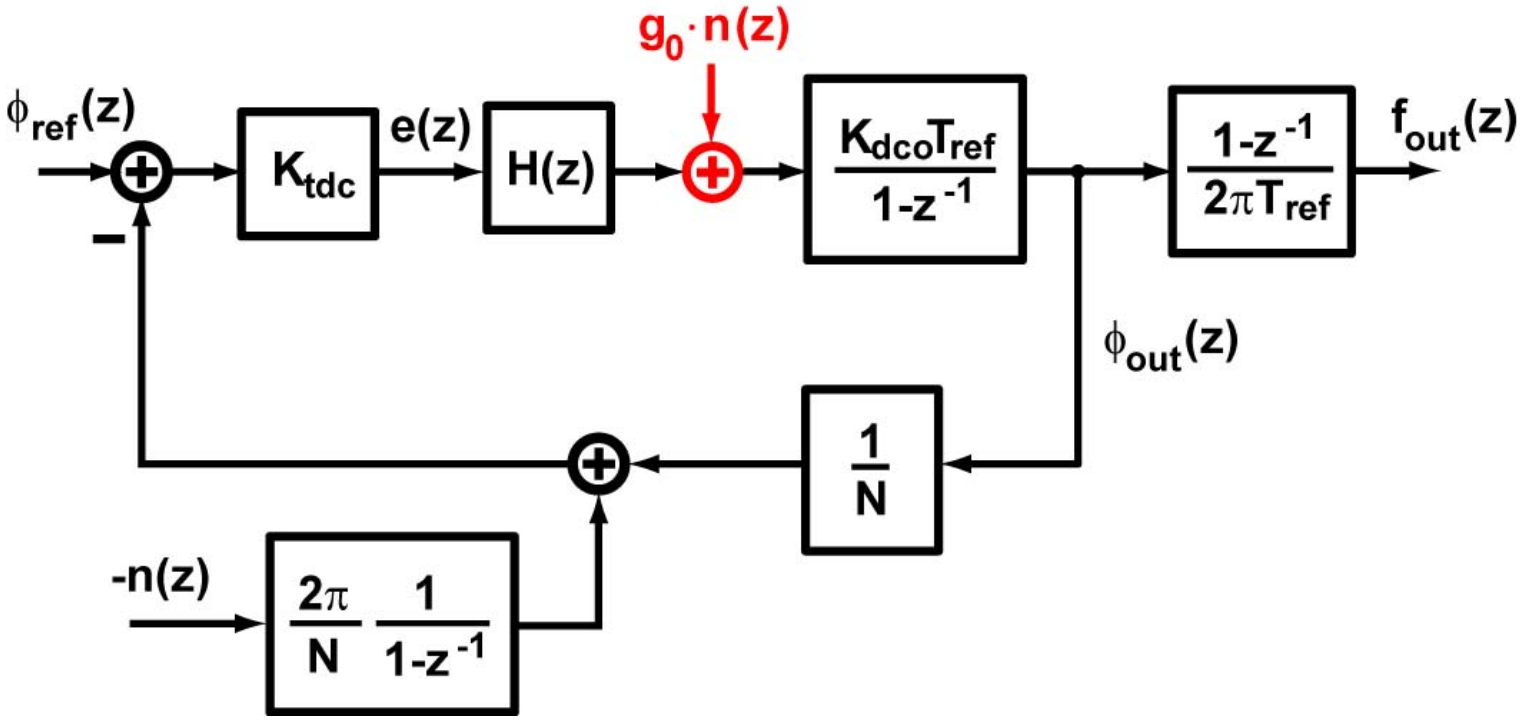
Output Frequency Expression



$$f_{out}(z) = n(z) \cdot \left[\frac{g_0 K_{dco}}{2\pi} \cdot \frac{1}{1 + G_{loop}(z)} + f_{ref} \cdot \frac{G_{loop}(z)}{1 + G_{loop}(z)} \right]$$

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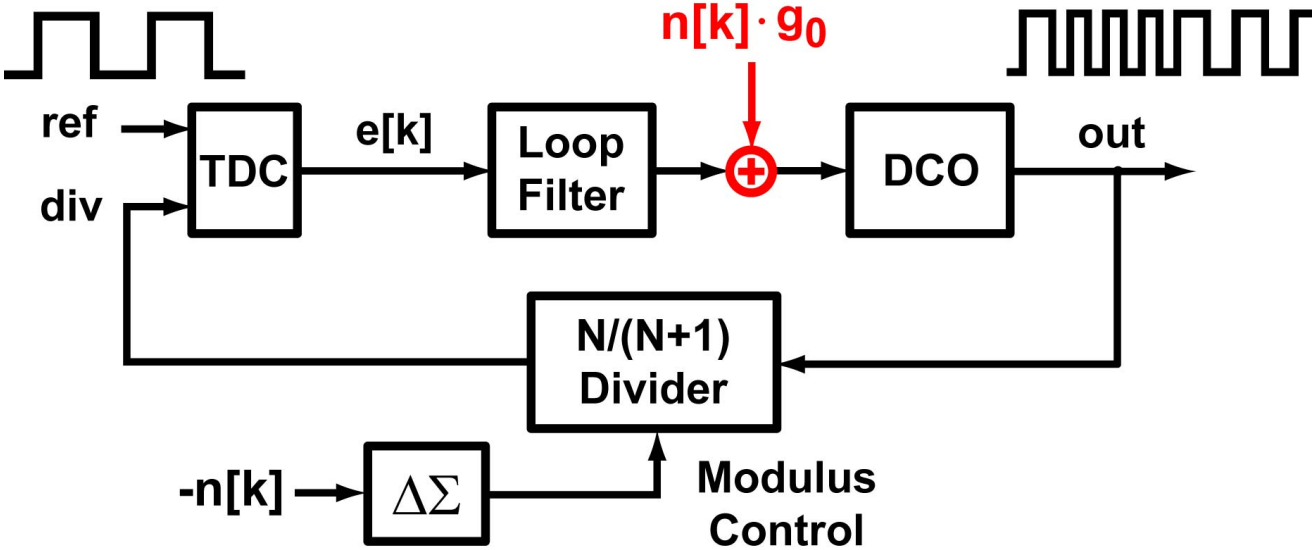
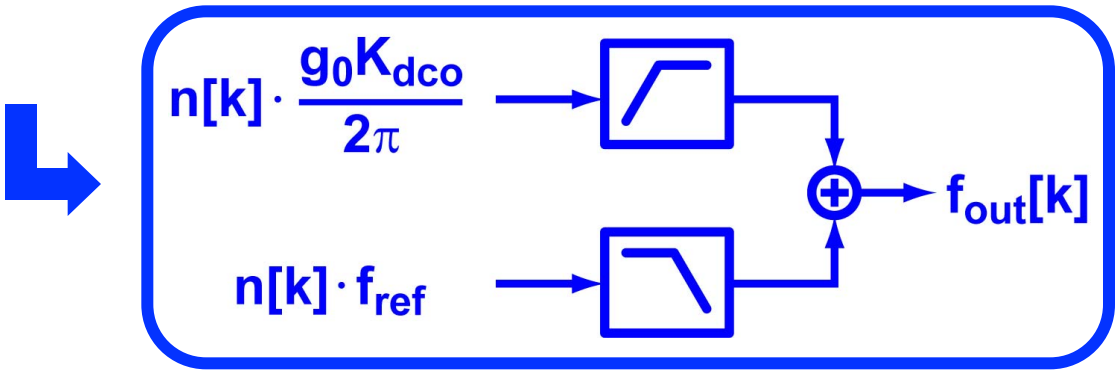
Extension of Modulation Bandwidth





- **All-pass transfer function if $g_0K_{dco}/2\pi = f_{ref}$**

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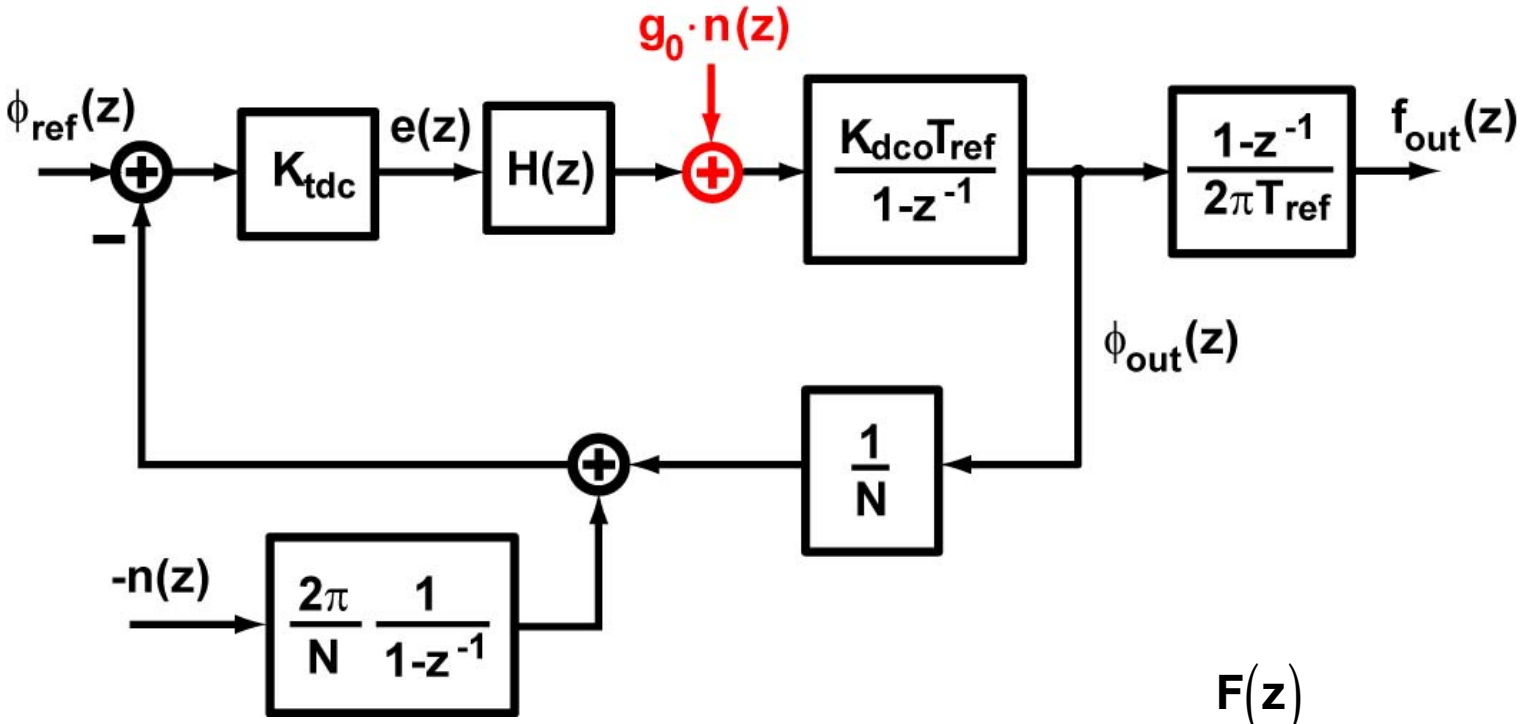
Tracking of K_{dco} Variations



$$e(z) = n(z) \cdot \left[2\pi f_{ref} - g_0 K_{dco}\right] \cdot \overbrace{\frac{G_{loop}(z)}{1+G_{loop}(z)} \cdot \frac{1}{K_{dco}H(z)}}^{F(z)}$$

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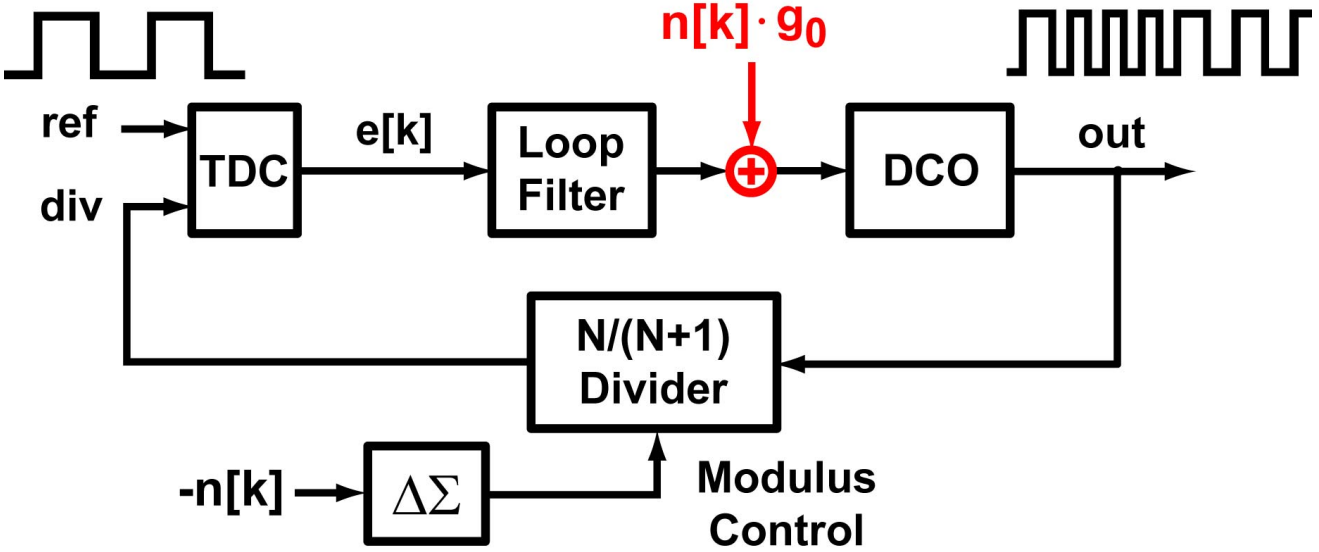
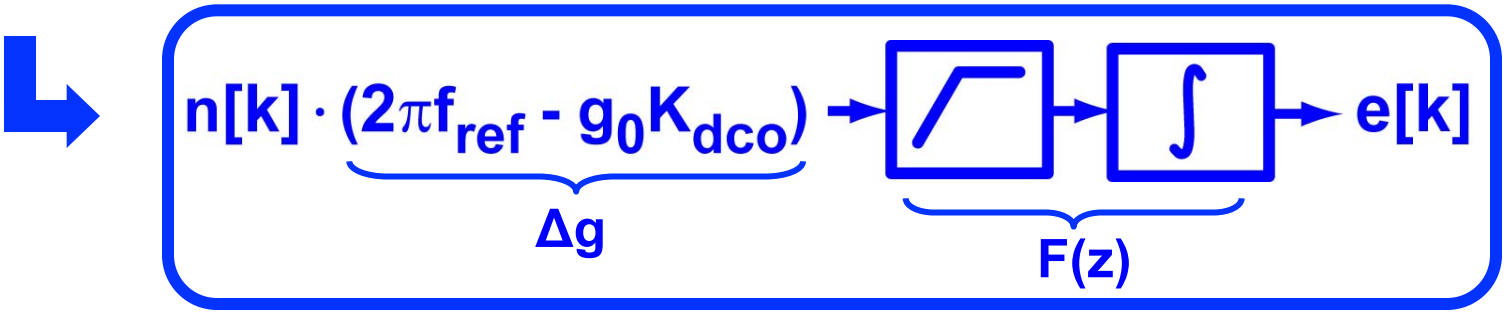
Effect of Gain Imbalance





- Correlation c[k] = E{ e[k]·n[k] } is proportional to gain imbalance Δg

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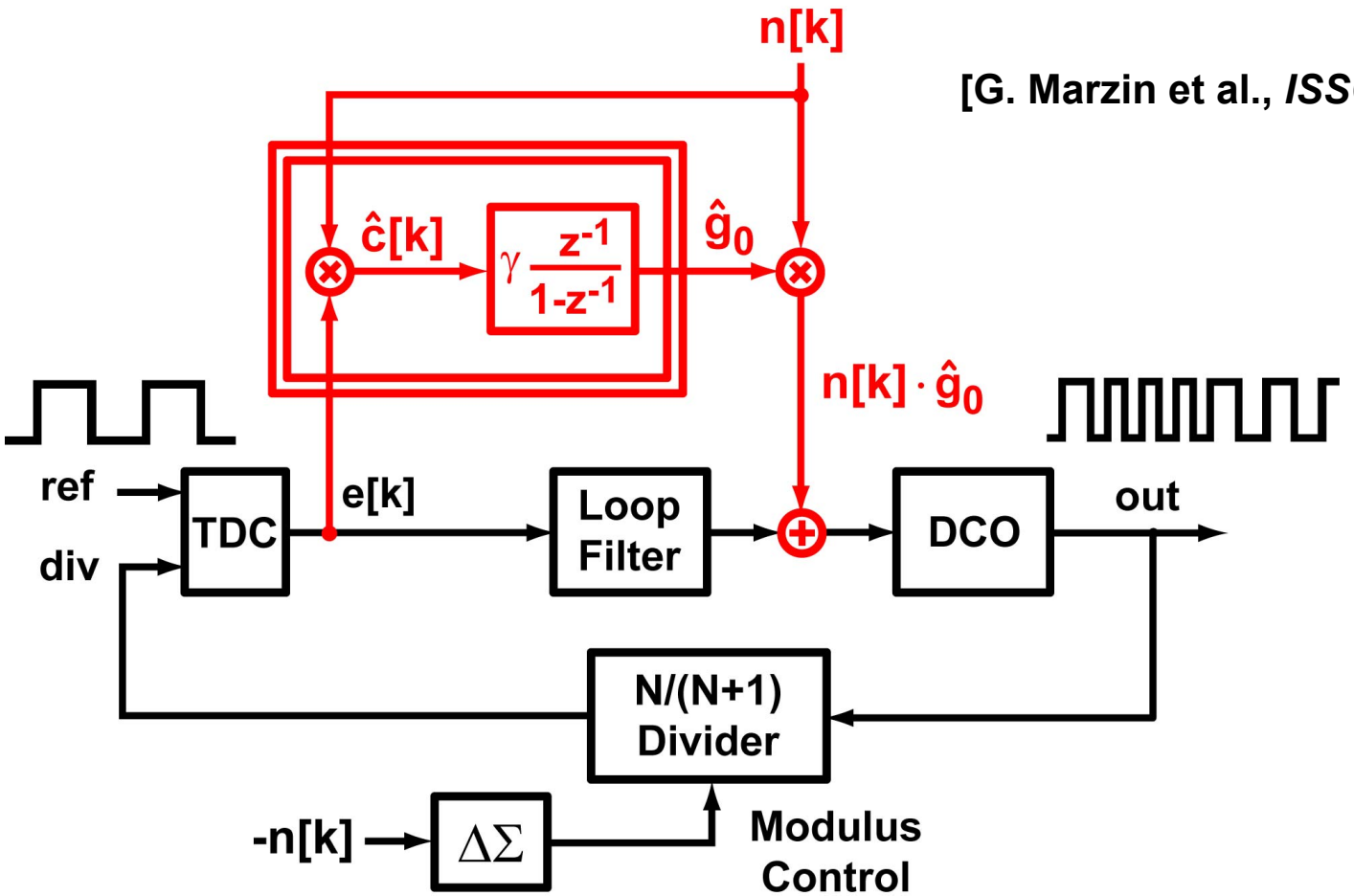
Adaptation of DCO-Path Gain via LMS

[G. Marzin et al., *ISSCC*, 2012]



- **LMS loop nulls ĉ[k], thus gain imbalance Δg**

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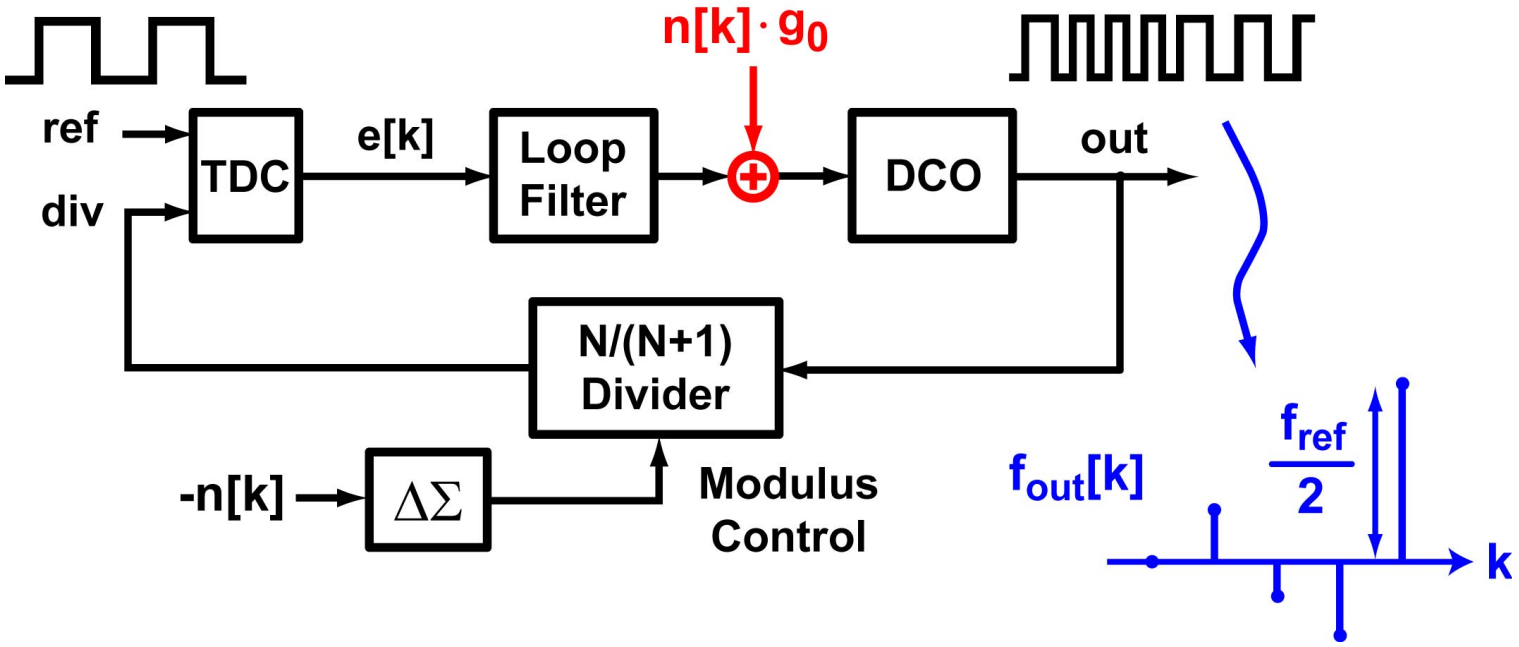
DCO Range Requirements



- Phase shift up to ±π in one ref cycle
- DCO tuning range in excess of f_{ref}
- DCO frequency granularity order of 10kHz
- DCO with linear control over 10-12 bit

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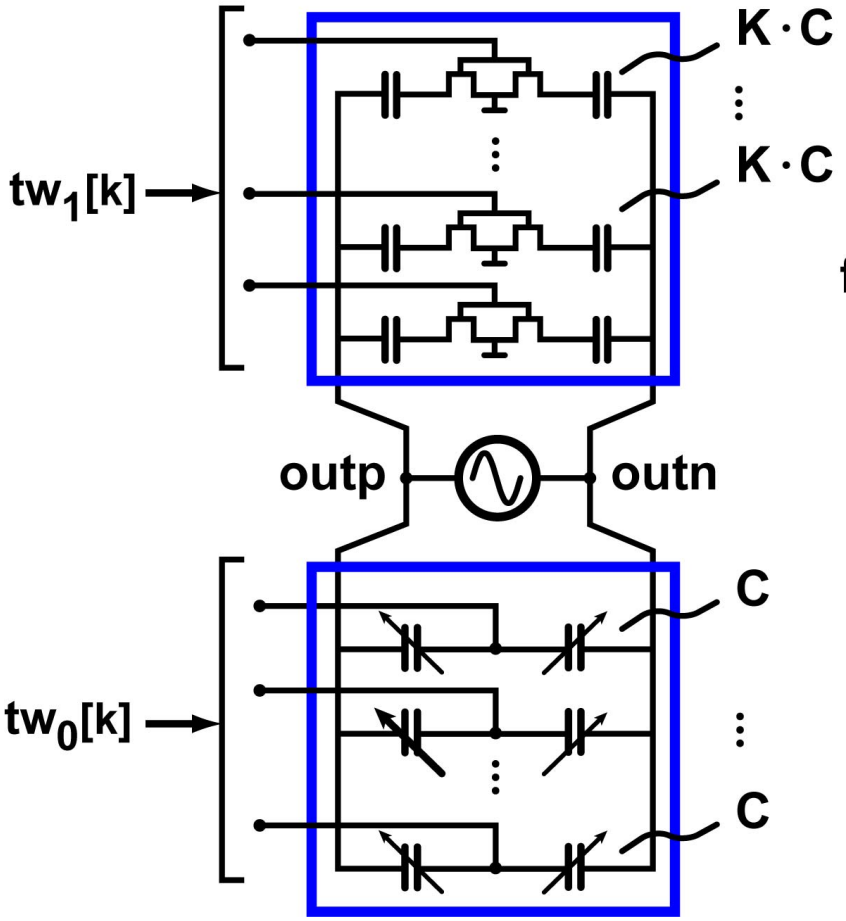
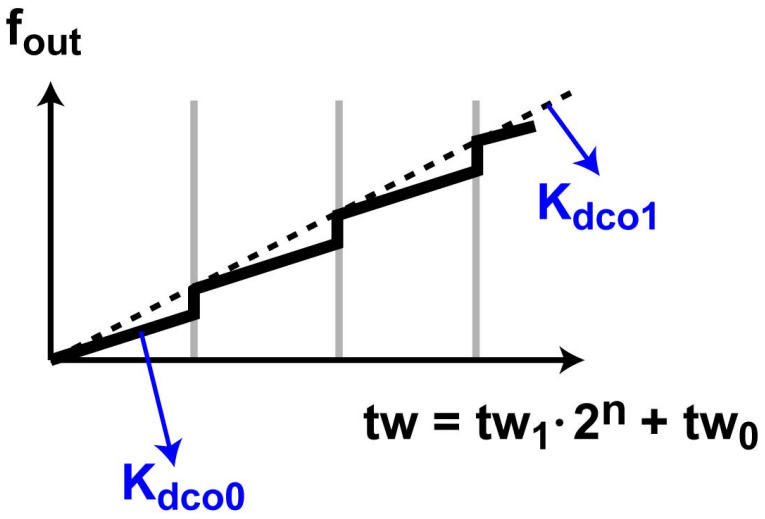
Nonlinearity of DCO w/ Multi-Capacitor-Bank





- Saves area and improves tuning range
- Produces *inter-bank* nonlinearity

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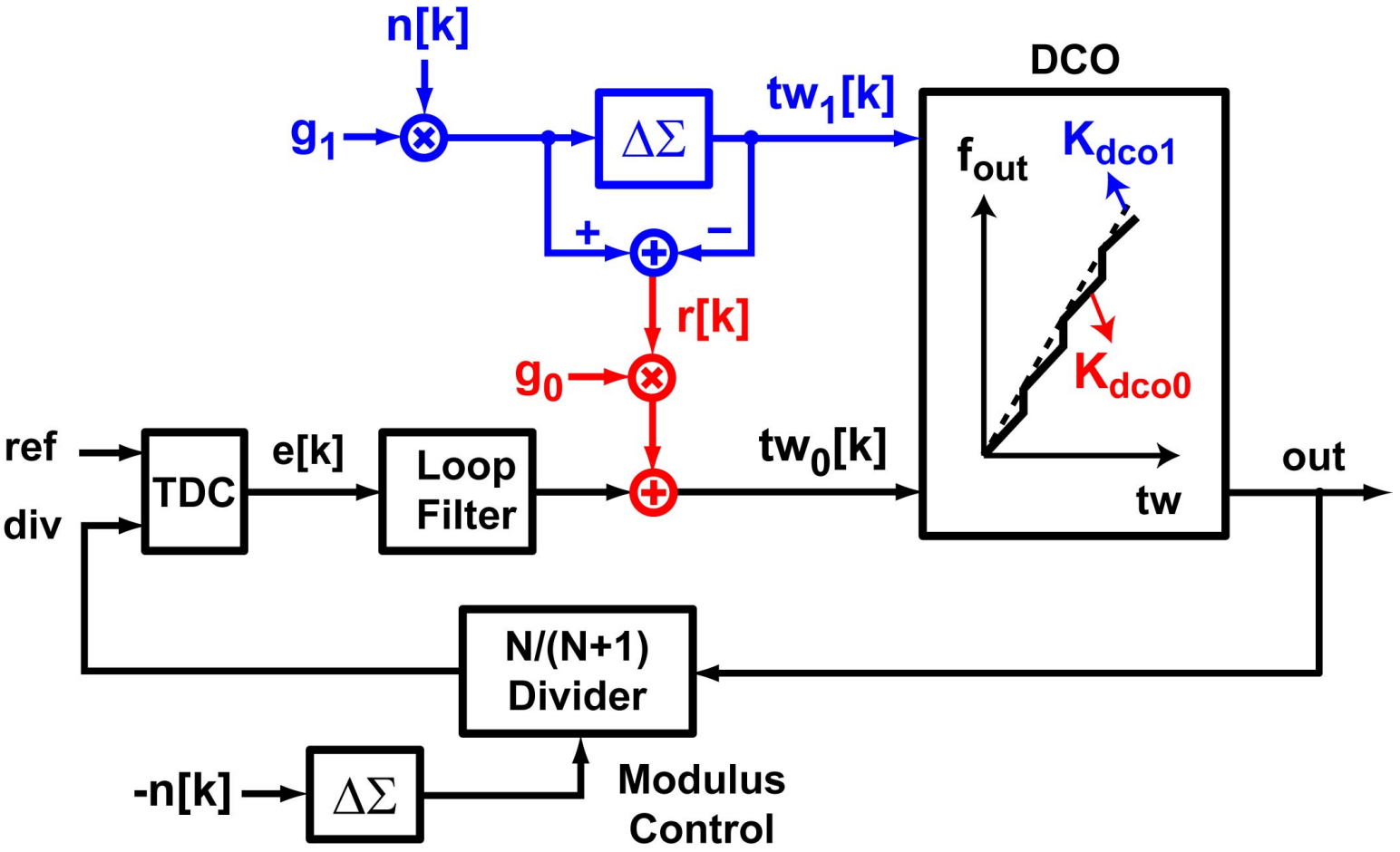
Direct-FM with Multi-Bank DCO



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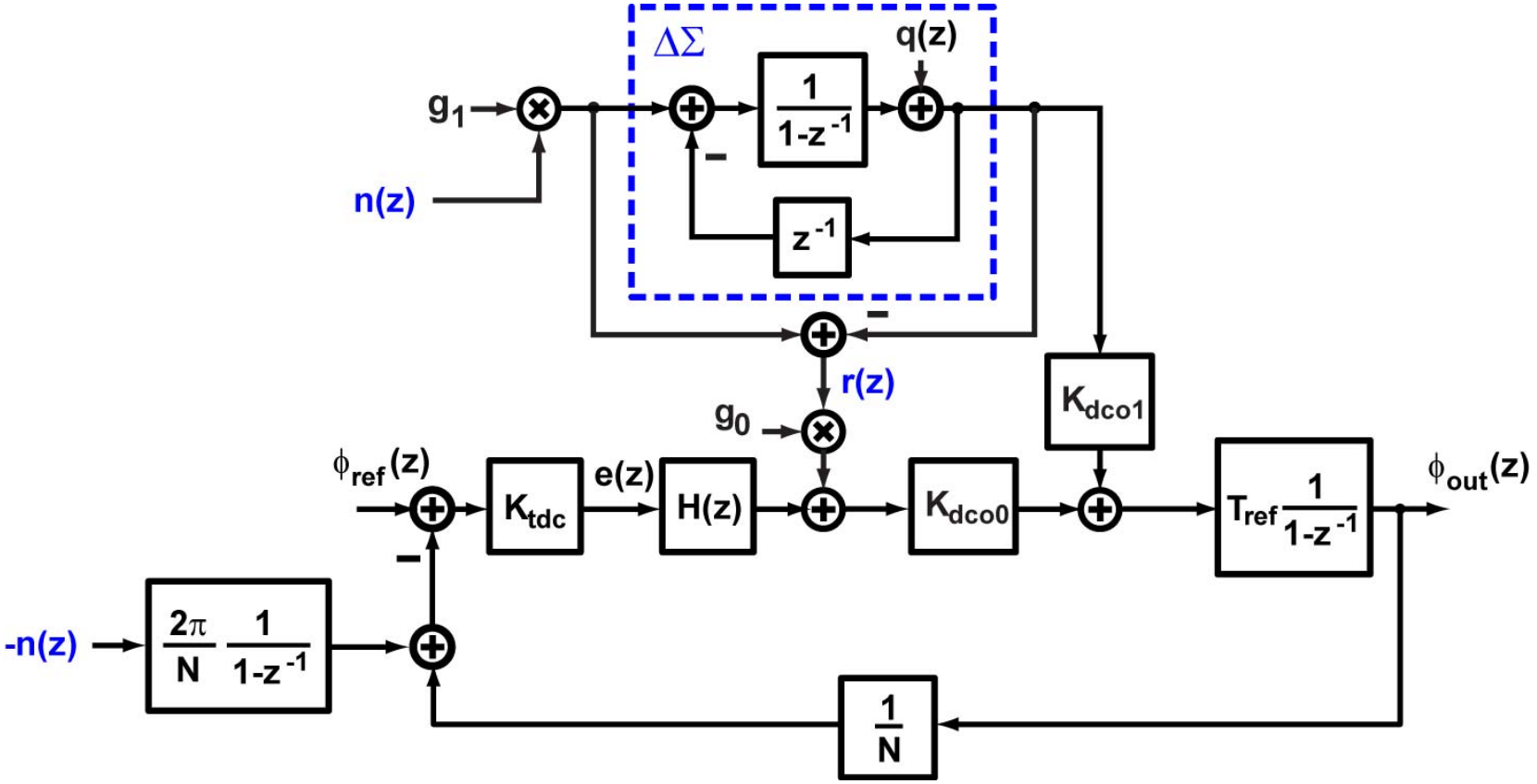
Model of the Modified System



$$e(z) = n(z)\cdot\left[2\pi f_{ref} - g_1 K_{dco1}\right]\cdot F(z)$$
$$+\, r(z)\cdot\left[K_{dco1} - g_0 K_{dco0}\right]\cdot F(z)$$

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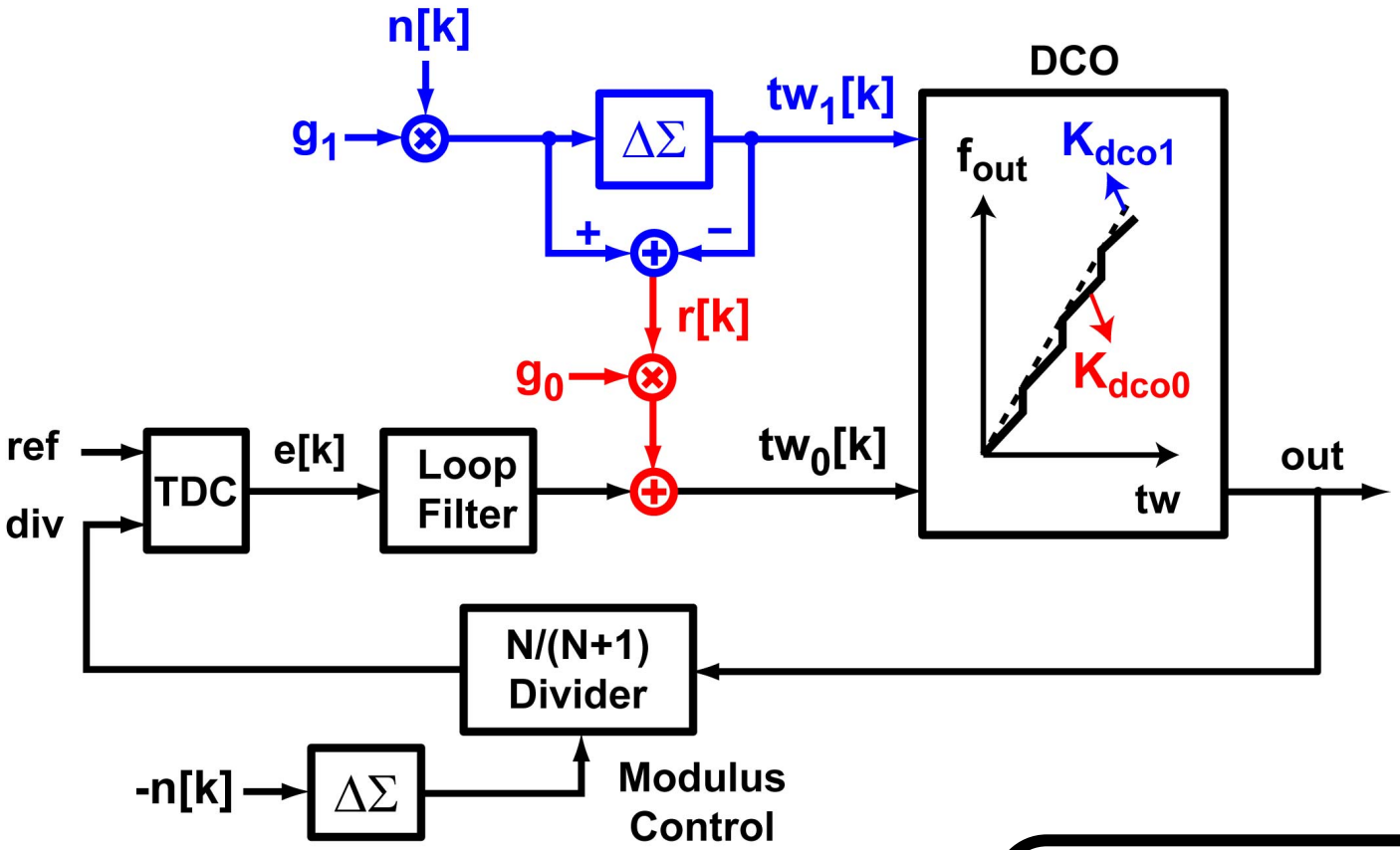
Direct-FM with Multi-Bank DCO



- **All-pass transfer function if:**

$$2\pi f_{ref} = g_1 K_{dco1}$$

$$K_{dco1} = g_0 K_{dco0}$$

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Gains and Correlations

$$e(z) = n(z) \cdot \left[2\pi f_{ref} - g_1 K_{dco1} \right] \cdot F(z)$$
$$+ r(z) \cdot \left[K_{dco1} - g_0 K_{dco0} \right] \cdot F(z)$$

- Gain g_1 must be regulated so that it nulls the correlation $c_n[k] = E\{ e[k] \cdot n[k] \}$
- Gain g_0 must be regulated so that it nulls the correlation $c_r[k] = E\{ e[k] \cdot r[k] \}$

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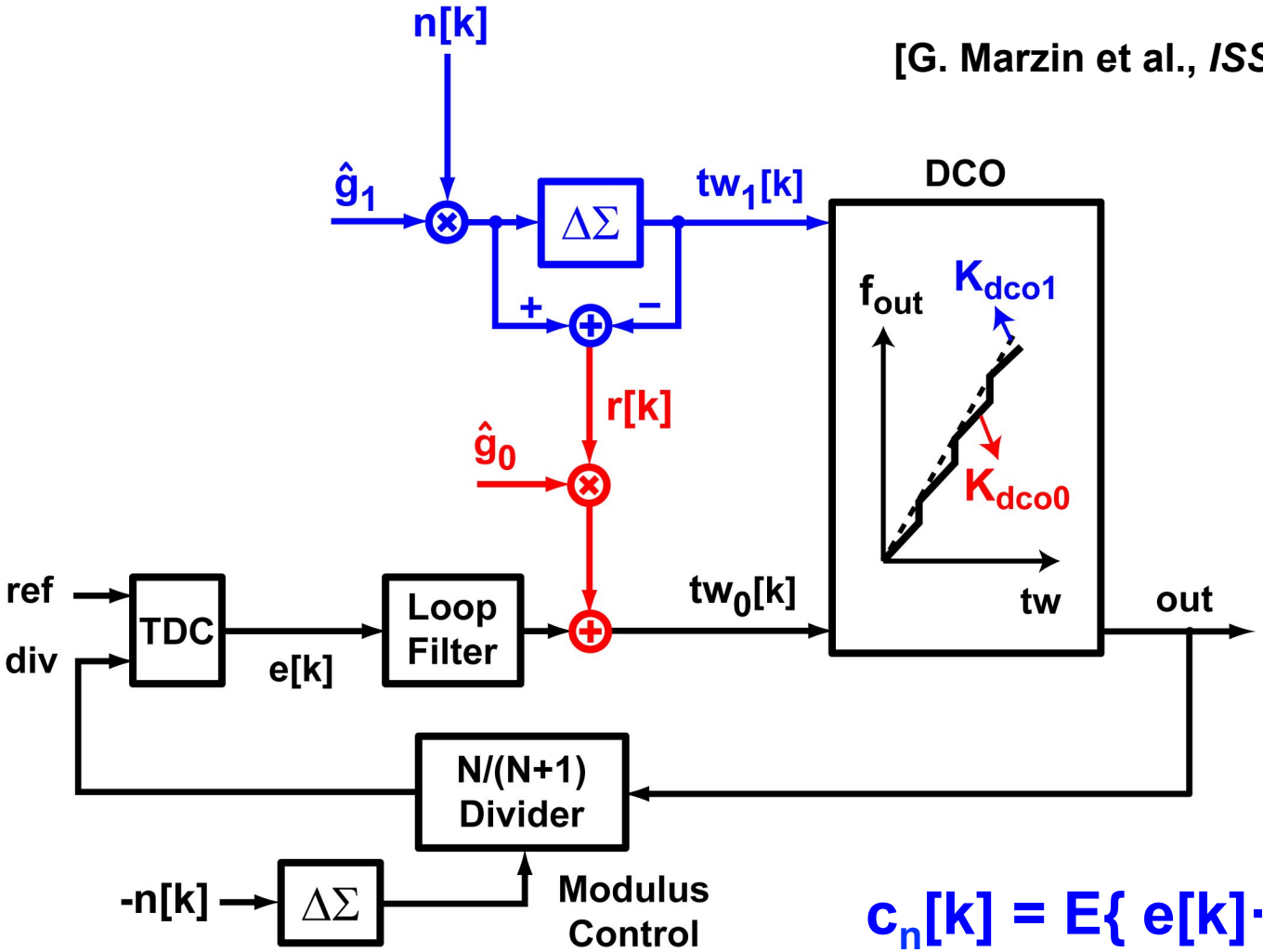
Gain Adaptation of Multi-Bank-DCO

[G. Marzin et al., *ISSCC*, 2012]



$$c_n[k] = E\{ e[k] \cdot n[k] \}$$

$$c_r[k] = E\{ e[k] \cdot r[k] \}$$

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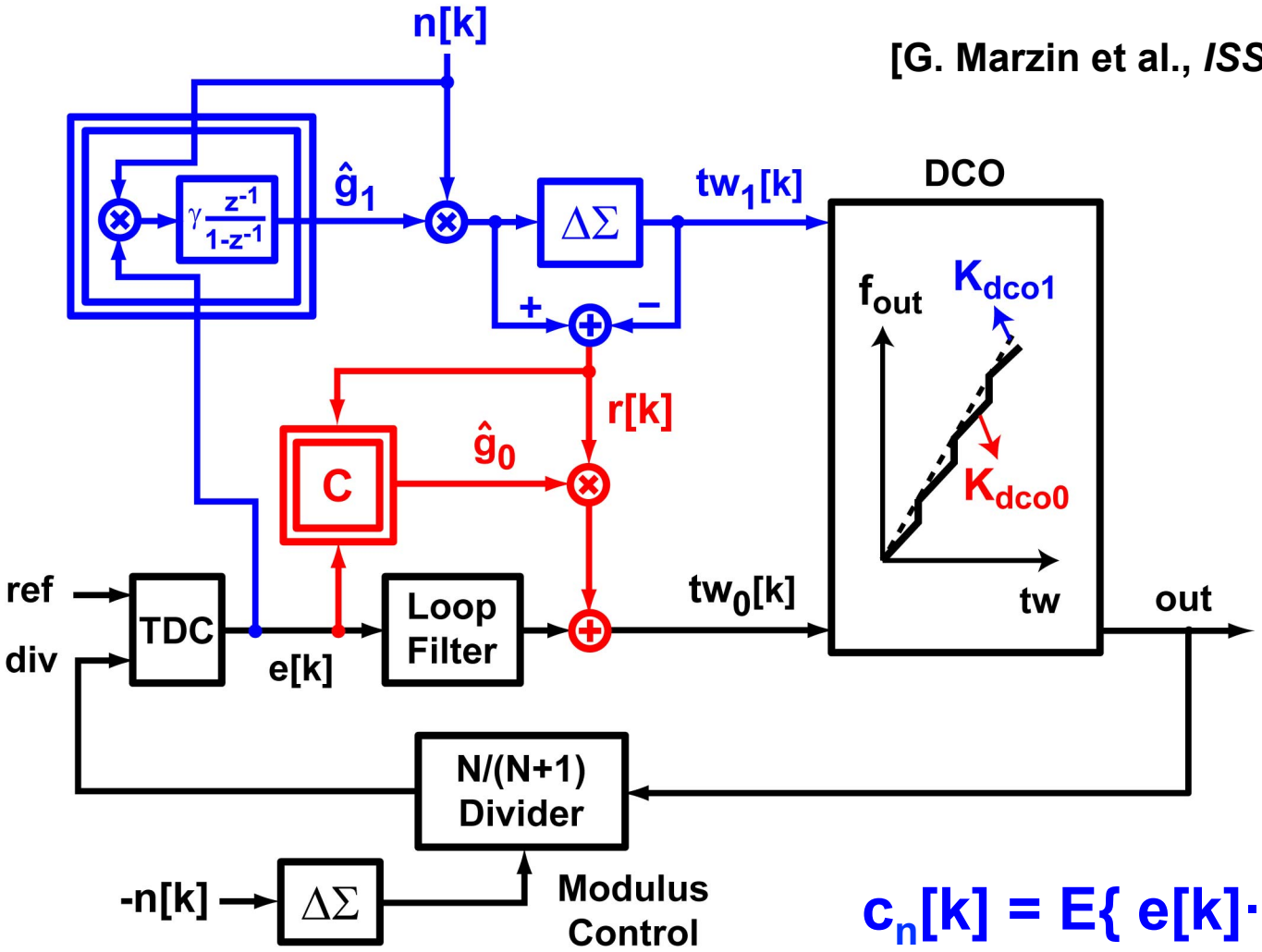
Gain Adaptation of Multi-Bank-DCO (Cont'd)

[G. Marzin et al., *ISSCC*, 2012]



$$c_n[k] = E\{ e[k] \cdot n[k] \}$$

$$c_r[k] = E\{ e[k] \cdot r[k] \}$$

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Practical Implementation

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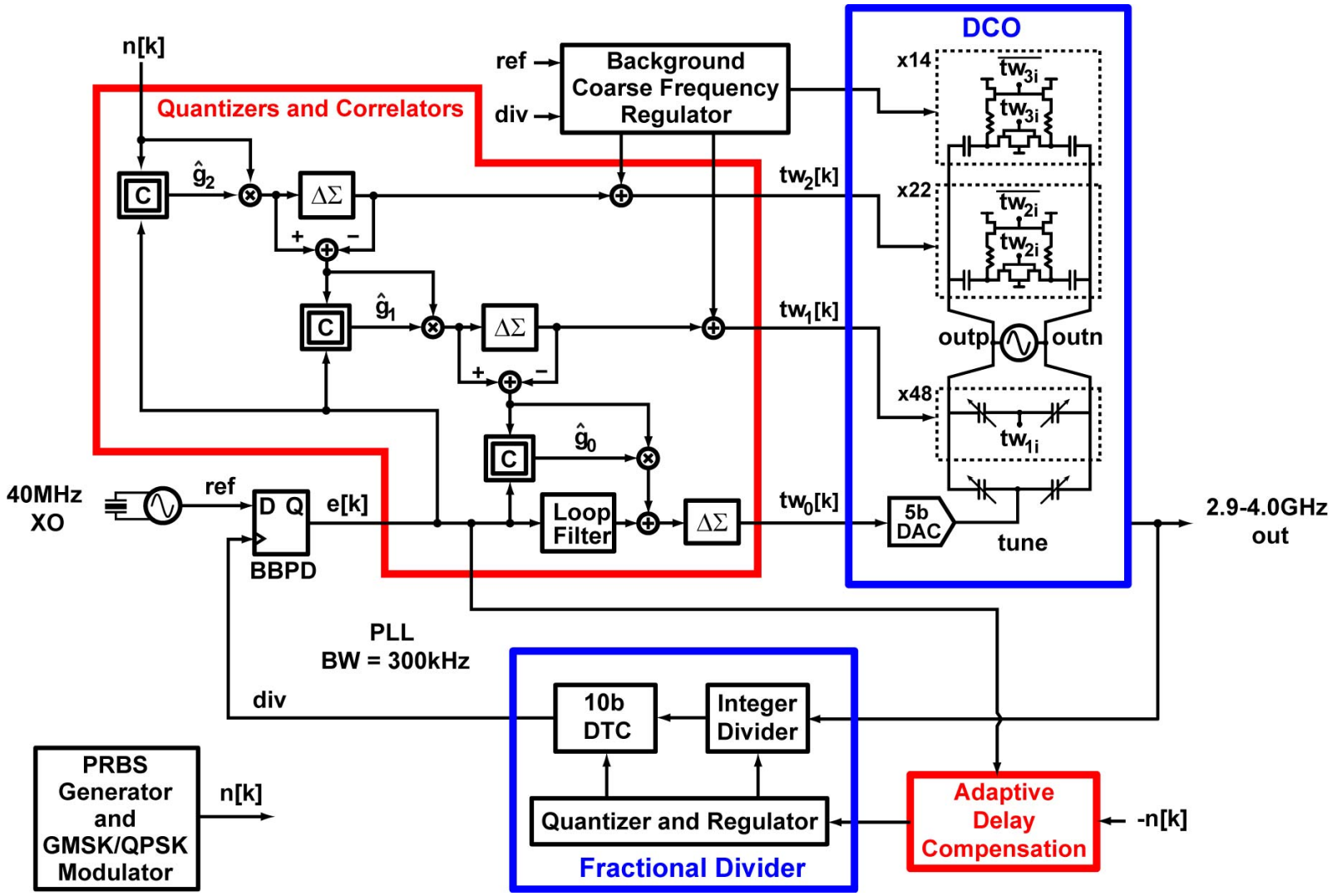
Implemented Phase Modulator



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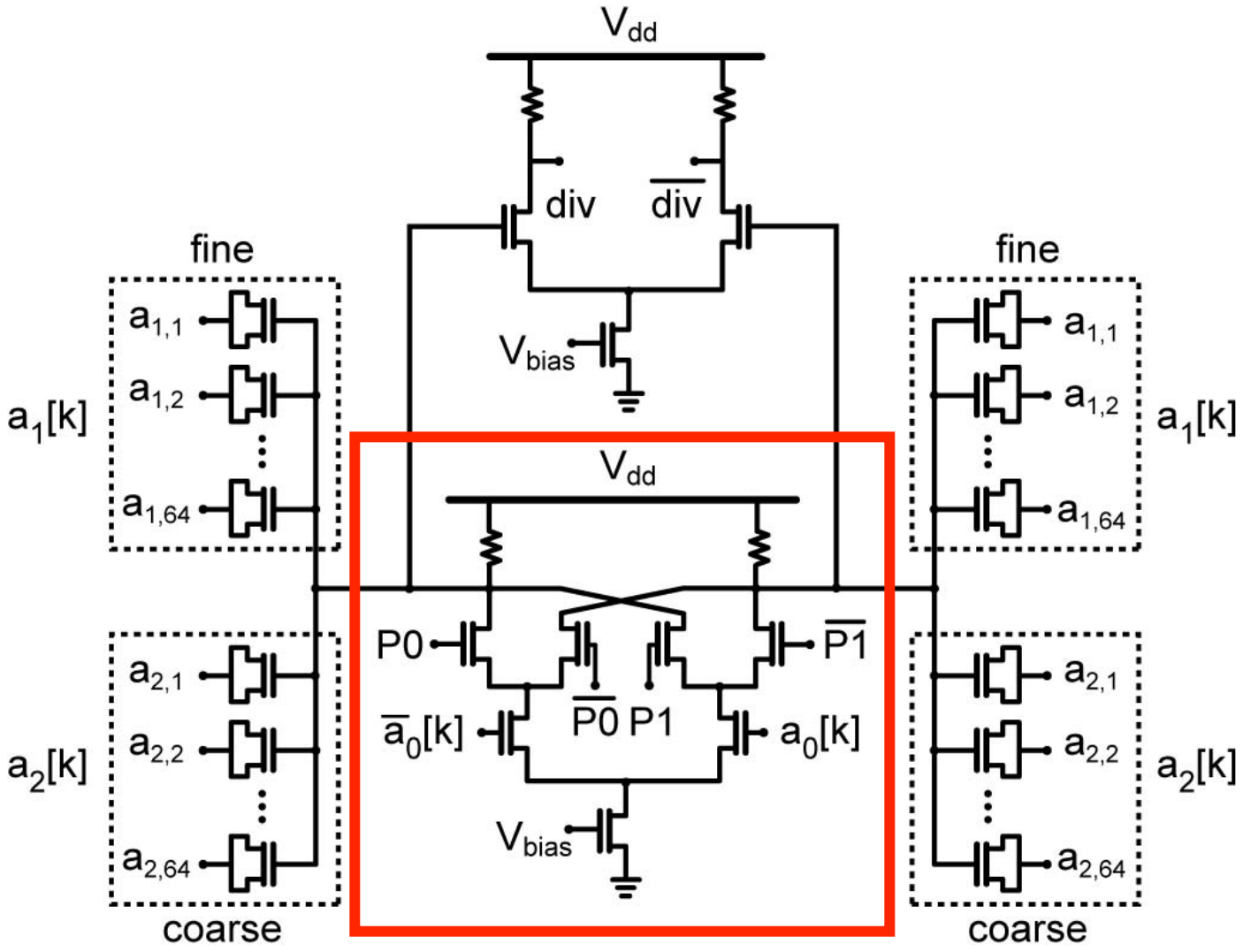
Practical DTC Schematic



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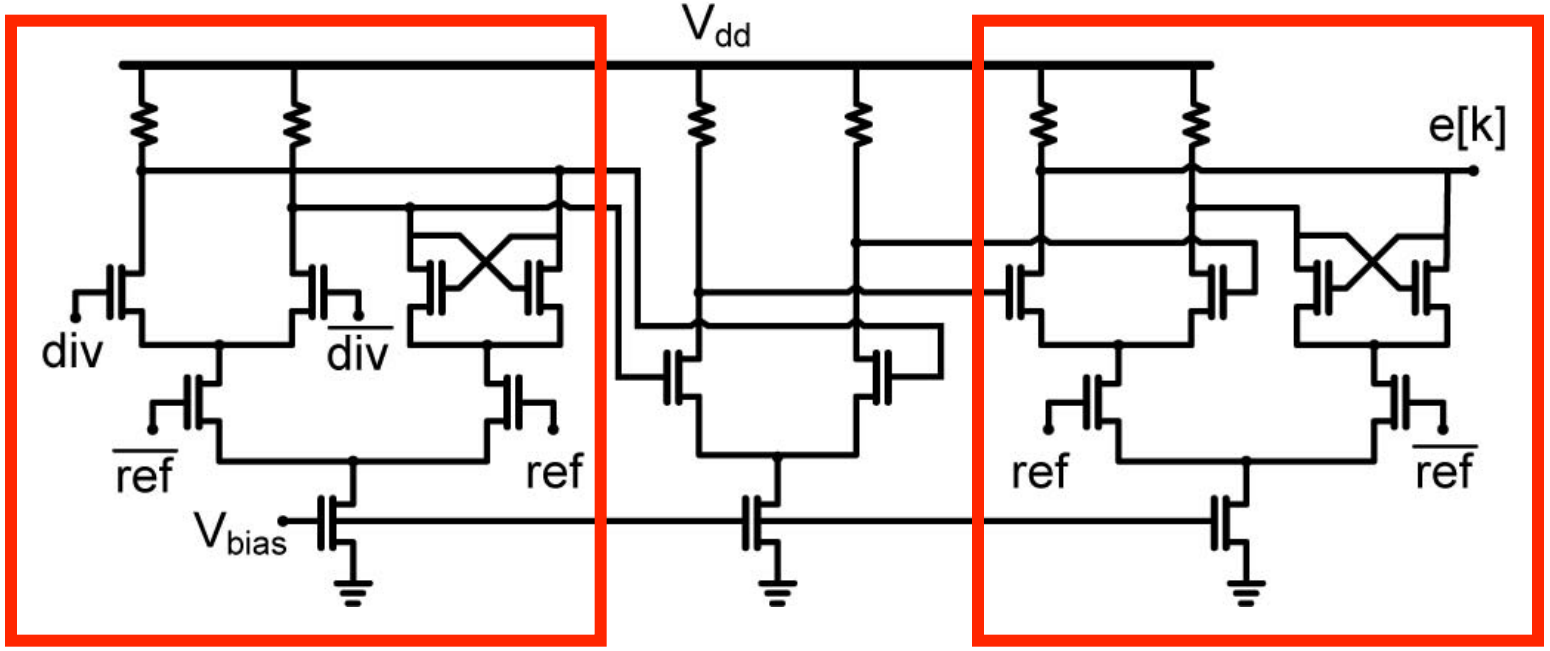
Practical Bang-Bang-Detector Schematic



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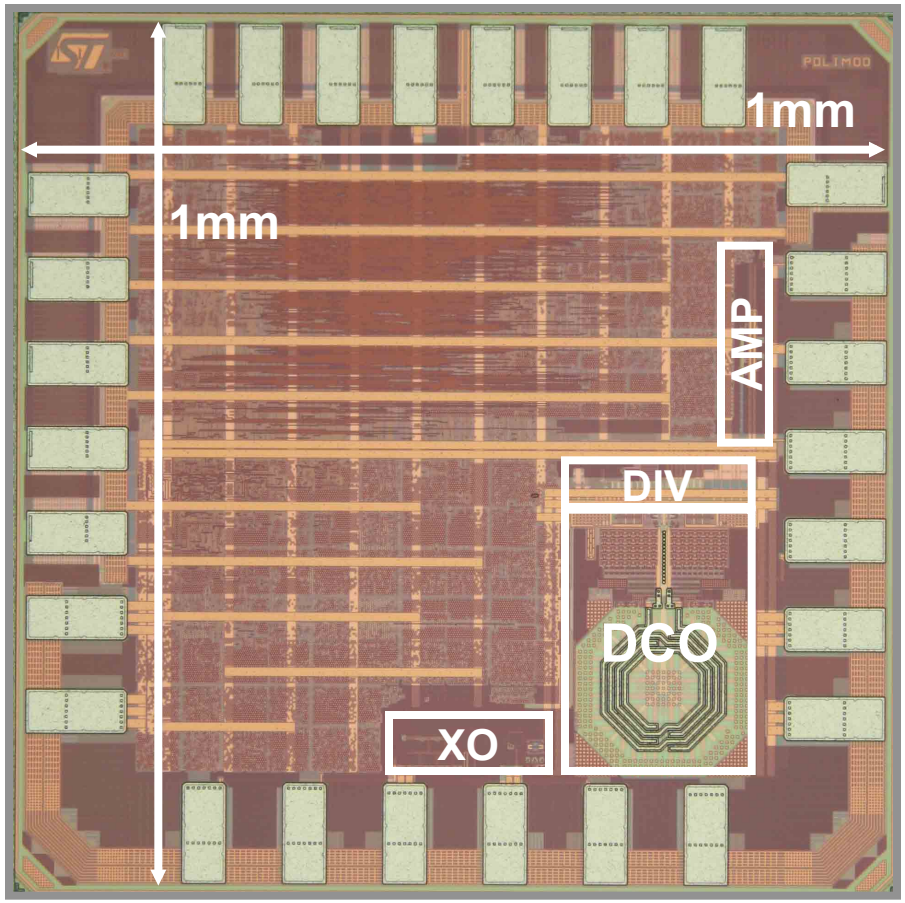
Die Photograph



[G. Marzin et al., *ISSCC*, 2012]

- 65nm CMOS
- Active area: 0.52mm^2
- Chip area: 1.0mm^2
- Power: 5mW
- Supply voltage: 1.2V

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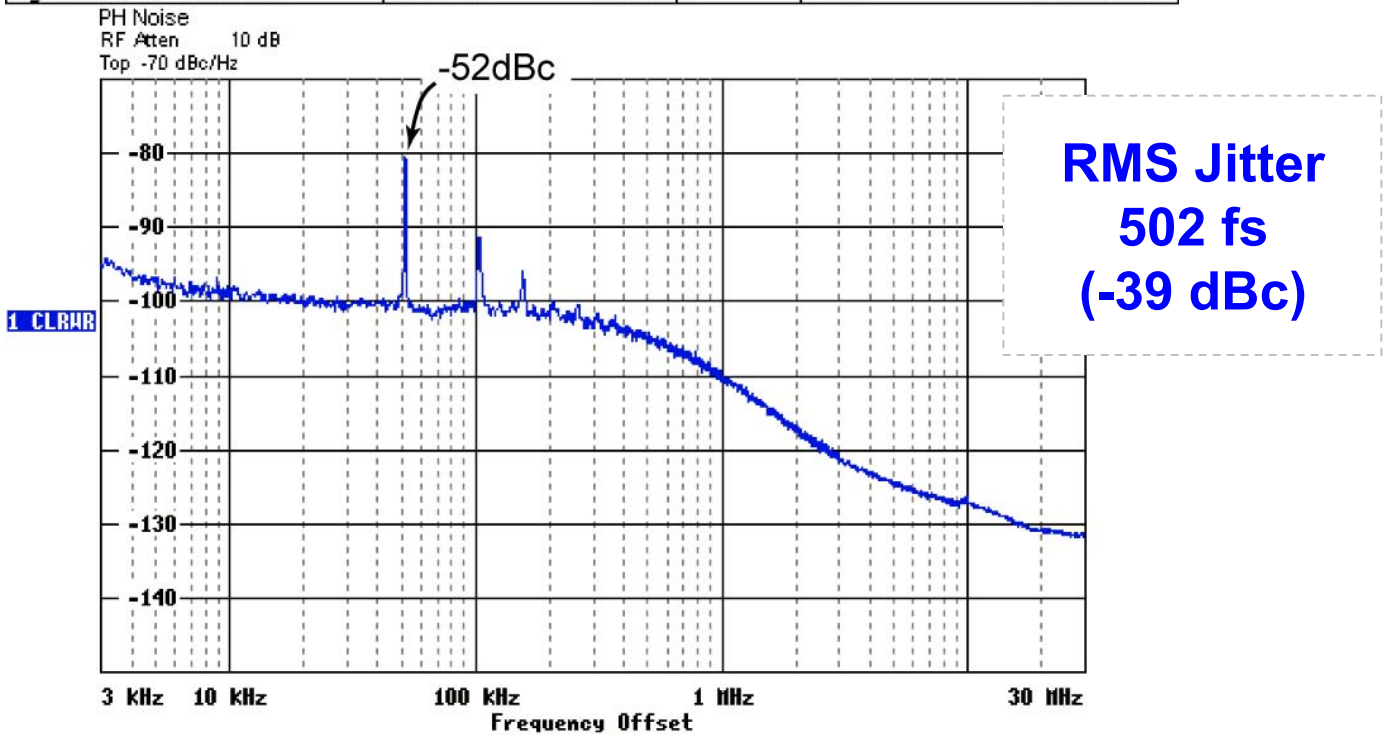
Phase Noise of 3.6-GHz Unmodulated Carrier

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T1]	
Signal Freq:	3.600902 GHz	Evaluation from 3 kHz	to 30 MHz	1 kHz	** Not Valid **
Signal Level:	-5.52 dBm	Residual PM	0.652 °	10 kHz	-99.19 dBc/Hz
Signal Freq Δ:	-38.41 Hz	Residual FM	40.594 kHz	100 kHz	-99.48 dBc/Hz
Signal Level Δ:	-0.48 dBm	RMS Jitter	0.5028 ps	1 MHz	-110.00 dBc/Hz



RMS Jitter
502 fs
(-39 dBc)

- **Near-integer channel (50 kHz offset)**

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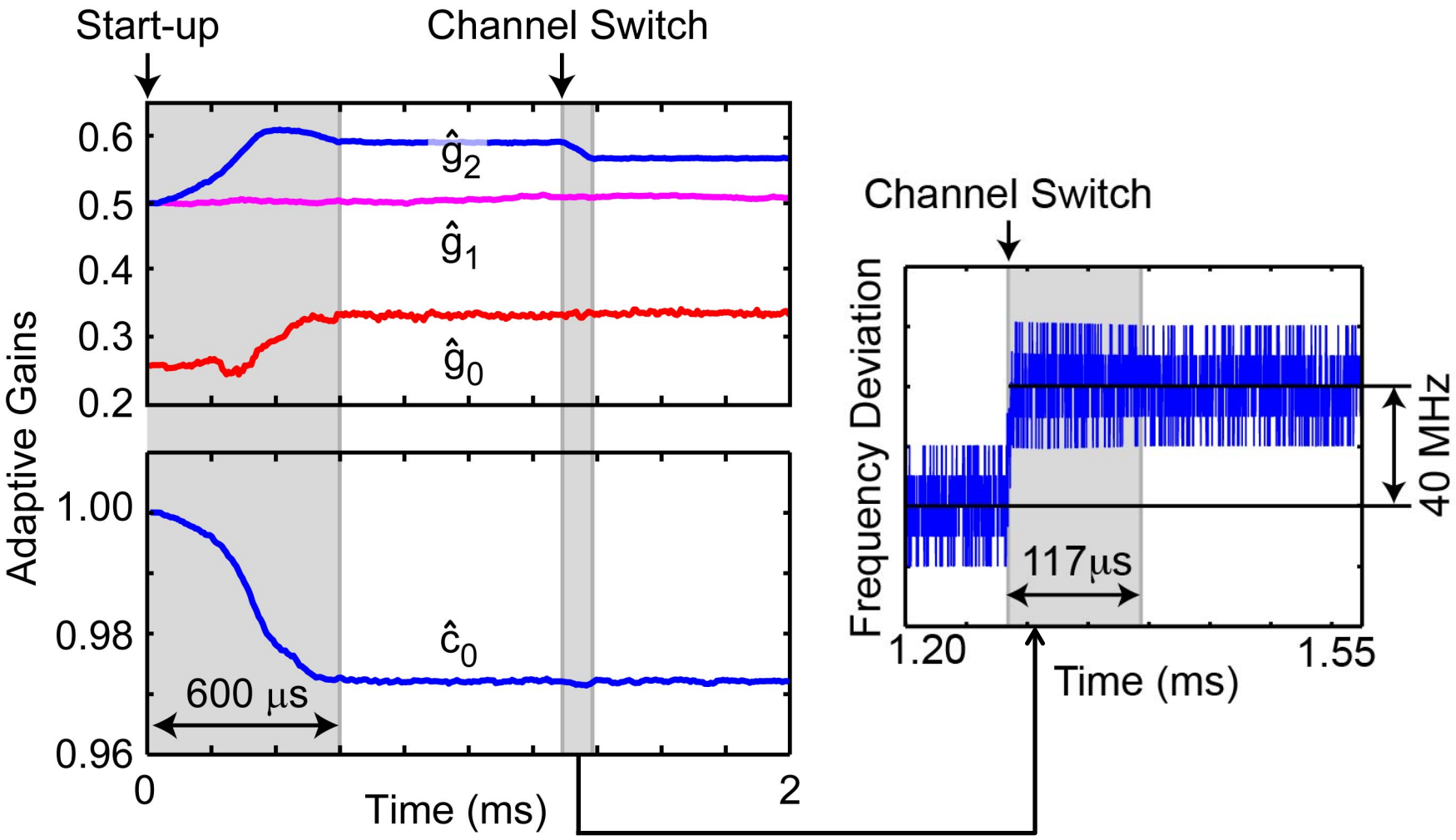
LMS Coefficients and Frequency Deviation



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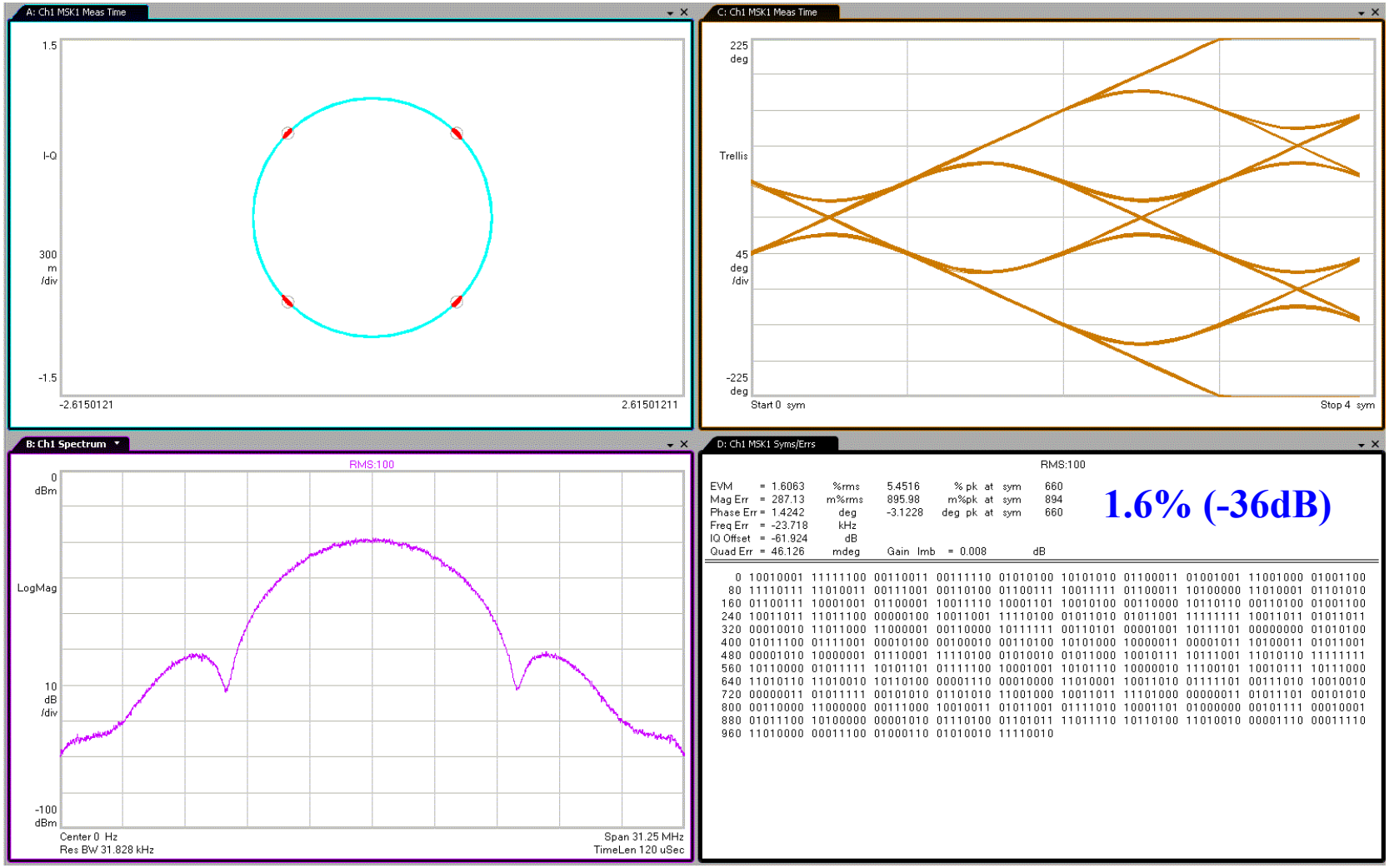
10-Mb/s GMSK Modulation



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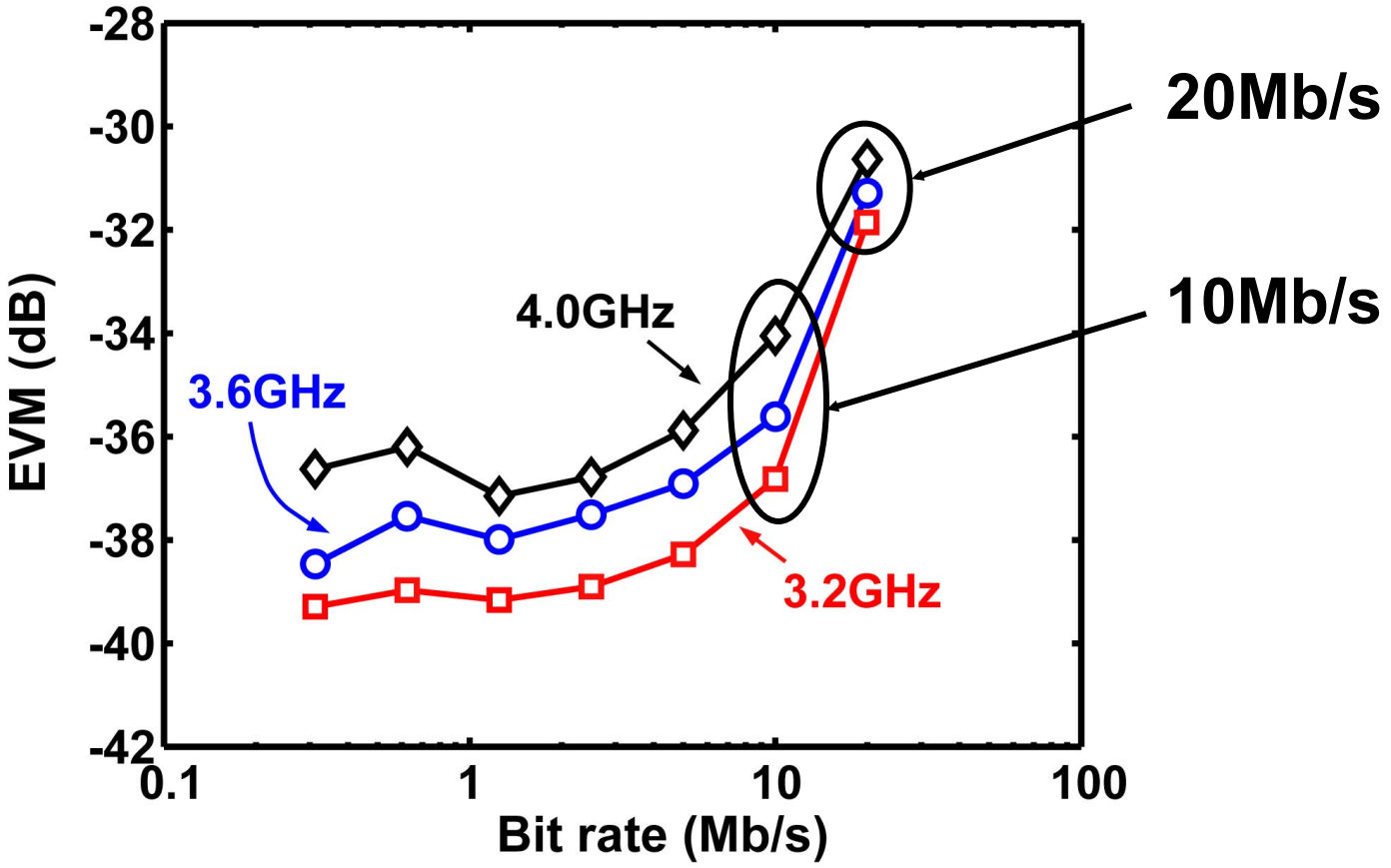
Measured EVM vs. Bit Rate



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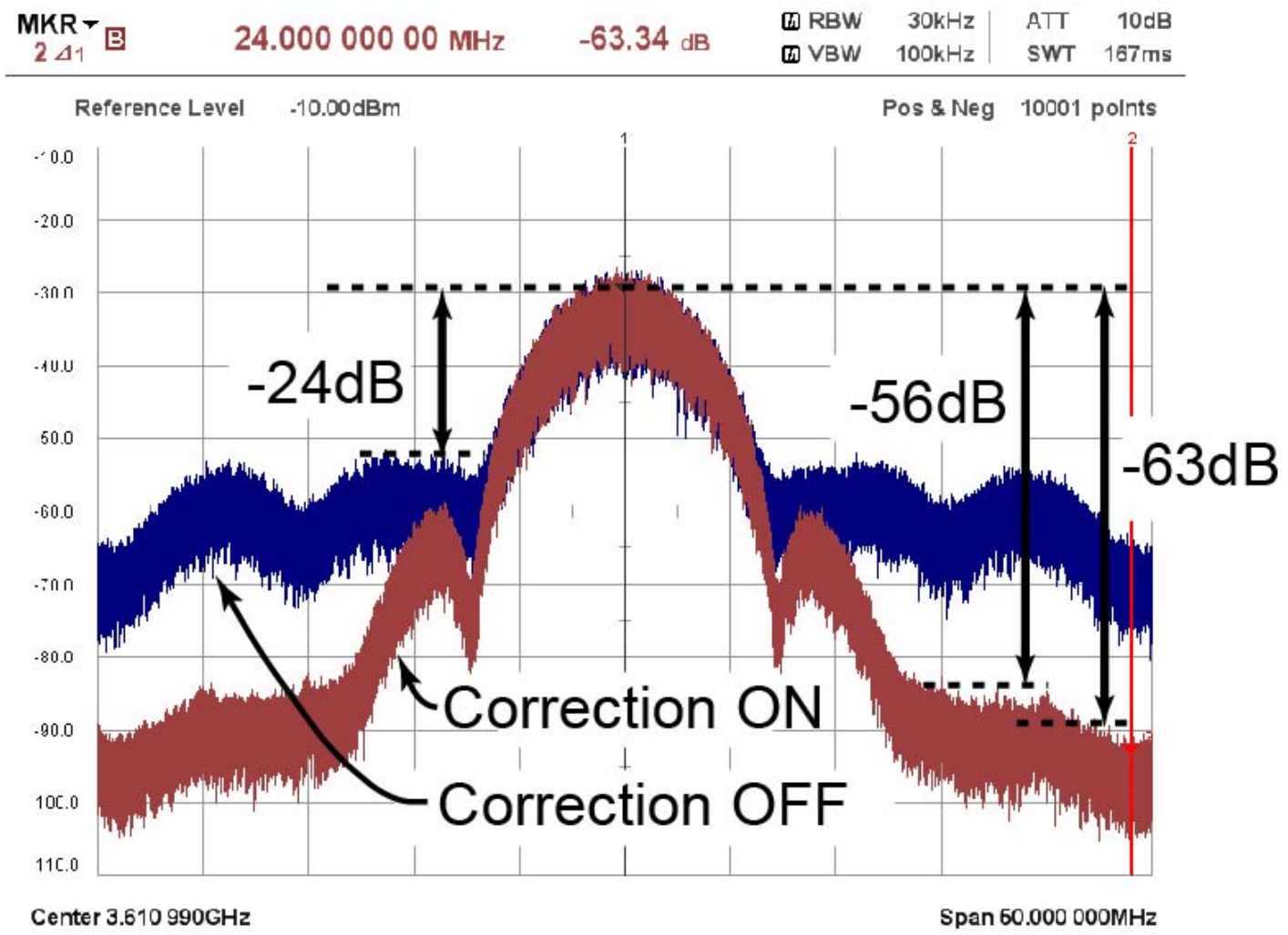
Out-of-band Emission



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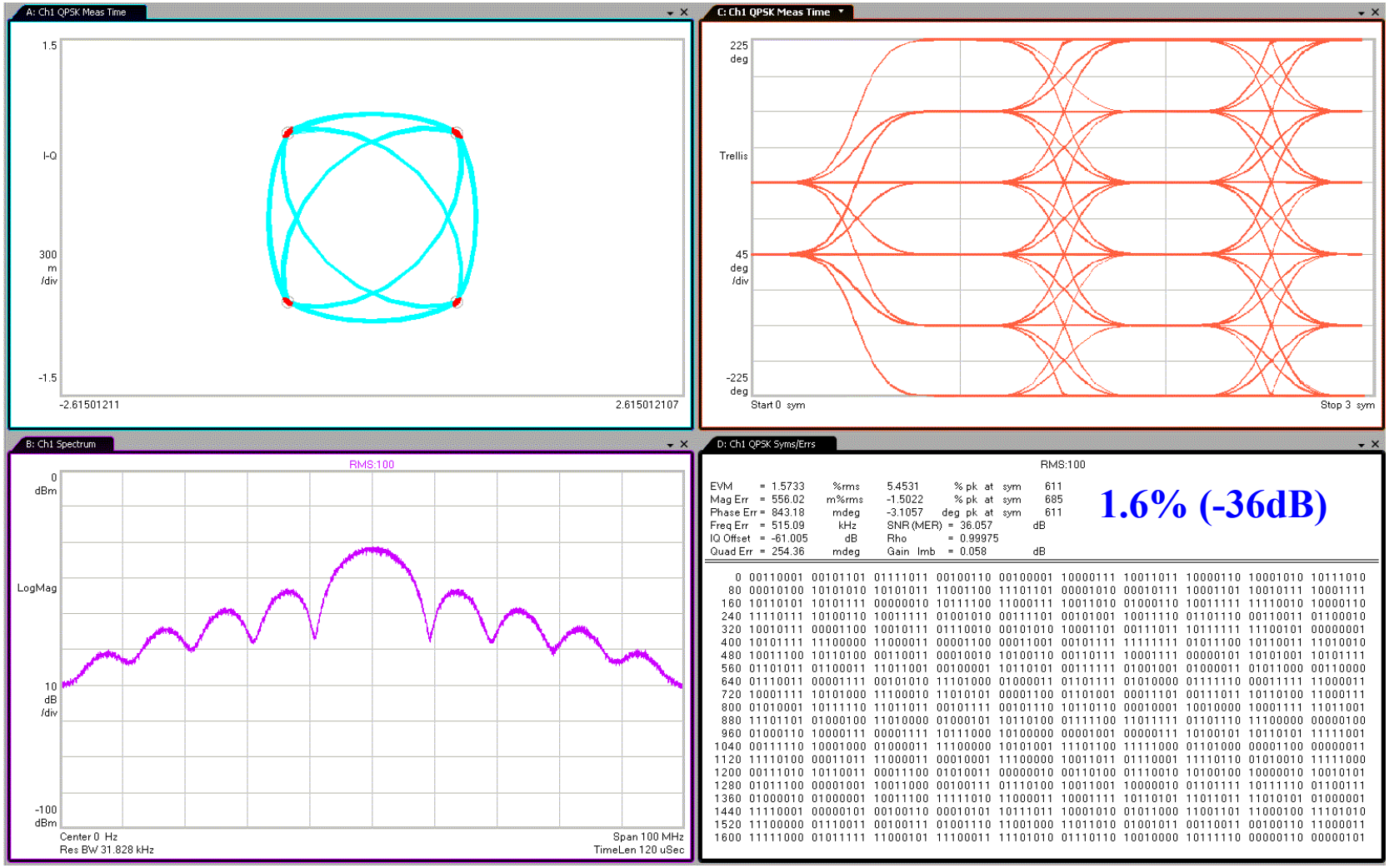
20-Mb/s QPSK Modulation



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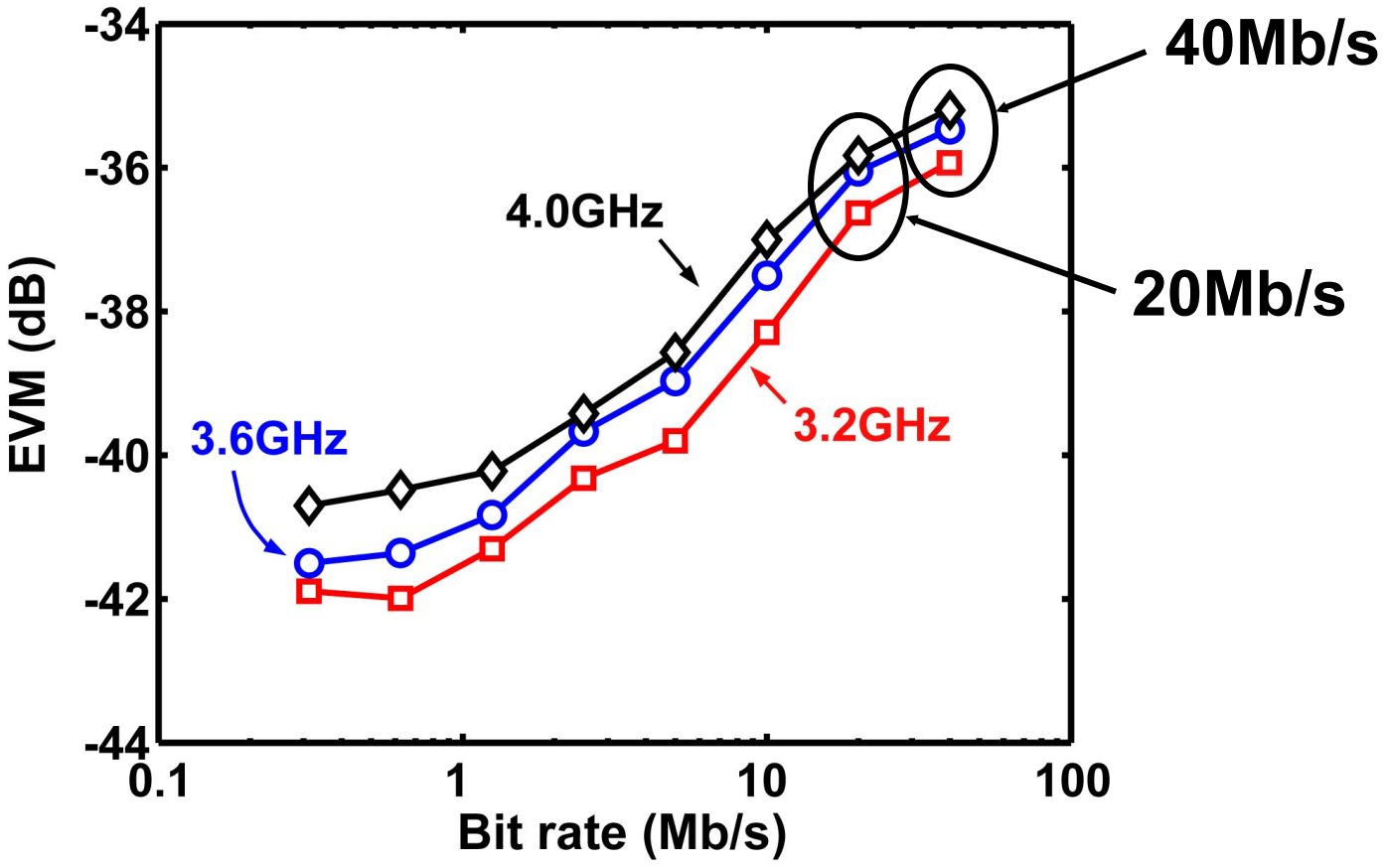
Measured EVM vs. Bit Rate



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Performance Summary

Clock Frequency (MHz)	40	
Output (GHz)	2.9-4.0	
Tuning Range	31.9%	
Power Diss. (mW)	5.0	
PLL Bandwidth (kHz)	312	
Phase Noise (dBc)	-39	
In-band Fract. (dBc) Reference Spur (dBc)	-52 (50 kHz) -76 (40 MHz)	
Start-up Settling Time (μs) Channel Switch Settling Time (μs)	600 117	
Modulation Type	GMSK	QPSK
Maximum Data Rate (Mb/s)	10	20
Energy/bit (nJ/bit)	0.5	0.25
EVM r.m.s. (dB)	-36	-36
Out-of-band Emission (dBr)	-56	-38
Area occup. (mm^2)	0.5	
Process (nm)	65	

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State-of-the-Art Comparison (GMSK)

	P. Su, JSSC11 [25]	H. Shanan, ISSCC09 [31]	This work
Architecture	Phase-Switching	Direct-FM	Direct-FM
Clock Frequency (MHz)	480	52	40
Output (GHz)	2.4	2.4	2.9-4.0
Power Diss. (mW)	62.1	16.0	5.0
Modulation Type	GFSK	GMSK	GMSK
Maximum Data Rate (Mb/s)	40	2	10
Energy/bit (nJ/bit)	1.55	8	0.5
EVM r.m.s. (dB)	-26	-18	-36(*)
Phase Noise (dBc)	N/A	N/A	-39
Out-of-band Emission (dBr)	-49	-57	-56
Area occup. (mm^2)	2.5	1.1	0.5
Process (nm)	180	180	65

(*) EVM equivalent to -39.5dB for a 2.4-GHz carrier

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State-of-the-Art Comparison (QPSK)

	Y.-H. Liu, MTT09 [54]	S. Diao, MTT12 [55]	This work
Architecture	Phase-Switching	Phase-Switching	Direct-FM
Clock Frequency (MHz)	N/A	102	40
Output (GHz)	0.35-0.44	0.915	2.9-4.0
Power Diss. (mW)	3.0	3.5	5.0
Modulation Type	OQPSK	QPSK	QPSK
Maximum Data Rate (Mb/s)	17.5	50	20
Energy/bit (nJ/bit)	0.17	0.07	0.25
EVM r.m.s. (dB)	-23	-24	-36(*)
Phase Noise (dBc)	-45	N/A	-39
Out-of-band Emission (dBr)	N/A	N/A	-38
Area occup. (mm^2)	0.7	0.28	0.5
Process (nm)	180	180	65

(*) EVM equivalent to -55dB for a 0.4-GHz carrier and -44.5dB for 0.9-GHz carrier

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Conclusions

- **Analog PLLs do not scale down as process and are not amenable to noise-cancellation and other calibration algorithms**
- **Digital PLLs exploit CMOS scaling and allow for simple, accurate implementation of digiphase and two-point modulation**
- **Typically, DPLLs require TDCs with tight resolution to achieve low phase noise and fractional-spur level, which increase both power consumption and design effort**

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Conclusions (Continued)

- **DPLLs with Bang-Bang Detectors (i.e. coarse midrise TDCs) in combination with a DTC allows same phase-noise performance and fractional-spur level at much lower power consumption**
- **Fine resolution is only required to DCO and DTC, which can be both improved leveraging oversampling techniques**
- **Bang-Bang DPLLs achieve superior noise/ power trade-off over conventional DPLLs, while reducing design effort**

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