Reverse Short Channel Effects in High-k Gated nMOSFETs

Jin-Ping Han, Sang-Mo Koo, Eric Vogel,
Evgeni Gusev, Chris D'Emic*,*
Curt Richter, John Suehle

Semiconductor Electronic Division, NIST
** IBM T.J. Watson Research Center*

Outline

- Motivation
- Experimental conditions
- Channel length dependence measurements on high-k and control samples
- Possible mechanisms ruled out
- Roles of interface traps & oxide changes
- Conclusions

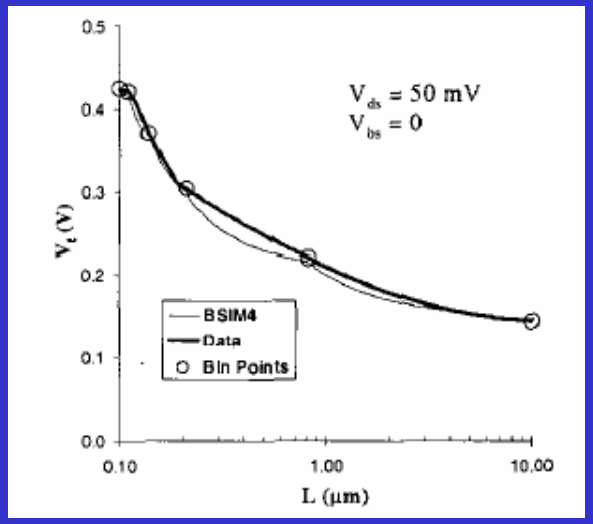
Introduction

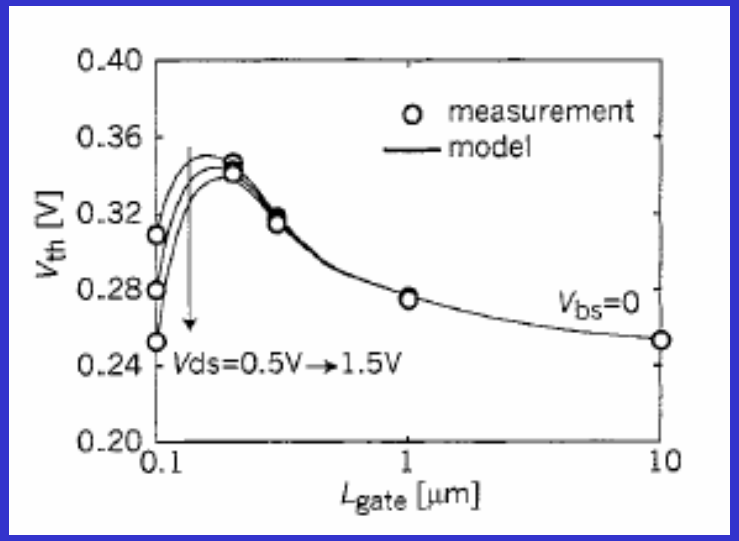
- It's widely believed that high-k dielectric is needed to replace SiO_2 in order to fulfill scaling scenario (ITRS).
- Current focus has been on Hf based dielectric
- Many challenges still exist: mobility degradation, interfacial properties, metal gate integration etc.
- Threshold voltage (V_{th}) characteristics control is of critical importance to achieve high performance for scaling CMOS technology.

Motivation

- The reverse short channel effect (RSCE) refers to an increased threshold voltage (V_{th}) with decreasing channel length (L_{ch}) in MOSFETs

Examples:





Rafael Rios et. al, IEDM '02

Hioraki Ueno et. al, ED 49(10) '02

State of Art about RSCE on SiO_2

1. **RSCE is attributed to a laterally inhomogeneous channel doping profile generated by enhanced diffusion at S/D ends of the channel due to gate reoxidation** (Orlowski, IEDM'89), **silicidation**(Lu, EDL'89) **or originate from damage created by S/D implantation** (NUPAD IV tech dig.'92)
2. **Negative oxide charge due to the interjection of Si-interstitials** (Jocobs,IEDM'93)
3. **Vth roll-up is very sensitive to post-S/D anneal conditions** (Crowder, IEDM'95)
4. **RSCE is caused by enhanced diffusion by impl. damage at S/D** (Nishi, IEDM'95) **.**
5. **The thinner gate oxide exhibits smaller RSCE; impl. N into sub before gate oxide reduce RSCE** (A. Kamgar, IEDM'97)
6. **RSCE is based on respective physical origins:impurity distribution vertical to the channel** (Mattausch, ED'01)
7. **RCSE modulation by Poly-Si doping level is explained in terms of effective oxide thickness change due to poly-Si depletion effects. (**Sadovikov, ED'01)
8. **Channel impurity profile and S/D extension profile control (by RTA) to reduce transient enhanced diffusion therefore RSCE.** (Ineba, ED'02)
9. **RSCE is due to the modeled fixed charge @ S/D ends assuming substrate bias independent** (Arora, EDL'02)
10. **Optimal Phosphorus-assisted low energy Arsenic ion impl supresses the RSCE** (Imai, JJAP'03) **.**

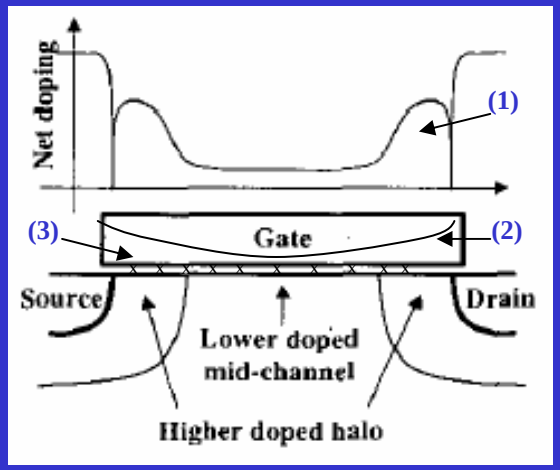
Motivation

Possible causes for reverse short channel effect in high-k gate dielectrics:

(1). inhomogeneous channel doping profile –

(2). gate oxide thickness variation near S/D ends-

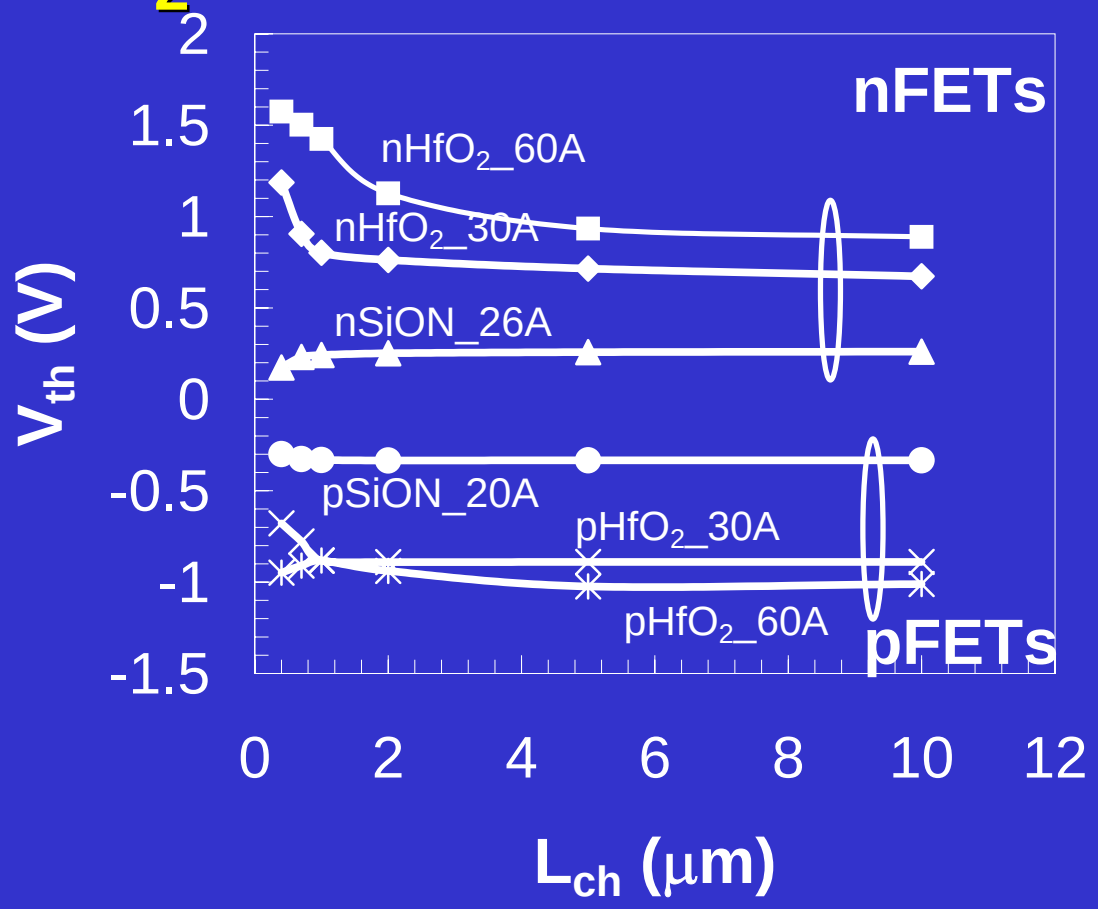
(3). Coulombic/Trapping - Differences in amount of trapping or density of Coulombic scattering centers for e- and h+.



Experimental Conditions

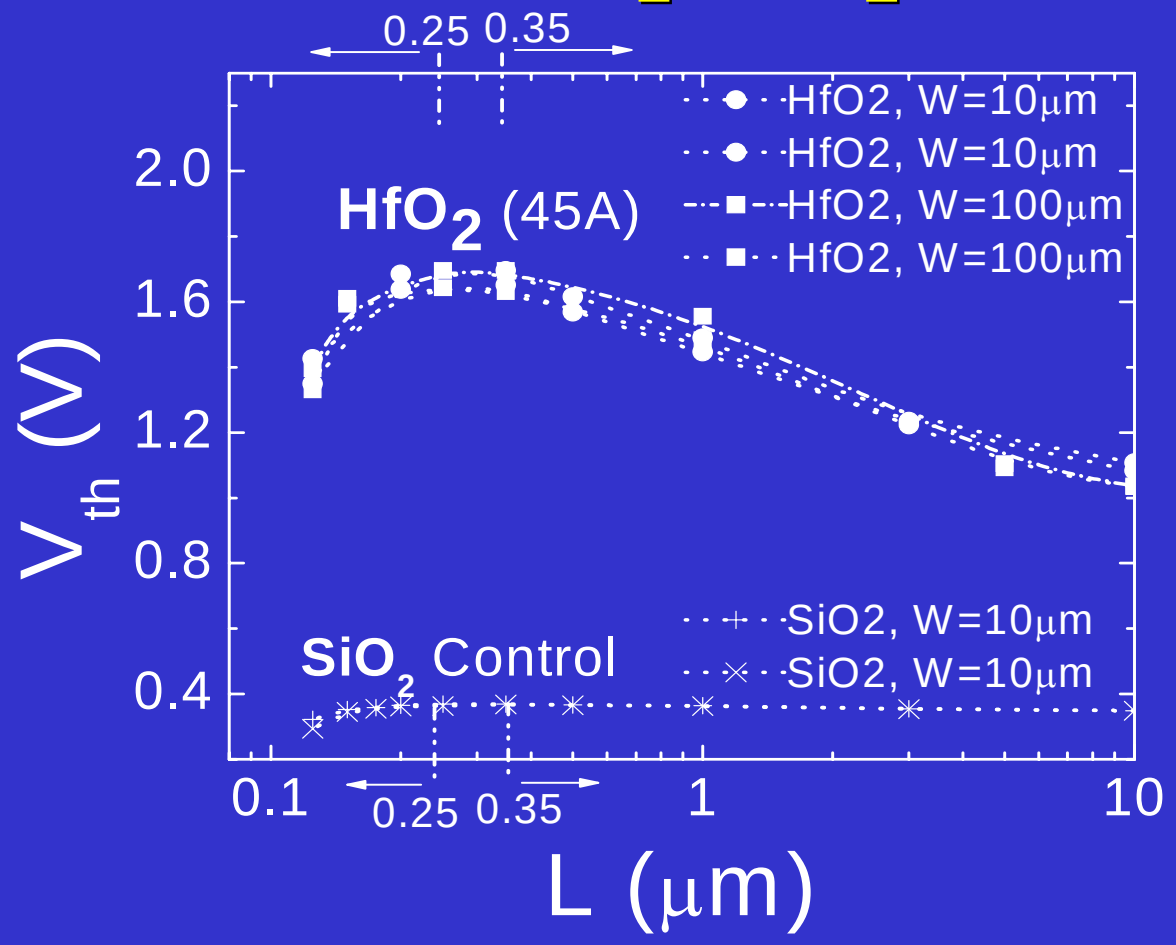
- N- & P-channel MOSFETs with gate dielectric of HfO_2 atomic layer deposited on an ultra-thin layer of silicon oxynitride.
- N- & P-channel MOSFETs with control gate dielectric of silicon oxynitride.
- FETs were polysilicon gated and fabricated using a conventional CMOS flow
- Channel lengths from 0.4-10 μm. Channel width of 50-100 μm.
- EOT of HfO_2 ~ 1.8-2.5 nm, EOT of oxynitride ~ 2.0 nm

Vth vs. Lch of n- & p- MOSFETs (IBM HfO_2/SiON and control SiON)



High-k HfO_2/SiON stack gated MOSFETs have different L_{ch} dependence of V_{th} from SiON gated control samples. n- FETs behave differently from p- FETs.

V_{th} vs. L_{ch} (log scale) of nMOSFETs (Sematech 45A HfO_2/SiO_2 & control SiO_2)



RSCE has been observed on n-FETs gated with 45A HfO_2 for L_{ch}>0.35um, while normal SCE starts to show up when L_{ch}<0.25um. SiO_2 control samples show the normal SCE.

Observation & Explanation

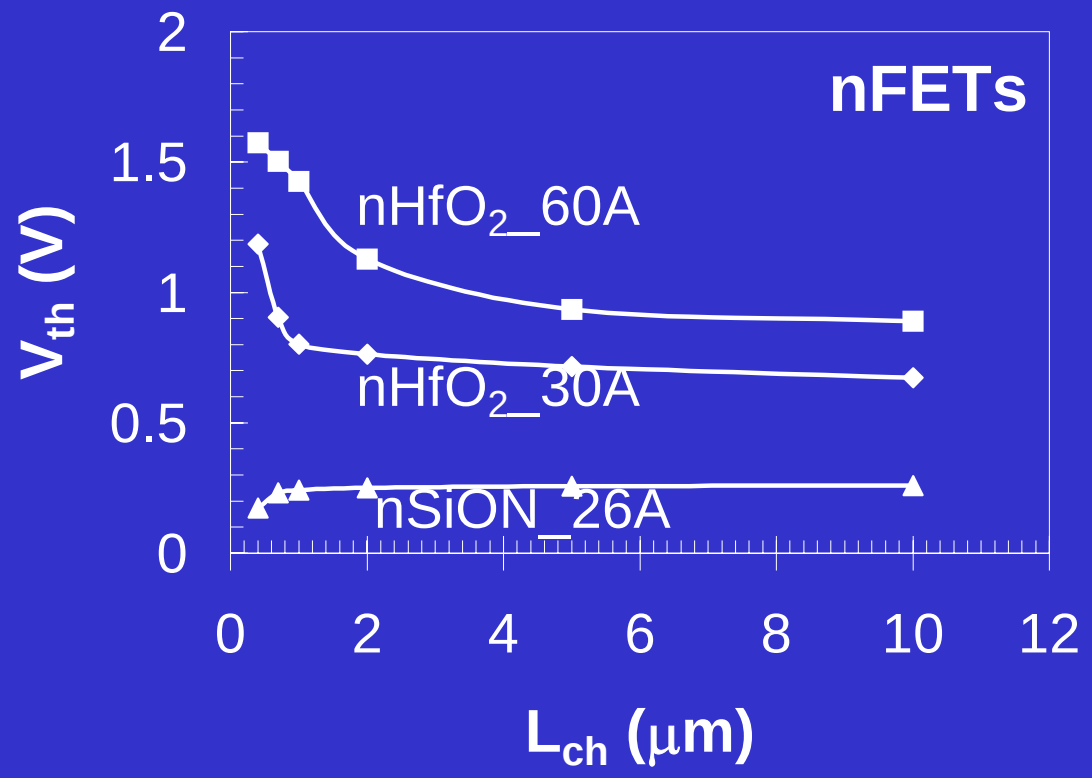
- High-k HfO_2/SiON (SiO_2) stack gated MOSFETs have different Lch dependence of Vth from SiON (SiO_2) gated control samples.
  ➔ different interface and bulk trap properties

- n- FETs behave differently from p- FETs.
  ➔ maybe due to asymmetric distribution of interface trap density cross the band gap (Han, VLSI 03)

- RSCE has been observed on n-FETs gated with HfO_2 for L_{ch} > 0.35um, while normal SCE starts to show up when L_{ch} < 0.25um.
  ➔At least two mechanisms competing in L_{ch} range.

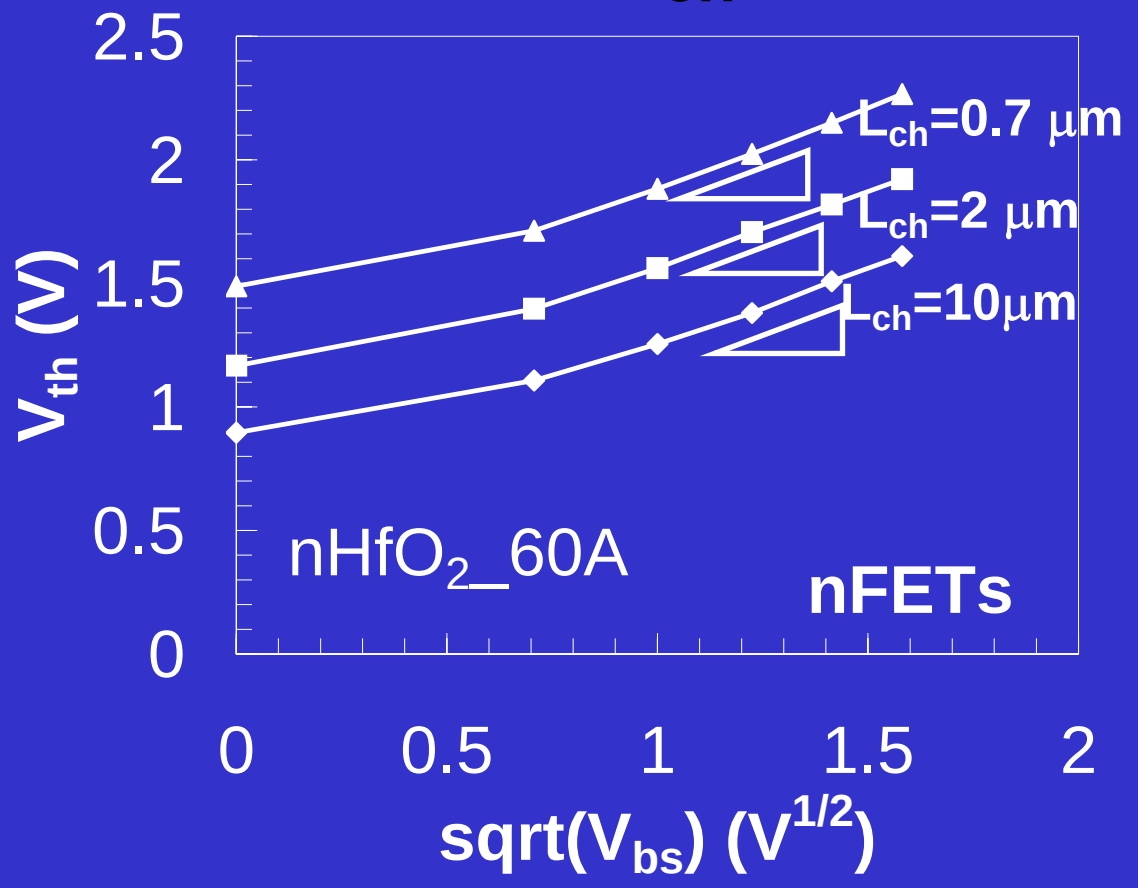
RSCE in nFETs with Lch > 0.35um will be our focus here

Focus on V_{th} vs. L_{ch} of nMOSFETs (HfO_2/SiON & control SiON)



RSCE has been observed on n-FETs gated with 30A HfO_2 and 60A HfO_2 on SiON buffer layers, in comparison with the normal SCE on SiON control nFETs

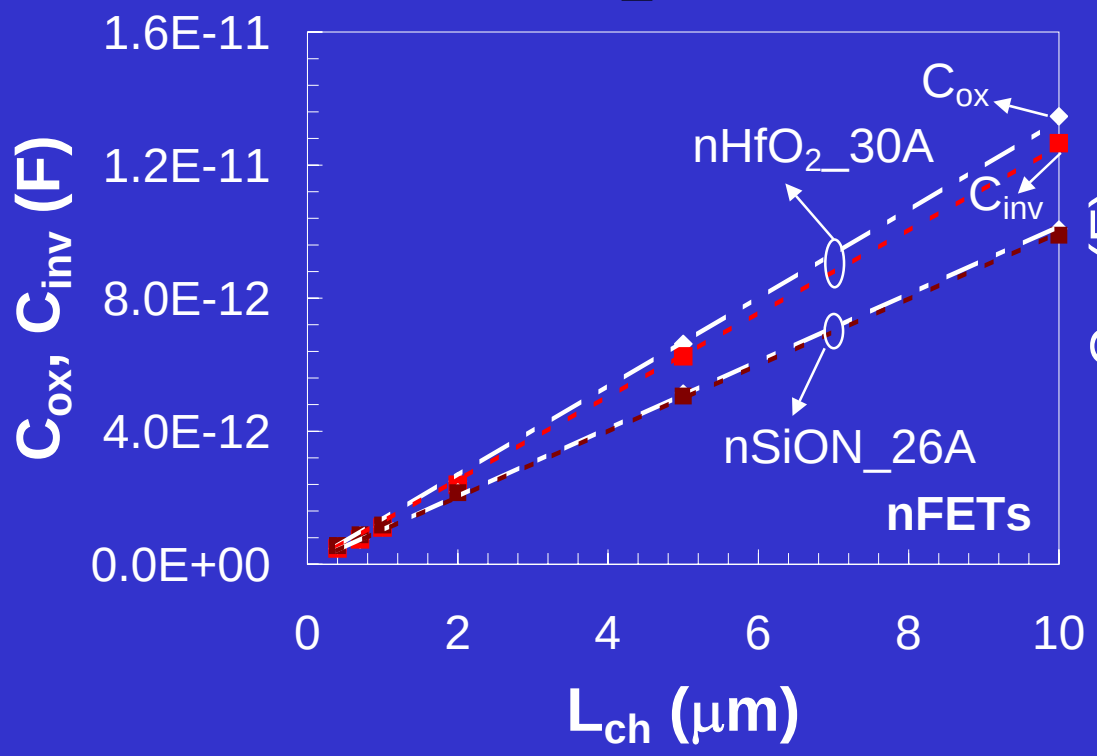
V_{th} vs. sqrt(V_{bs}) of n- MOSFETs with various L_{ch} (60 A HfO_2/SiON)

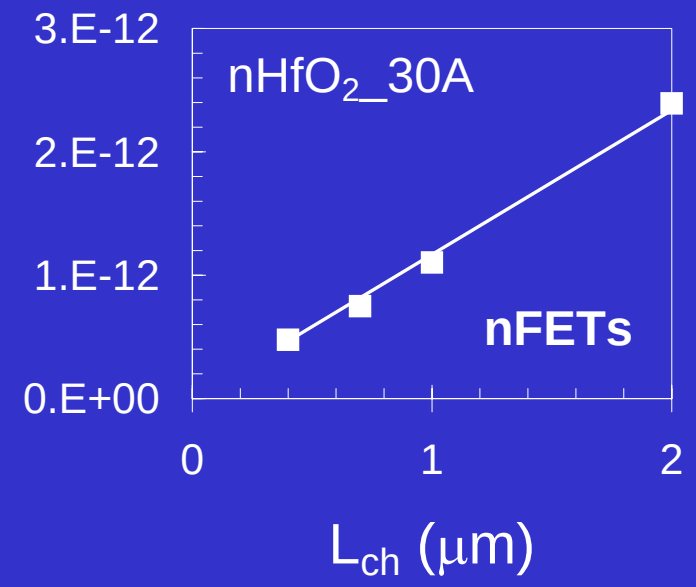


$$V_T \propto \sqrt{N_A\left(V_{bs} + C\right)}$$

Similar slopes for 3 different L_{ch}, indicates no significant dependence of N_{doping} on L_{ch}. It rules out possibility of element diffusion near S/D extension region & surface.

C_{acc} & C_{inv} vs. L_{ch} of nMOSFETs (30 Å HfO_2/SiON & control SiON)





C_{ox} (C_{inv}) is a linear function of L_{ch} for nMOSFETs with SiON and 30 Å HfO_2/SiON, right plot is C_{inv} vs. L_{ch} ($\leq 2\mu m$) for 30 Å HfO_2 case, indicating there is a uniform oxide thickness for FETs of all tested L_{ch}.

Simplified equations about relationships of N_{it}(Dit), N_{ox} & V_{th}, V_{mg}, SS

$$N_{it} \approx \frac{[(V_{th} - V_{mg}) - (V_{th} - V_{mg})_{ideal}]C_{ox}}{qA}$$

$$N_{ox} \approx \frac{(V_{mg} - V_{mg(ideal)})C_{ox}}{qA}$$

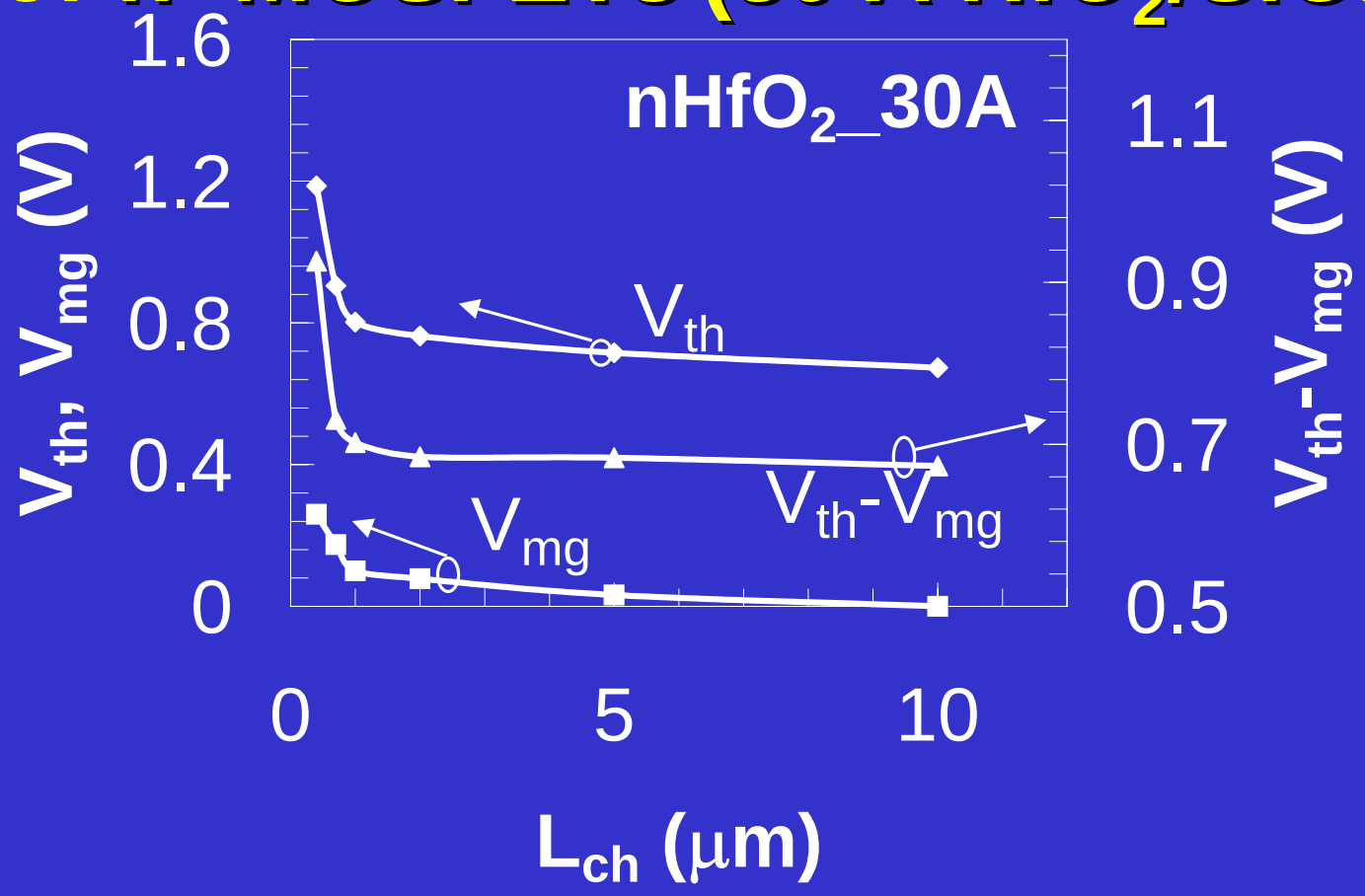
$$SS = \frac{kT}{q}\ln 10(1 + \frac{C_{\min} + qD_{it}}{C_{ox}})$$

(1) $\Delta(V_{th}-V_{mg})$ is proportional to interface trap density, assuming $V_{th(ideal)}$ and $V_{mg(ideal)}$ are constant for all L_{ch}

(2) V_{mg} shift is proportional to fixed oxide charge density

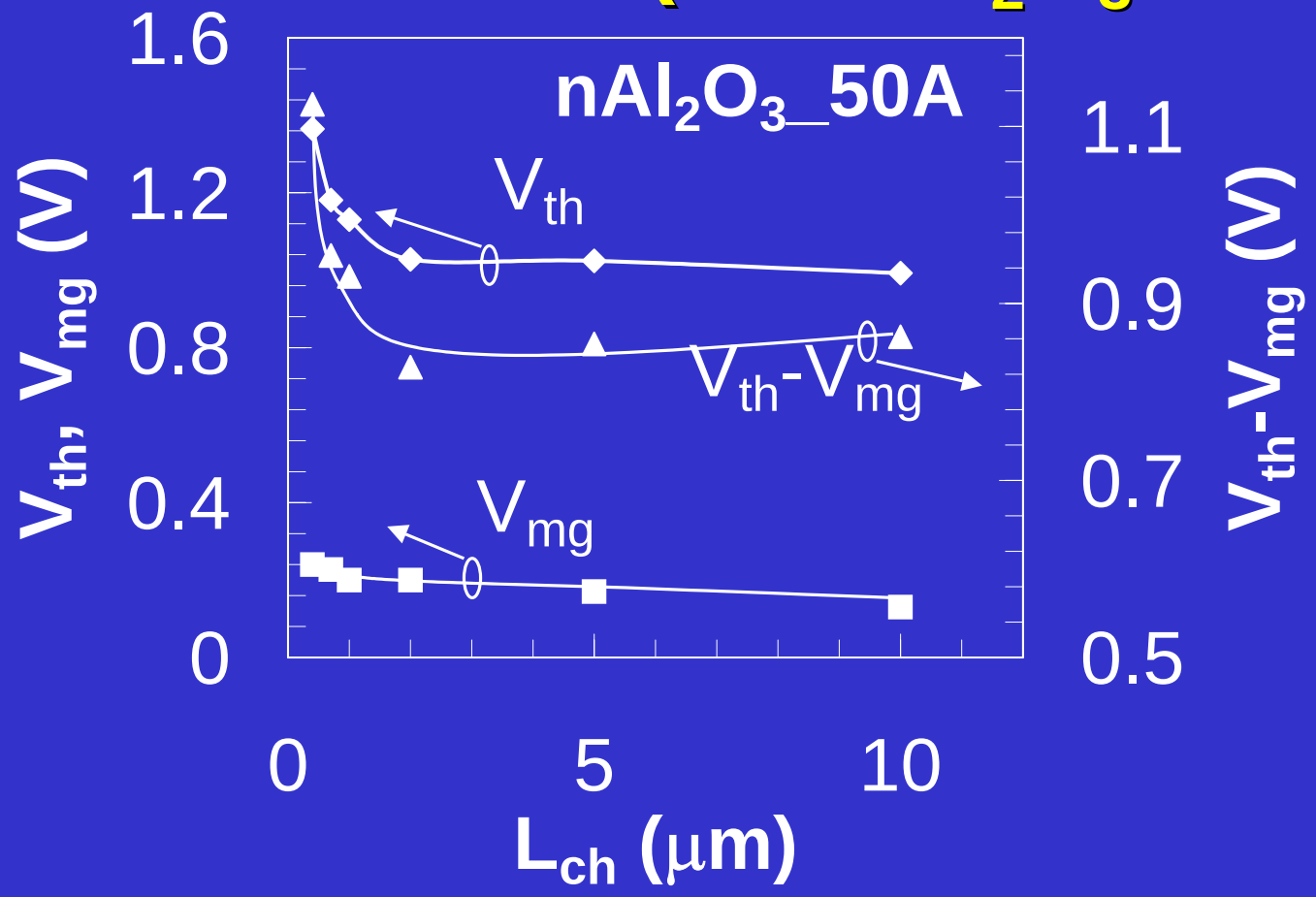
(3) SS is proportional to the interface trap density (including both fast Dit and border traps) in the weak inversion region

V_{th} ,V_{mg} & (V_{th} –V_{mg}) vs. L_{ch} of n- MOSFETs (30 A HfO_2/SiON)



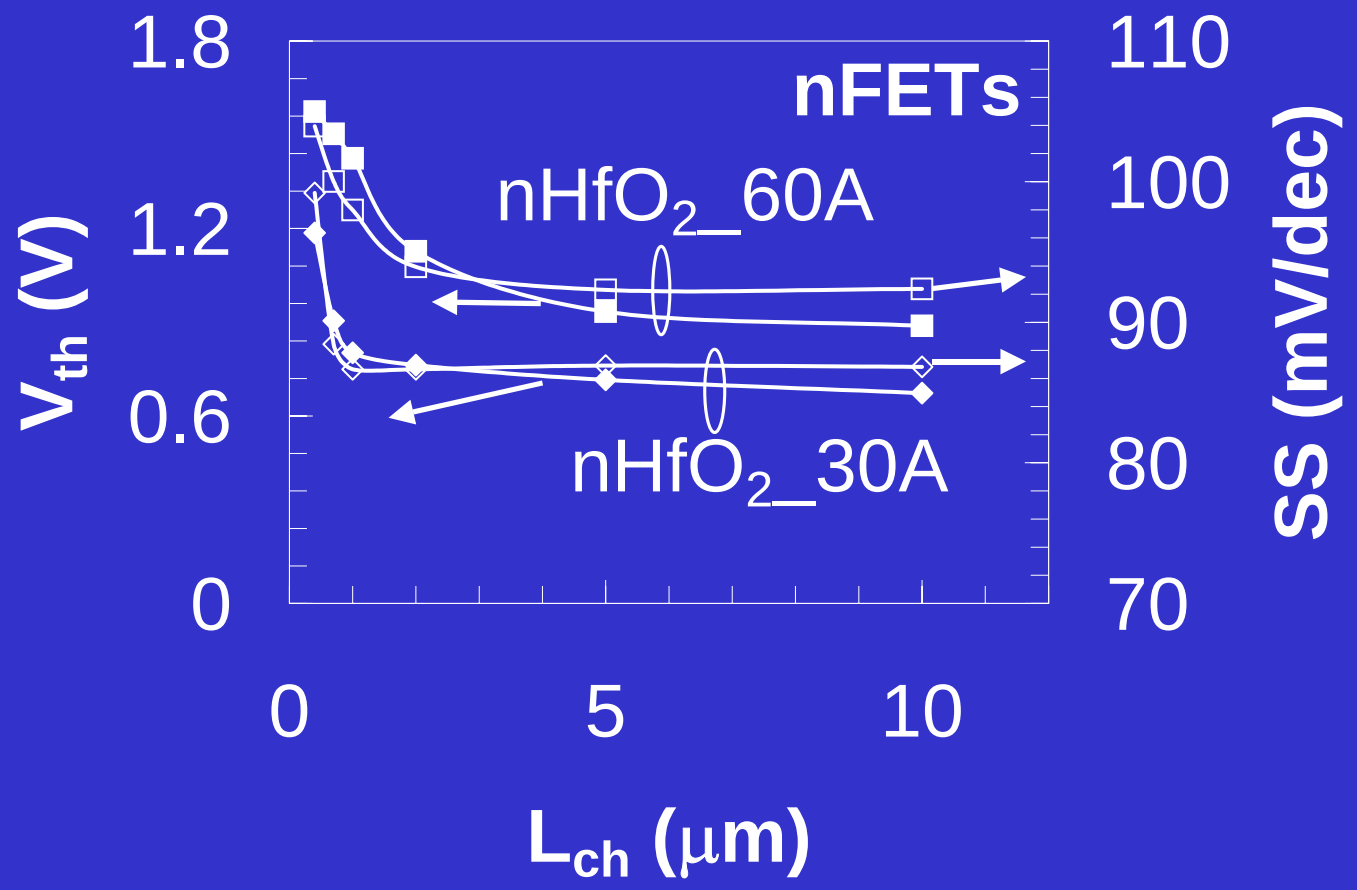
V_{th} ,V_{mg} and their difference (V_{th} -V_{mg} , right hand ordinate) as a function of L_{ch}, suggesting that both interface traps and oxide charge may contribute to the RSCE.

V_{th} ,V_{mg} & (V_{th} –V_{mg}) vs. L_{ch} of n- MOSFETs (50 A Al_2O_3/SiON)



Pilot data obtained in 50 Å Al_2O_3 gated nFETs. Again, interface traps are the major cause of the RSCE whereas oxide charge play minor role here.

V_{th} & SS vs. L_{ch} of n- MOSFETs (30A & 60A HfO_2/SiON)



V_{th} and SS as a function of L_{ch} of nMOSFETs (30 Å and 60 Å HfO_2, respectively). Both, V_{th} and SS, show similar dependence on L_{ch}. SS is proportional to interface traps.

Summary

- The RSCE has been observed in high-k gated samples (HfO_2 on SiON(SiO_2) buffer, Al_2O_3 on SiON buffer), while control samples (SiO_2 or SiON) show normal SCE.

- An inhomogeneous channel doping profile generated by dopant enhancement near the S/D extension region has been ruled out as a possible cause.

- Strong evidence indicates that channel length dependent interface traps may be the major cause of the RSCE in high-k gated MOSFETs.