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The Effect Of Bonding Conditions On The Electrical Properties Of Solder Joints Fabricated By Mechanical Caulking Using Reflowed Sn Bumps

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- Introduction
- Our approach
- Part Ⅰ. Formation of Through Si Via Electrode
- Part Ⅱ. Formation of Reflowed Sn bumps and Interconnection lines
- Bonding and Electrical Test Results
- Summary

Introduction

- ✓ **Advantage of 3D-stacked chip technology**
  - ➢ High density
  - ➢ System integration improved
  - ➢ Miniaturization & light-weight
- ✓ **Advantage of method of through via hole**
  - ➢ Extremely small
  - ➢ Good electrical transmission characteristics
  - ➢ Cost reduction

Introduction of mechanical caulking technology

✓ **Mechanical caulking technology (By Hitachi-Renesas)**

Source by ECTC 2006

✓ **The back side of chip makes through via hole electrode & upper side of chip makes metal bumps**

✓ **Bonding between the chips is achieved by deformation-injection of metal bump on a chip into the through via hole in the other chip**

Characteristics of mechanical caulking technology

➢ Advantages of Mechanical caulking technology

- ✓ Simple process
  :CMP & Via filling process are not necessarily
- ✓ Cost reduction
  :Simple process
- ✓ Low temperature process
  :Mechanical bonding
- ✓ Good Reliability
  :Improved reliability due to unfilled via

➢ Disadvantages of Au stud bump formation

- ✓ High cost of bump materials
- ✓ Batch process
- ✓ Au stud bump:Relatively hard ➡ Mismatch problem

Source by ECTC 2005

Our approach

➢ Our Method

Sn bump (reflowed) & via bonding

➢ Advantages of Sn bumps over Au stud bumps

- Low cost of bump materials
- Wafer level bumping possible
- Soft Sn bumps ➡ Easy deformation
- Metallurgical bonding Between Sn and Au/Cu

Electrical path

✓ **Through via electrode and Reflowed Sn / Cu bumps on substrate**

➢ **Chip side**

➢ **Substrate side**

➢ **Flip chip bonding**

Mask Design

AC_NW
AC_NE
AC_SW
AC_SE
0. 81 mm
2 mm
2.16 mm
1.47 mm
2 mm
16×10 array
Total: 172 bumps
5 mm × 5 mm
+++ Mask +++
:deep RIE
:sub. chip metal line
:via chip metal line

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Experimental procedure

- Thin Si wafer preparation
- Thin film (UBM) deposition
  - DC magnetron sputtering system
  - Au (50 nm) / Cu (1 ㎛) / Ta (50 nm)
- Metal line & Vias hole formation
  - Photolithographic process
  - Wet chemical etching
- Glass-bonding for handling
  - To use a crystal wax, glass bonding
- Si wafer deep RIE(Reactive Ion Etching)
- Dicing and deposition of electrode
  - To use a sputter, Au layer deposition
  - To use an electroplating, Cu layer formation
  - To use a sputter, Cu / Ta layer deposition
- Patterning electrode and dicing

Source of KAIST

Metal line patterns

<Mask design>

<After pattering metal line>

Through Si via (TSV) formation

<Mask design>

<Top view after electroplating>

Through-Si via formation
Bosch process
(NNFC)

→

Cu/Ta deposition in TSV
(Cu/Ta: 1㎛/90nm)
IMP sputtering
(ICP/Sub.: 20/40W)

→

Cu electroplating
DC 1.0mA/cm^2
5hrs (~1.2㎛/hr)

Cross-section Image of Electrode in the Through Si via (TSV)

<Cross-sectional view after electroplating>

TSV: diameter 53㎛, depth 100㎛

EP thickness: 6~8 ㎛

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Experimental Procedure

- **SiO_2/Si wafer cleaning**
  - In TCE, ACE, MET ultrasonic for 5min
- **Thin film (UBM) deposition**
  - DC magnetron sputtering system
  - Ti (50 nm) / Au (50 nm) / Cu (1 ㎛) / Ti (50 nm)
- **Metal line & Via hole formation**
  - Photolithographic process
  - Wet chemical etching
- **Copper plating:Cu (5 ㎛) bump formation**
  - Current:5 mA / cm^2
  - Deposition rate:0.17 ㎛ / min
- **Tin plating:Sn (20 ㎛) bump formation**
  - Current:5 mA / cm^2
  - Deposition rate:0.20 ㎛ / min
- **Sn / Cu bump reflow**

Metal-line Patterns

The metal line patterns on the SiO_2/Si

Via hole formation

PR on the interconnection lines (Substrate side)

Sn / Cu bump formation (SEM image)

Sn / Cu Bump Reflow Condition

- **Sn / Cu bump reflow condition**
  - **Peak Temperature:275 ℃**
  - **In the flowing forming gas (95%N_2+5%H_2)**
  - **In Rapid Thermal Annealing System (RTA)**
  - **Fluxless**

Reflow condition

	Temp.	Time
Preheating - Zone	0 ~ 275 ℃	25 sec.
Reflow - Zone	275 ℃	12 sec.

SEM Images of Reflowed Bumps

➢ Reflow bump condition

- ✓ Bump composition: Sn(20 ㎛) / Cu(5 ㎛)
- ✓ Bump size: Φ 60 ㎛ (height: 26 ~ 27 ㎛)
- ✓ Shape: Domed

Reflow Method Comparison

➢ Sn / Cu bump reflow condition-1

- Peak Temperature:270 ℃
- In the flowing forming gas (95%N_2+5%H_2)
- In Rapid Thermal Annealing System (RTA)
- Fluxless

Reflow condition

➢ Sn / Cu bump reflow condition-2

- Peak Temperature:270 ℃
- In atmosphere
- In Reflow Machine
- Fluxless

Reflow condition

Reflow Method Comparison

RTA	Temp.	Time
Preheating Zone	0 → 270 ℃	15 sec.
Reflow - Zone	270 ℃	10 sec.

Reflow machine	Temp.	Time
Preheating Zone	0 → 270 ℃	300 sec.
Reflow - Zone	270 ℃	30 sec.

Reflow Method Comparison

✓ **RTA (Rapid Temperature Annealing)**

IMC (Cu_6Sn_5) thickness = 2.4 ㎛

✓ **Reflow Machine**

IMC (Cu_6Sn_5) thickness = 4.8 ㎛

➢ **The IMC (Cu_6Sn_5) thickness of Reflow Machine is thicker than that of the RTA.**

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SEM images of through-hole Solder Joints

Observed cross-sections of interconnection area between Sn / Cu bumps and through-hole electrodes on silicon substrate (Pressure: 40 N / Temperature: Room Temperature / Time: 60 sec.)

SEM images of through-hole Solder Joints

Observed cross-sections of interconnection area between Sn / Cu bumps and through-hole electrodes on silicon substrate (Pressure: 20N / Temperature: 270 ℃ / Time: 60 sec.)

Electrical Resistance (DC)

➢ Mask design for DC measurement

➢ Chip condition

Via size: Φ 39 ~ 40 ㎛ (height: 90 ㎛)

Bump size: Φ 60 ㎛ (height: 26 ~ 27 ㎛)

Bump composition: Sn(20 ㎛) / Cu(5 ㎛)

Number of bumps: 160 ea (daisy chain type)

Electrical Resistance (DC)

➢ DC contact resistance

$$R_{measured} = (R_{via} + R_c + R_2) \times n + (2R_1 - R_2)$$

Conductor line(R_2) calibration

$$R_2 = \rho_{\text{sheet resistanc}} \times t_{\text{conductor line thickness}} \times \frac{L_{\text{conductor line length}}}{W_{\text{conductor line width}} \times t_{\text{conductor line thickness}}}$$

$P'_{\text{sheet resistance}}$=45 mΩ (Substrate)

$P''_{\text{sheet resistance}}$=29 mΩ (Chip)

$W_{\text{conductor line width}}$ = 120 ㎛

$L_{\text{conductor line length}}$ =90 ㎛

✓ **$R_2 = R_2' + R_2''$ = 45 X 90/120 + 29 X 90/120**
= 444 mΩ

$W_{\text{conductor line width}}$ = 120 ㎛

$L_{\text{conductor line length}}$ =1880 ㎛ / 270 ㎛

✓ **$R_1 = R_2' + R_2''$ = 45 X 270/120 + 29 X 1880/120**
= 806 mΩ

➢ Schematic of flip chip via

Electrical Resistance (DC)

- **Bonding condition-Sample 1**

Bonding Pressure: 20 N

Bonding Temperature: 270 ℃

Bonding Time: 60 sec.

	$R_{via}+R_c$: per bump
Left-line	33 mΩ
Right-line	36 mΩ

- **Bonding condition-Sample 2**

Bonding Pressure: 20 N

Bonding Temperature: 270 ℃

Bonding Time: 30 sec.

	R_2+R_c: per bump
Left-line	38 mΩ
Right-line	32 mΩ

- **Bonding condition-Sample 3**

Bonding Pressure: 40 N

Bonding Temperature: R. T.

Bonding Time: 60 sec.

	R_2+R_c: per bump
Left-line	35 mΩ
Right-line	34 mΩ

Multiple Reflows Test Condition

- Peak Temperature: 250 ℃
- In the atmosphere
- In Reflow machine
- Fluxless

	Time	Temperature
Preheating zone	90 sec.	0 ℃ → 250 ℃
Reflow zone	120 sec.	250 ℃
Cooling zone-1st	90 sec.	250 ℃ → 30 ℃
Cooling zone-2nd	300 sec.	30 ℃

Effect of multiple reflows

- **Sample 1 (bonding condition; 20 N / 270 ℃ / 60 sec.)**

$R_{via}+R_c$: per bump	0 → 1st time→ 2nd times
Left-line	39.23 → 45.41 → 47.57 mΩ
Right-line	44.23 → 44.21 → 62.00 mΩ

- **Sample 1 (bonding condition; 20 N / 270 ℃ / 30 sec.)**

$R_{via}+R_c$: per bump	0 → 1st time→ 2nd times
Left-line	46.09 → 57.45 → 56.01 mΩ
Right-line	33.85 → 44.11 → 46.26 mΩ

✓ **The electrical resistance was increased after increased after multiple reflows**

Summary

- The reflowed Sn bumps and through via hole electrodes were successfully joined through the plastic deformation of Sn bumps.
- The contact resistance of solder joints was very low.
- The contact resistance was not sensitive to the bonding pressure, bonding temperature, and bonding time.
- The electrical resistance was slightly increased after multiple reflows.

Thank You!