

## Single-electronics: the story so far

- For small enough structures and low enough temperatures, Coulomb charging effects can determine the conducting properties of circuits.
- Two-terminal double-junction devices can show complicated (Coulomb staircase)  $IV$  curves.
- Multiterminal devices can show transistor-like functionality, with substantial current switching modulated by the positions of individual electrons.

Main driver for possible applications:

- Need  $E_c = e^2/C_{eq} \gg k_B T$ , so want smallest junctions possible.  
SIZES OF THINGS: for  $E_c = 50 k_B T$  at 300 K, need  $C_{eq} \sim 0.1$  aF.

## Implementations of single electron devices

Several different ways of making SETs:

- Shadow-evaporation + oxidation of Al  
Most common approach, best suited for large-scale fabrication of arrays.
- Oxidation of silicon  
Compatibility / ease of integration with Si
- Chemically-aided approaches  
Trapped nanoparticles; AFM contacting; molecular devices.

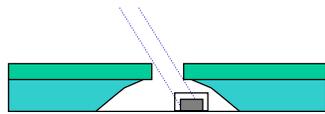
## Shadow evaporation and oxidation of Al

Takes advantage of ease of growth of thin, high-quality  $\text{Al}_2\text{O}_3$  for tunnel barriers.

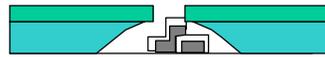
Uses geometry to make smallest possible junctions.



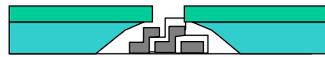
Double-layer resist for e-beam lithography leads to overhang.



Evaporate at an *angle*. Then oxidize for controlled length of time.



Evaporate straight down - forms first junction. Then oxidize for controlled length of time.



Third evaporation forms second junction..

source island drain

## Shadow evaporation and oxidation of Al

- Lateral size of junction overlap determined by resist thicknesses (well-controlled) and angles (also well-controlled).
- By tilting in different directions, can make complicated structures:

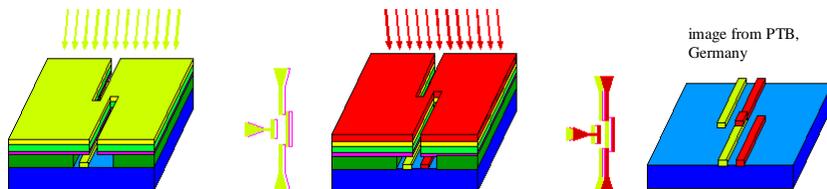


image from PTB, Germany

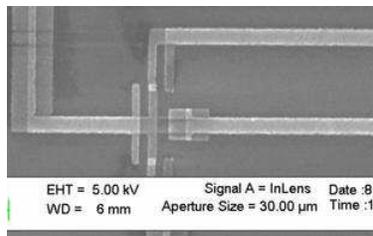
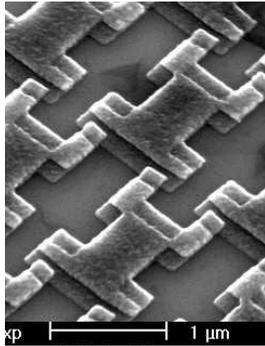


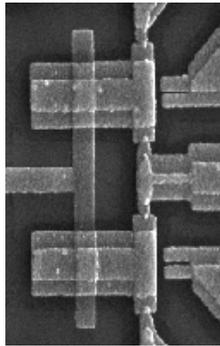
image from KTH, Sweden

## Shadow evaporation and oxidation of Al



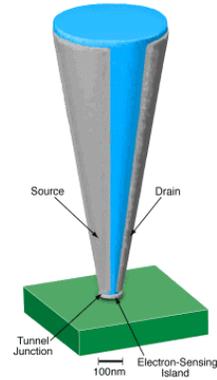
2d Josephson junction array

image from Mooij, Delft, Netherlands



Inverter from two coupled SETs

image from Mooij, Delft, Netherlands

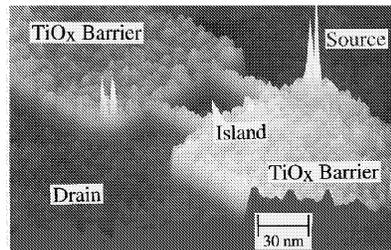
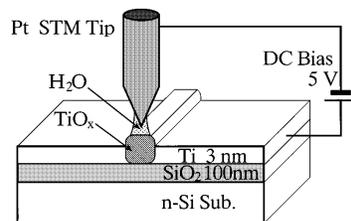


SET on tip of drawn glass fiber

image from Bell Labs

## Local oxidation

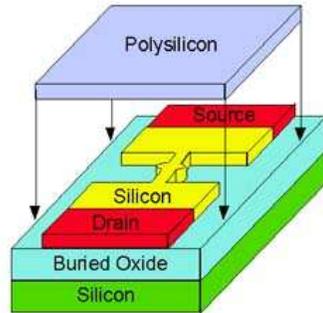
images from Matsumoto *et al.*, APL 68 34 (1996).



- Recall tunneling transistor: local electrochemical oxidation (anodization) used to convert continuous Ti strip into island + insulating tunnel barriers.
- Painstaking fabrication, but payoff is SET with some room-temperature functionality.

## Oxidation of Silicon

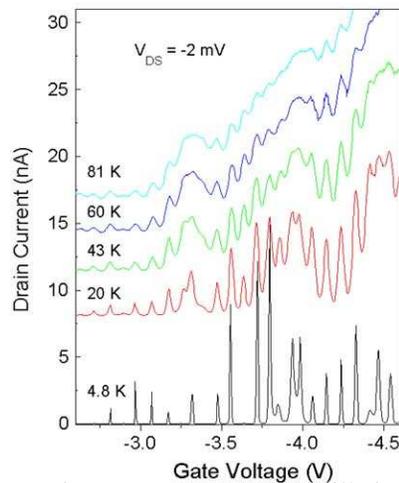
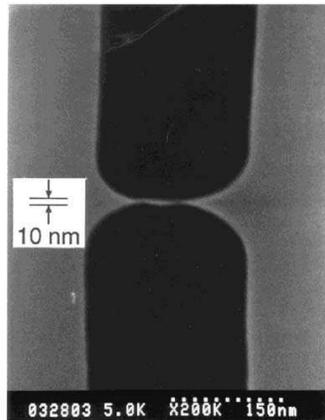
image from Steve Chou, Princeton



- **In-plane size of QD** defined by **e-beam lithography and reactive-ion etching**
- **Vertical size of QD** defined by **top Si layer thickness**
- **Si QD size Reduced** during gate oxidation
- **Hard-wall confinement**

## Oxidation of Silicon

images from Steve Chou, Princeton



Even for an island as small as this, getting room temperature oscillations is a real challenge.

## Nanocrystalline silicon

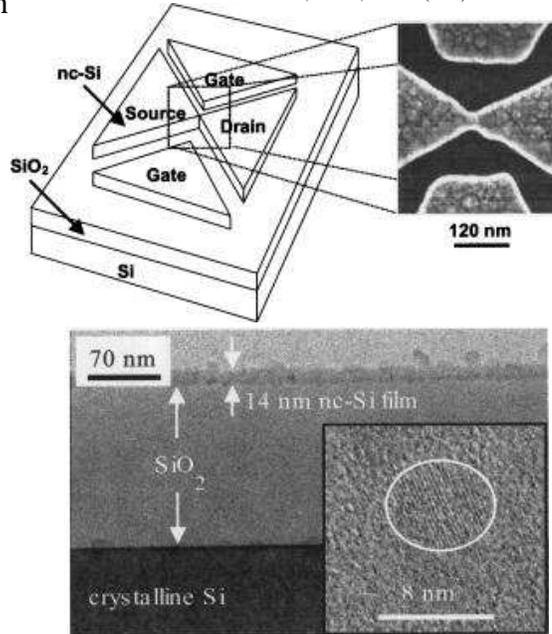
Tan *et al.*, JAP **94**, 633-637 (2003)

Tan *et al.* work with doped nanocrystalline Si deposited by PECVD.

Nanocrystalline regions surrounded by amorphous matrix.

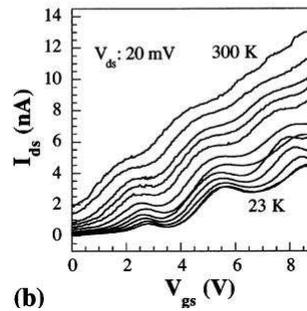
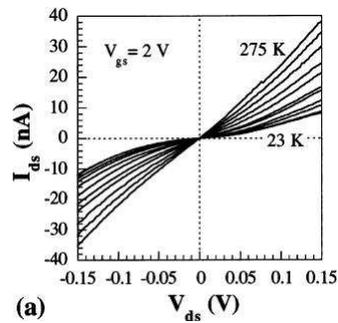
Oxidize for known amount of time to form barriers.

Gated *laterally*.



## Nanocrystalline silicon

Tan *et al.*, JAP **94**, 633-637 (2003)

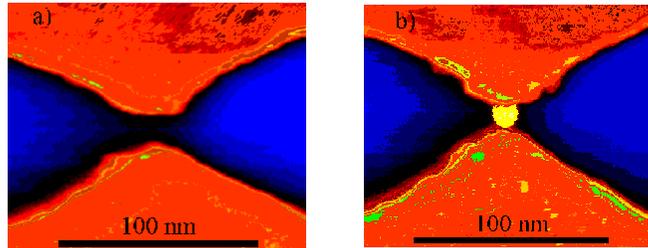


Grain size is sufficiently small that some gate modulation of conductance is detectable even at 300 K.

Still a far cry from a workable device.

## Trapped nanoparticles

images from Dekker, Delft



One approach: use chemical fabrication to make nanoparticles for use as SET islands.

Trap particles between lithographically created electrodes.

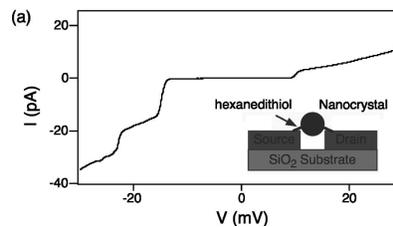
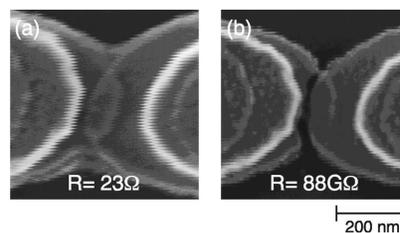
Electrostatic trapping in above – nanoparticle drawn to region of high local electric field as source/drain are biased.

## Trapped nanoparticles

images from Park *et al.*, APL 75, 301 (1999).

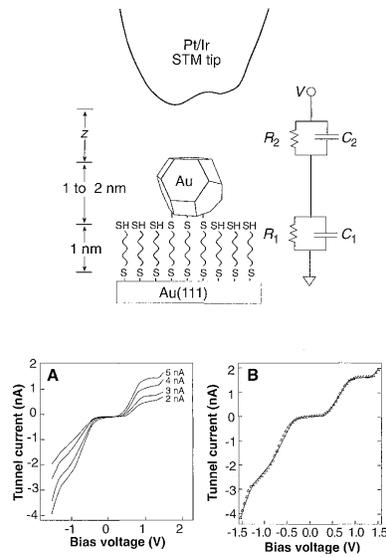
Alternative:

- Start with continuous metal electrodes on top of insulated metallic substrate, to be used as a gate.
- Dust surface to decorate with nanoparticles, such as chemically synthesized CdSe nanocrystals.
- Break into separate source-drain electrodes by “electromigration”, and sometimes nanocrystal ends up ideally positioned to act as island.



## Nanoparticles on surfaces

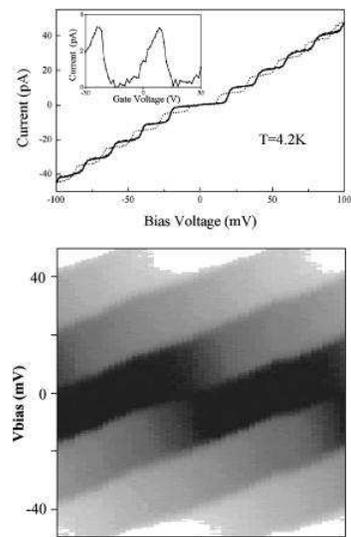
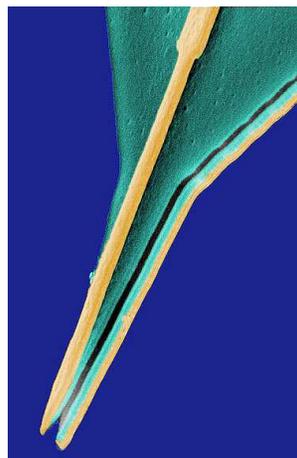
- Can decorate surface with tethered nanoparticles, in this case Au colloid.
- Insulating layer = self-assembled monolayer of thiol-terminated alkane chains.
- Scanned probe microscope tip as drain electrode: Coulomb staircase.



images from Andres *et al.*, Science **272**, 1323 (1996).

## Nanoparticles on surfaces

Special tip can incorporate gate, too, for SET action.



images from Gurevich *et al.*, APL **76**, 384 (2000).

### Clear technological challenges:

- Reliable fabrication of sub-10 nm structures with little or no variation for room temperature Coulomb blockade physics.
- Tuning of “environmental characteristics” such as stray capacitance.
- Reliable (self-controlling?) tunnel junctions.
- Control of single electronic offset charges: individual charged defects can have effects identical to random offset voltages on gates!

### Incentives:

- Dense integration.
- Possible ultralow power operation (reversible?).
- Ultimate limits of switching technology.

### Technology possibilities

#### Voltage-based logic:

- Very similar to typical CMOS logic: high voltage = logic high; low voltage = logic low.
- Nonmonotonic drain current as function of gate voltage opens up designs not possible with regular MOSFET devices.

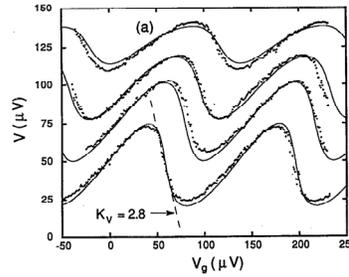
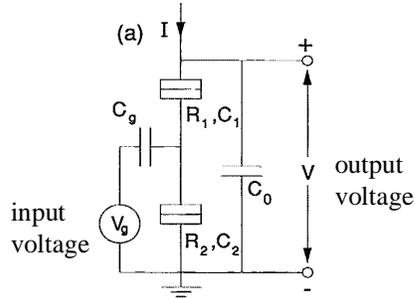
#### Charge-based logic:

- Since SETs can sense presence/absence of single electronic charges, use positions of charges to represent data / logic values.
- Some novel architectures possible, since charge positions can cause alter voltages capacitively, which can then move charges: *e.g.* Quantum Cellular Automata.

### Voltage-based logic:

It is possible, with SETs, to achieve *voltage gain*. That is, the output voltage modulation of a circuit can be greater than the input voltage modulation:

$$K_V \equiv \left| \frac{\partial V_{out}}{\partial V_G} \right|$$

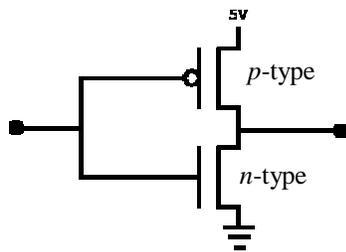


images from Zimmerli *et al.*, APL 61, 2816 (1992).

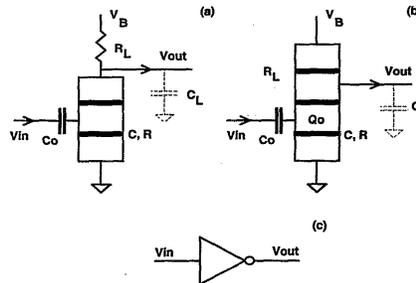
### Voltage-based logic:

Circuit designers can treat SET-based logic gates like conventional logic gates (keeping current designs) and leave the details up to the hardware folks.

Good point: SET characteristics (oscillatory response to  $V_G$ ) mean that **one SET can sometimes replace more than one regular MOSFET**.



CMOS inverter: 2 transistors of opposite types



SET inverter: 1 SET + resistive load.

## Voltage-based logic:

### Problems:

- Analysis shows that, for acceptable device performance, either temperatures must be very low, or devices must be extremely small....

$$k_B T \sim 0.01 \frac{e^2}{2C}$$

This can be mitigated slightly (~factor of 3) by using arrays of tunnel junctions, but at cost of lower packing density and more challenging fabrication.

- “Off”-state leakage leads to power consumption problems comparable to highly-scaled CMOS.

## Charge-based logic:

- Try to use positions of individual charges to represent “1”s and “0”s.
- Have switching action depend on charge state of device (necessary for logic).

Potential advantage: does not require substantial current flow for operation. Power consumption could therefore be advantageous.

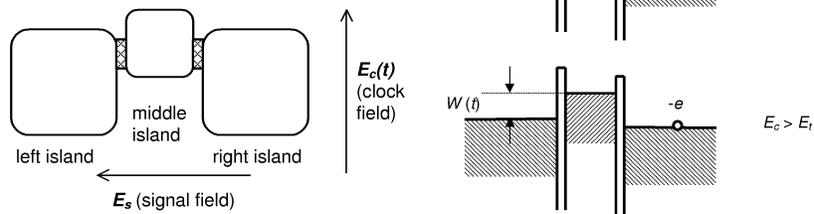
Tricky problem: single charge errors now become very important.

### Charge-based logic:

One approach analyzed in detail = SET “parametron”.

Has series of islands with “middle” islands asymmetrically coupled.

Clock signal pushes electrons along chain.



### Summary of problems:

- Temperature range of operation places great restrictions on device sizes.
  - Such small devices are likely to suffer tremendous variability.
  - Further, (especially in semiconductor devices) quantum level spacing effects (which superpose on the charging energies and alter the heights of the blockade conductance peaks) are likely to be significant.
- Background charges are also a serious problem.

Some chance that this may be self-correcting at sufficiently tiny scales, but not at all clear.
- Characteristic resistances ( $\sim 10 \text{ k}\Omega$ ) mean that for realistic capacitances these devices are unlikely to operate at high speeds.

### Prognosis:

Single electron devices are unlikely to be the technology that replaces CMOS at the few nm scale, unless there is a major breakthrough in fabrication, performance, or architectures.

SEDs more likely to find applications in niche areas:

- Nonvolatile memory
- Electrometry
- Metrology standards

### Next time:

Applications of single electron devices

Capacitance standard

Electrometers - the scanning SET

Thermometry

Intro to the rf-SET