

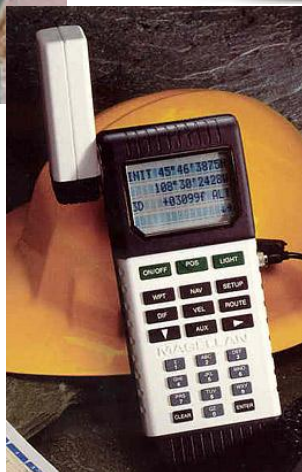


A Low Power Asynchronous GPS Baseband Processor

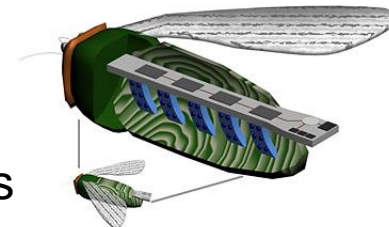
Benjamin Z. Tang, Stephen Longfield, Jr.,
Sunil A. Bhave, Rajit Manohar
Cornell University



Motivation



Augmented reality



Micro robotics navigation



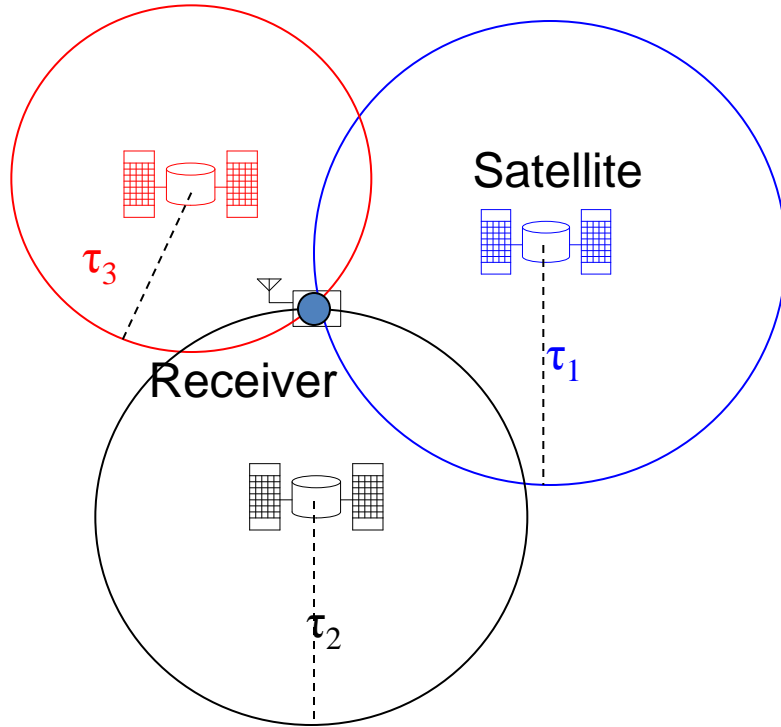
Location-based services



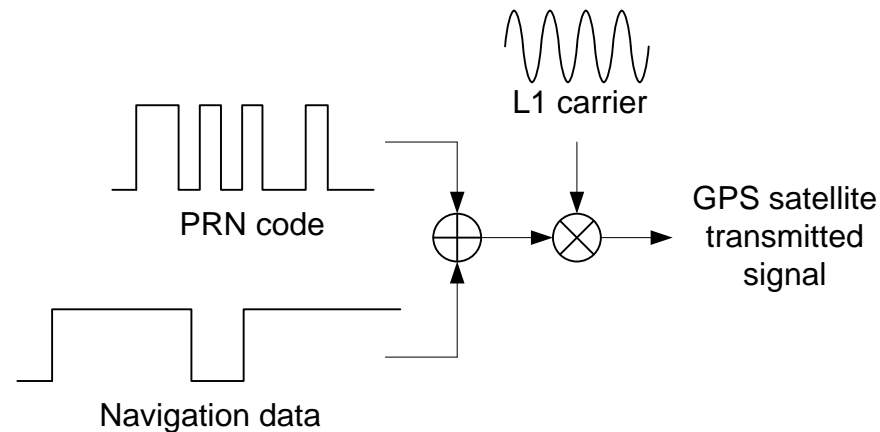
Decreasing power, but still too high

Need continuous operation, much lower power

How Does GPS Work?



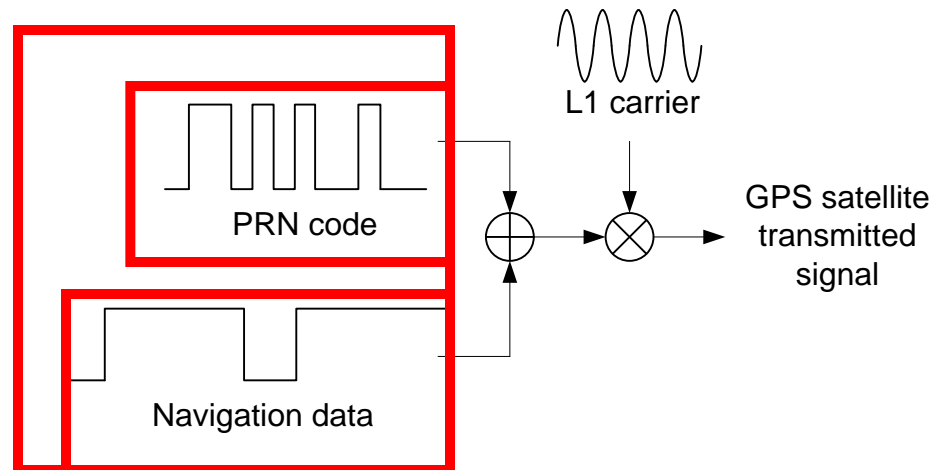
- GPS L1 civil signal
 - L1 carrier
 - 1ms repeat period, 1.023MHz
 - Unique for each satellite
 - Pseudorandom noise code (PRN)
 - 1ms repeat period, 1.023MHz
 - Unique for each satellite
 - Navigation data



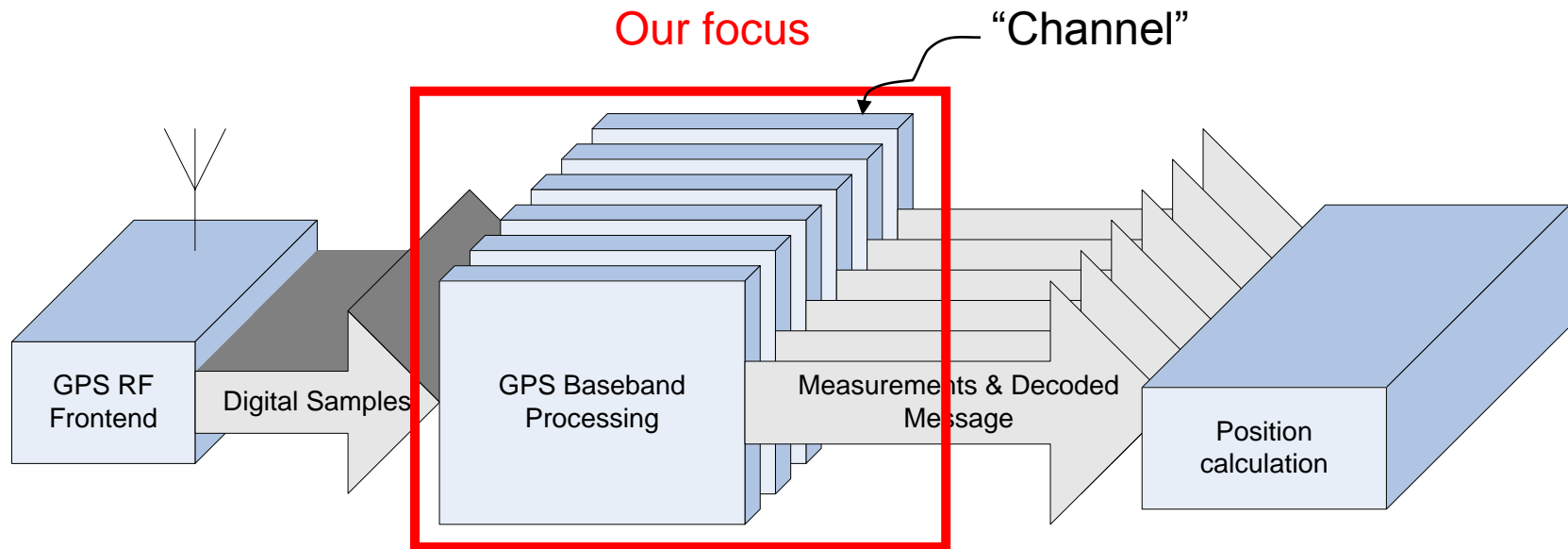


How Does Receiver Know...

- Which satellite's signal was received?
 - Use CDMA
- Where the satellite is?
 - Orbital information in navigation data
- When was the signal transmitted?
 - Navigation data + PRN code phase



GPS Receiver



Medium
power
<10mW

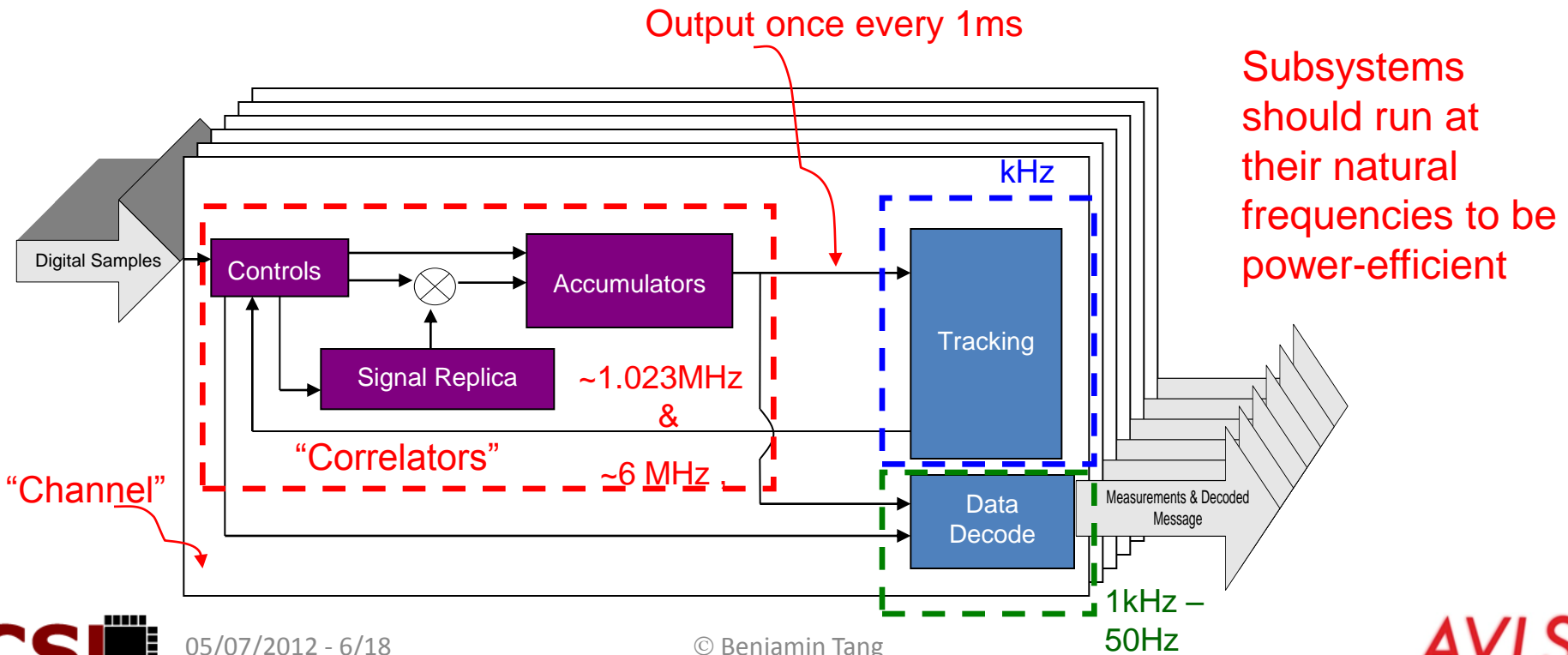
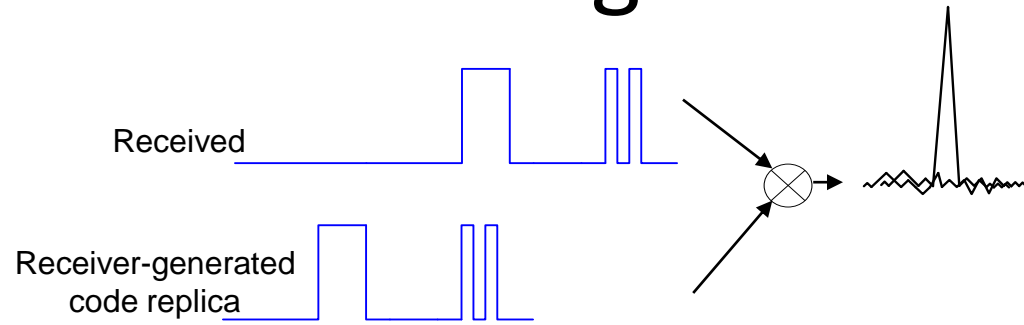
More power-hungry
~20-100mW

Negligible
power



GPS Baseband Processing

- Correlation in CDMA
 - Generate signal replica
 - Multiply and accumulate





Baseband Processor Design Options

Options	Correlators	Tracking	Decode
Option 1	Software	Software	Software
Option 2	Hardware	Software	Software
Option 3	Hardware	Hardware	Hardware

Our implementation

Typical synchronous design issue: What clocks to use?

- Shared with front end oscillator crystal
 - Optimized for one particular front end
 - Clock ratios, unnecessary power
- Independent oscillator crystals
 - Optimizations less front end dependent
 - Clock ratios
 - Processor clock \gg sampling clock, unnecessary power

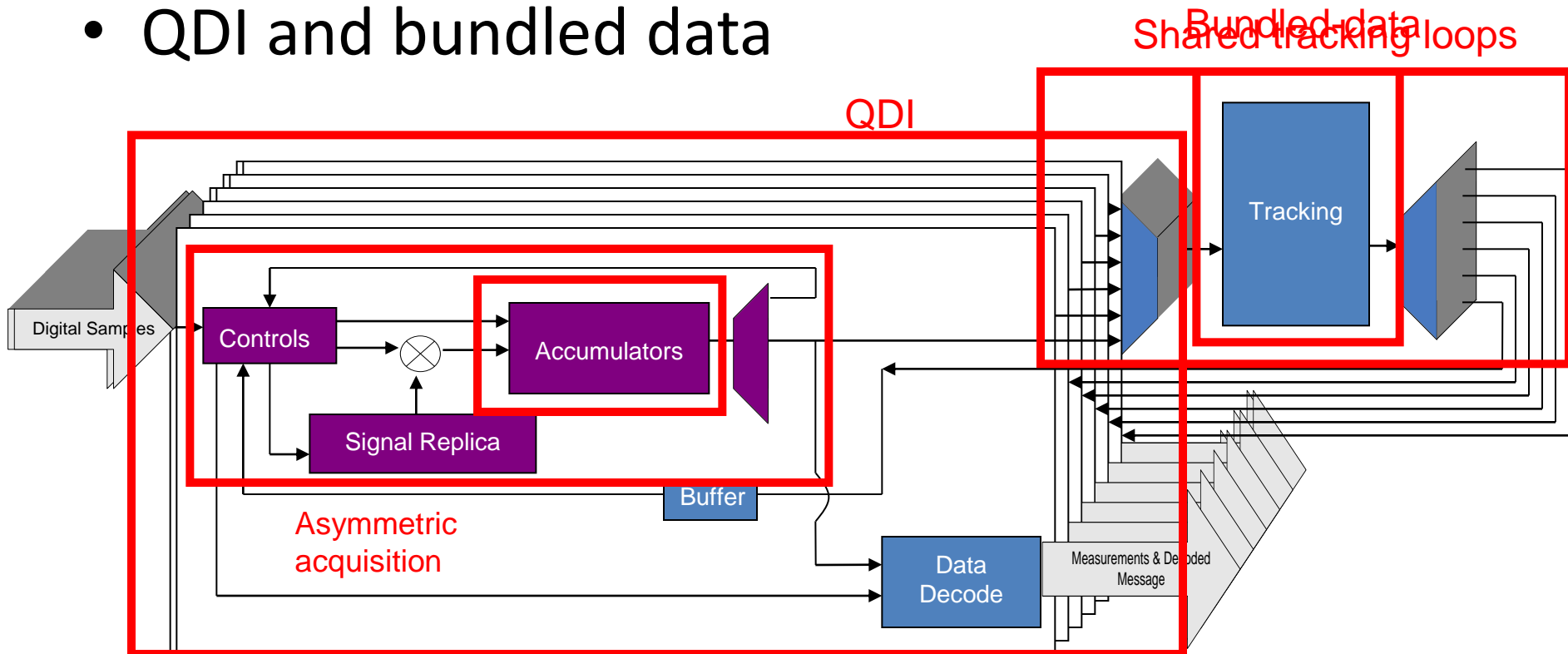
Asynchronous:

Each subsystem
only runs as fast
as it needs to



Asynchronous GPS Baseband Processor

- 6 channels
- Selected optimizations
- QDI and bundled data

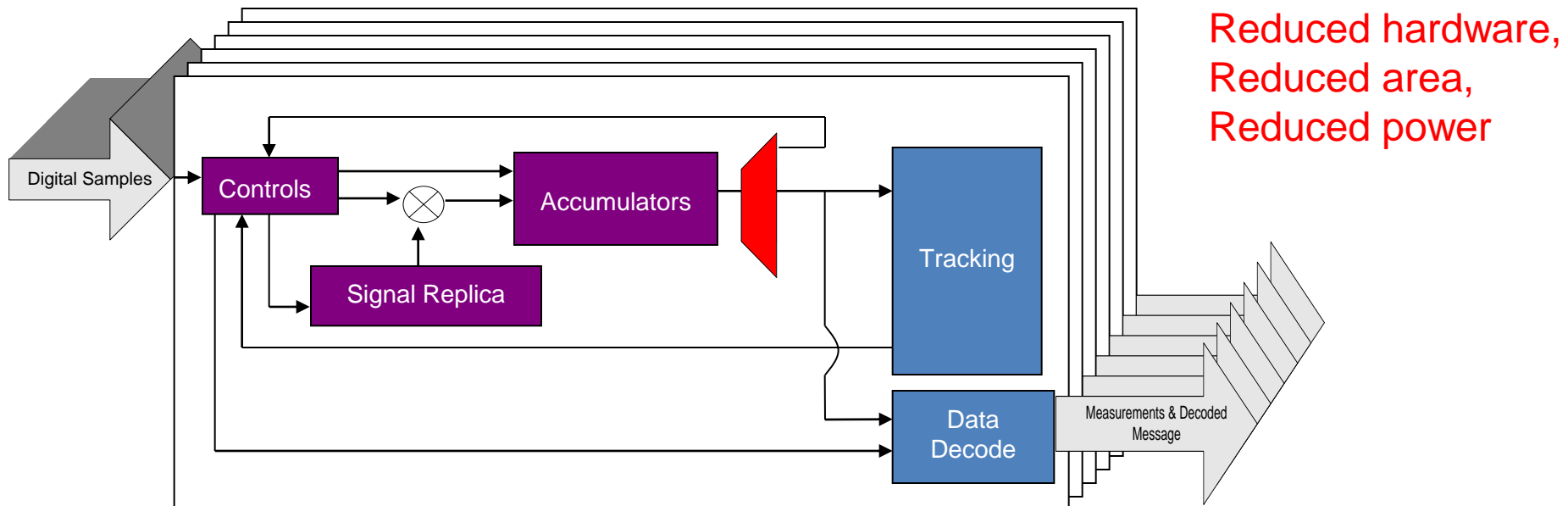




Asymmetric Acquisition

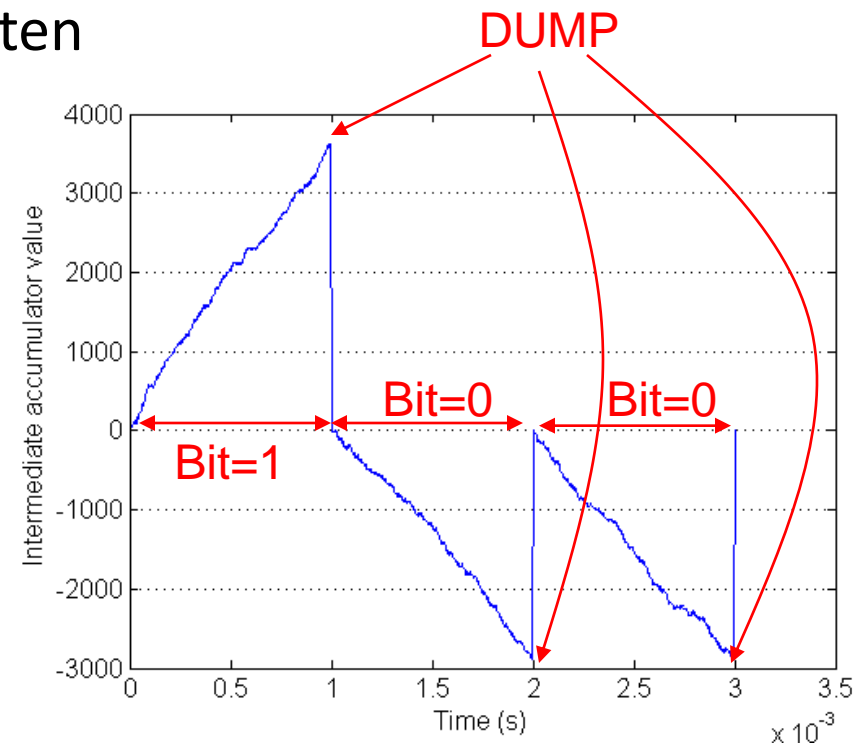
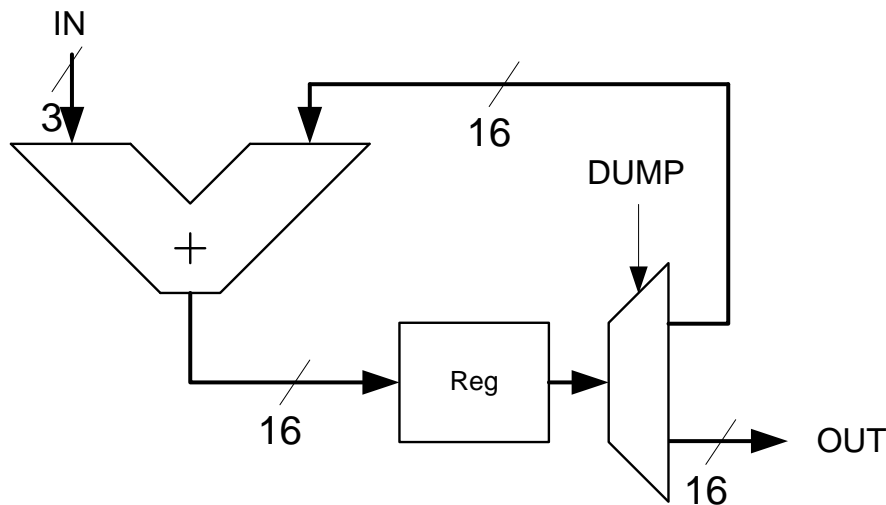
Full Acquisition (Other receivers)	Asymmetric Acquisition (Our receiver)
(+) Acquires: satellite ID, code phase offset and Doppler frequency	(-) Acquires: code phase offset, the rest from software
(-) FFT engine and memory or thousands of correlators	(+) Use pre-existing correlators

Full acquisition not needed often. Use asymmetric acquisition scheme.



Accumulators

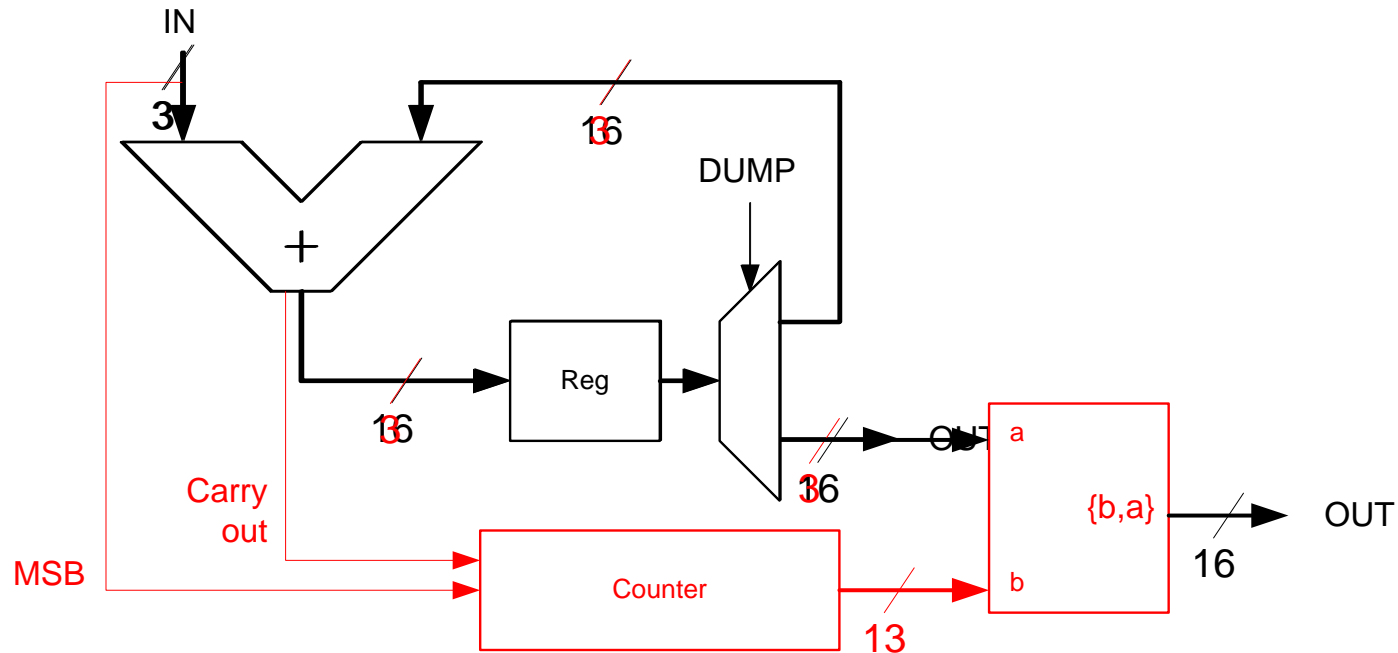
- Operate at input frequency
- 6 accumulators per channel
- 3-bit inputs iteratively added to 16-bit sum
- Only dump output once every 1ms
- Higher order bits do not switch often





Accumulators

- Standard 3-bit accumulator coupled with a 13-bit constant time counter
- Concatenate results at DUMP

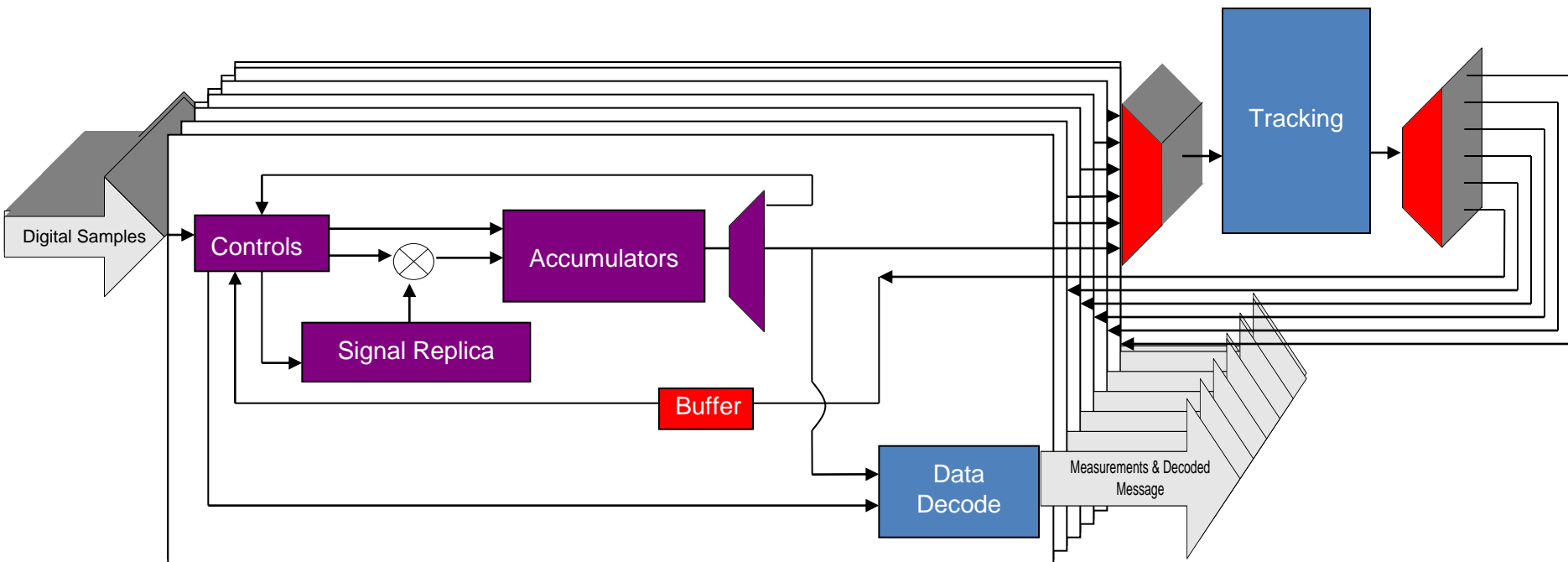


- Naïve 16-bit accumulator: $\sim 40\mu\text{W}$
Counter-based accumulator: $\sim 10\mu\text{W}$

**4X
less
power**

Tracking Loops

- ~~Digital updates~~ feedback loops
 - ~~Slow tracking loops, shared between the next data samples~~ power
 - Fast tracking loops, power hungry





Tracking Loops

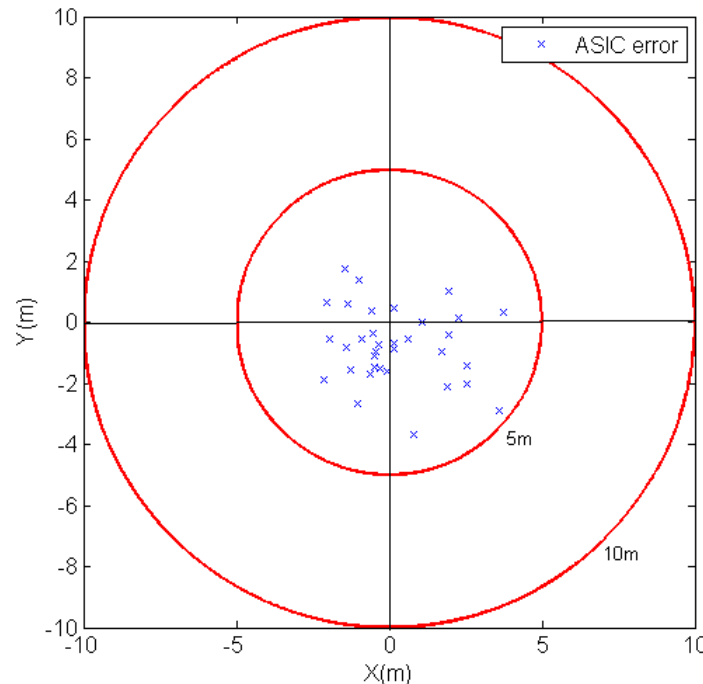
- Frequency Locked Loop (FLL), Phase Locked Loop (PLL) and Delay Locked Loop (DLL)
- Computations involve vector magnitude, arctangent, multiplication and division operations. Simplify:
 - Fixed point arithmetic, bundled-data
 - Apply Taylor series small angle approximation: $\tan^{-1}(\theta) \approx \theta$
 - Apply modified version of Robertson approximation:

$$A = \sqrt{I^2 + Q^2} \approx \max\left(|I| + \frac{1}{4}|Q|, |Q| + \frac{1}{4}|I|\right)$$

Position error increases by ~1m
on average

Receiver Performance Simulations

- Transistor-level implementation of our system
- Position accuracy simulation
 - 60 seconds of signal from commercial GPS signal simulator
 - No added atmospheric, ionospheric and multipath errors



3D-RMS error <4m



Power Simulations

SPICE simulation: V_{dd}=1V, T=25°C, 90nm technology

Subsystems		Acquisition (μ W) (6 Channels)	Track (μ W) (6 Channels)
Correlators	Code Generator	41.8	39.9
	Carrier NCO	477.4	442.8
	Code NCO	439.4	400.2
	Accumulators	367.3	359.9
Tracking Loops		5.5	5.8
Data Decode		1.9	2.1
Controls, Support		240.3	239.1
Total		1.49mW	1.41mW

1.4mW during
continuous tracking



Comparison

- Other contemporary GPS receivers (SOCs with integrated RF front end and baseband processing)

Name	This work	MediaTek	ST
Process	90nm	0.11 μm	0.18 μm
Voltage (V)	1.0	1.2	1.6
Number of Channels	6	22	12
System Power (mW)	1.4	34.0	56.0
RF Power (mW)	-	19.5	20.0
Baseband Power (mW)	1.4	14.5	36.0
Baseband Power/Channel (mW)	0.2	0.7	3.0
3-D rms Error (m)	3.9	-	3.0

**10X lower
power
3X lower
power per
channel
Comparable
accuracy**

- MediaTek (J.-M. Wei, et al., ISSCC 2009)
- STMicroelectronics (G. Gramegna, et al., JSSC 2006)



Conclusion

- Transistor-level implementation of a low power asynchronous GPS baseband processor
 - Only runs as fast as it needs to
- Selected optimizations:
 - Asymmetric acquisition
 - Counter-based accumulators
 - Shared bundled-data tracking loops

1.4mW

3D-RMS < 4ms



Acknowledgement

- Dr. Paul Kintner
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