Grasping Particle-Beam Isolation Technology, and Winning in Coming SOC Era

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Background

The advent of ultra deep sub-micron silicon technology (of gate length 0.13 μm and below) has triggered a strong motive to integrate multiple existing functions onto a single chip, called system-on-a-chip or SOC. This is desirable from the consumers' perspective, as it will, eventually, reduce the overall system cost, size, and power consumption dramatically while enhancing product performance and functionality. However, this worldwide trend provoked mixed feelings among production firms. On the bright side, it gives enormous hopes for a variety of potentially large markets; on the dark side, SOC-related problems are much more involved and deceiving than at first glance. Aside from complicated verification issues related to IP (intellectual property) re-use integration in general, it is technically very challenging to place extremely noise-sensitive RF or analog blocks side by side with relatively noisy digital (or even analog) blocks on the same silicon (or SiGe) substrate.

This is because, unlike GaAs, there is lack of high resistivity substrates for Si or SiGe. Traditional guard-rings have very limited effectiveness in suppressing the underlying noise cross-talk due to the fact that they are only very shallow structures on the wafer surface. The popular scheme of deep N-well (i.e., pnp junction) isolation also loses its effectiveness at high frequency, when it comes to 0.13 micron and below processes. The expensive option based on SOI (silicon-on-insulator) wafers, though assuring full DC isolation, fails to maintain its advantage and in fact is paralleled by mere guard-rings in the high frequency AC regime [1]. In short, finite conductivity of Si and SiGe substrates essentially allows all built-on-top devices couple to one another within the SOC in an unpredictably dynamic fashion.

In an attempt to resolve this problem, several proposals have lately been promoted; including Motorala's GaAs film growth on Si, and the system-in-package (SiP) approach (see, e.g., [2] for a good introductory article of the latter). The former allows separated high performance GaAs function blocks to be built upon a Si substrate and integrated with Si circuitry upon it. However, it inevitably presents a formidable change in process and concern over contamination and cost issues for chipmakers. The SiP approach, though of much economic potential for many applications, is considered less favorable for complicated mixed-modes, and high frequency and RF SOCs for which impedance matching is always a critical factor.

Like such, undesirable substrate cross-talk is the main difficulty encountered when Bluetooth and Wireless LAN ASIC (application-specific IC) SOCs are attempted, for example. In a successful commercial scale operation, however, the secure of an acceptable product yield is definitely required. This is why the process of an ASIC SOC (esp. RF-related) development has always evolved into a continual, laborious and costly vicious cycle, in which trial-and-error iterations are constantly driven by each component of the self-entangled development process. In the long run, a final compromise would result with acceptable yield, but likely at the cost of sacrificing some of the original goals and thus the optimum performance in mind. More importantly, great setback can be incurred upon each ASIC product during the development period, as a result of missing the time to market. Particularly, products of nowadays normally have very short lives.

Proposed back-end solution: particle beam stand (PBS)

The Institute of Nuclear Energy Research (INER) and the Advanced Research & Business Laboratory (ARBL), both Taiwan-based, have been the main promoters of the particle beam stand (PBS) concept. Their prototype technology (invented by Dr. Chungpin Liao, founder of ARBL, then working for ERSO of ITRI at Taiwan) used energetic proton beam from a very compact (1.5 m diameter, < 2 m height) cyclotron of INER. In that primitive method, a 15-20 MeV proton beam is applied at selected locations on an IC wafer or chip, after the VLSI process while before packaging. It has been experimentally demonstrated that the cross-talk between circuit blocks over a > 1 Ω-cm silicon wafer can be reduced about 1,000 times by applying in-between a penetrating, through-wafer, proton beam of practical fluence [3][4]. In addition, the usual low-Q value of a typical spiral IC inductor on Si was demonstrated to increase more than 100 % without damaging the inductor metal line and adjacent circuits [3][4]. This implies that the long wanted Si MMIC (monolithic microwave IC) is now

realizable. The proton created Si phase is characterized by very high resistivity (about 10^5-10^6 Ω-cm) and can sustain to a temperature of about 400 °C.

The new version of the INER/ARBL isolation scheme is far more superior and economic than the above old prototype. It utilizes novel radiation-enhanced neutral particle beam injection technology to render accelerator energy saving and amplified local defect creation within the semiconductor substrates [5]. With proper chip-level and wafer-level masking, the achieved isolation line width is at least below 50 μm, enough for the mixed-mode isolation. Concerns over possible device damage near the injection beam of PBS will not materialize if using particular measures. Further, since this new technology does not harm metal lines running across the isolation zone, the traditional desire for preservation of Si real estate is easily secured.

Impacts likely brought by the PBS revolution

By employing this post-VLSI PBS treatment, the aforementioned vicious cycle associated with general mixed-mode SOC products development can be eliminated entirely. Things of the good old days can be brought back to life, in which pure RF, pure analog, and pure digital development teams can work individually and thus focus on their best areas, respectively, without needing to worry about the collective influence from one another. Only then, IP-reuse can be confidently realized and optimum design (e.g., wide band) actually implemented. More importantly, the crucial time-to-market can then be controlled precisely.

It is envisioned that, whichever IDM (integrated device manufacturer) or fabless and its vertical conglomerate that know to take advantage of this PBS technology will likely push this new edge to the front-end SOC design rules and fundamentally change the semiconductor ecosystem. It is believed that the day PBS reaches general SOC design rules, the world's favorable semiconductor value chain will become much like what is depicted in Fig. 1.

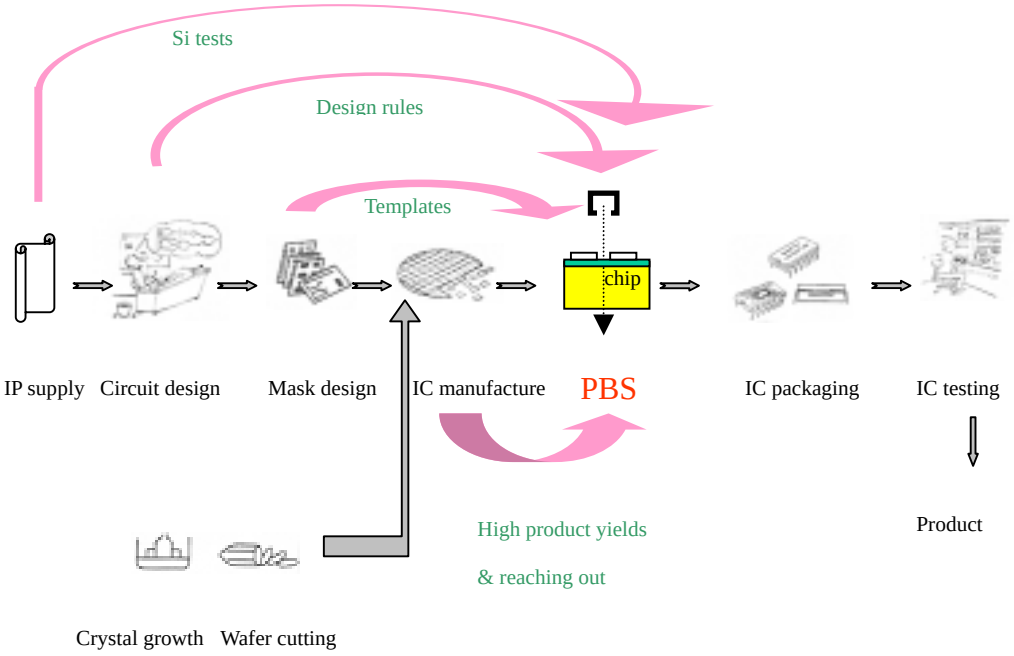

Fig. 1. New value chain for the global semiconductor industry

In the figure, it is seen that PBS would enhance the application domain for IP providers whose sale of commodity requires Si-tests to convince the customers. With the PBS design rules installed, design houses can swiftly come up with optimum SOC products at the first run. Mask manufacturers will have new business in supplying wafer or chip level high aspect ratio LIGA templates (layout masks) for the PBS system. IC fabs equipped with PBS capability can further reach out to its upper stream customers and build very special advantage for themselves. While, not shown in the above, equipment suppliers can enjoy the new business opportunity by providing PBS-related automation facilities.

On the other hand, once PBS-related defect generation model and microelectronic effects are incorporated into those widely used EDA (electronic design automation) tools, such as the MEDICI (device-level) and SPICE (circuit-level) software, many big-budget mixed-mode simulation tools may find themselves no longer favorable or even needed. The new PBS-enabled VLSI manufacturing platform

will easily jump across the traditional SOC integration barrier and succeed in bringing forward a bright era in which economic and versatile electronic systems are constantly made to serve all mankind.

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[5] Patents pending for INER and ARBL.