A Fast-Response Charge-Pump Gate Driver Applied to Linear Regulation

André L. R. Mansano[1], Jader A. De Lima[2] and Jacobus W. Swart[1]

[1]Electrical Engineering Dept, UNICAMP, Campinas, Brazil
[2]Center for Technology of Information (CTI), IC Design House, Campinas, Brazil.
e-mail: amansano1@gmail.com

ABSTRACT

This paper presents a compact charge-pump gate driver (CPGD) that dynamically adjusts the driving voltage V_{GS_SW} of power switches, following stringent load transients in amplitude and duration. Owing to its simple topology, the CPGD responsively sustains regulation of the charge-pump (CP) output voltage V_{OUT} within the range [2.4V, 3.0V] during transient load, while consuming only tens of µA. Contrary to driving techniques that depend on the settling of V_{OUT} before adjusting V_{GS_SW}, the CPGD instantaneously compares V_{OUT} to a reference V_{REF} and optimally sets V_{GS_SW}. The circuit shows low sensitivity with switching frequency f_{sw} across a broad range [50KHz f_{sw} 1MHz]. Simulations with PSPICE and Bsim3v3 models attest the CPGD performance at extreme scenarios of a light and heavy load current I_{LOAD}. For a 20µs-step of I_{LOAD} from 0 to 20mA, the CPGD takes only 20µs to raise V_{GS_SW} from 1.0V to 4.75V. The entire CP regulator was prototyped on a standard 0.35µm CMOS fabrication process, with the CPGD occupying an area of 0.014µm^2. Experimental results match closely both DC and transient the expectations for CPGD. The driver features consumption below 475µW and complies with a low-voltage supply, such as1.5V-batteries.

Index Terms: Gate driver, Charge-pump, Switched-capacitor converters.

1. INTRODUCTION

It´s common practice in designing switched-capacitor converters (SCC´s) to keep charge-pump (CP) switches continuously commuting at light loads [1-2]. However, the resulting simplification in the control circuitry is frequently objected, as the switching dissipation prevails over the average power delivered to the load. Since the converter efficiency is degraded, such an approach does not comply with rigorous power consumption requirements for modern battery-operated applications. While saving switching dissipation, skip-mode regulation [3] is a simple way to produce a well-controlled voltage VOUT at the converter output. In this technique, a finite wait time Δt_W is inserted between non-overlapping pulses of width Δt. During time intervals Δt, the energy is sequentially transferred from the power line to the flying capacitor, and from the later to the load. However, as compared to a linear-mode regulation, where $\Delta t_W = 0$, VOUT is subject to a higher voltage peaking that is increased by a factor $(1+ \Delta t_W/\Delta t)$. Unless special care is observed, this overvoltage may stress the gate-oxide of transistors being supplied by such a rail voltage, having their life expectance abbreviated.

On the other hand, linear regulation has been the preferred option to improve CP efficiency. The gate-source voltage V_{GS_SW} applied to power switches is regulated by linear feedback control of V_{OUT} [4-6,8]. An interesting variation, named *linskip* regulation, is proposed in [5,8] and combines both skip and linear modes. In this case, two current sources are alternately commuted by a comparator that arbitrates between the ripple on CP output voltage and a reference. An average voltage V_{AVG}, proportional to the commuting time of these current sources, is obtained through an averaging capacitor and used as V_{GS_SW} to drive the switches gate. Nonetheless, owing to its dependence on the settling time of V_{AVG}, this approach does not immediately respond to load transients.

To overcome such a limitation, this work introduces a compact charge-pump gate driver (CPGD) that instantaneously compares the SCC output voltage V_{OUT} with an internal reference V_{REF} and optimally sets V_{GS_SW}. The circuit simple topology leads to a fast reaction to transients. The CPGD circuit is embedded in a complete SCC system that performs a linear regulation on V_{OUT}.

The paper is organized as follows. Section II describes the SCC linear regulation mode, CPGD, auxiliary charge-pump ($CP_{\_AUX}$) and the main charge-pump (CP). Circuit design and simulation data are described in Section III. Experimental results, analysis are presented in Section IV and concluding remarks are summarized in Section V.

2. CIRCUIT DESCRIPTION

Figure 1 depicts the SCC block diagram, which comprises main and auxiliary charge-pump stages, respectively CP and $CP_{\_AUX}$, CPGD, D_{RB} driver and a feedback network R_1 - R_2 that provides V_{OUT}^*, a sampled value of V_{OUT}. Off-chip filter and flying capacitors C_{OUT} and C_{FLY}, respectively, complete the converter. The SCC load is represented by current source I_{LOAD}. Both charge-pump circuits are supplied by input line PV_{IN}, whereas CPGD is powered by the bootstrapped voltage V_{BOOT}, generated by $CP_{\_AUX}$. A decoupling capacitor can optionally be connected from the CPGD output to ground to avoid hazardous voltage spikes on V_{GS_SW} voltage.

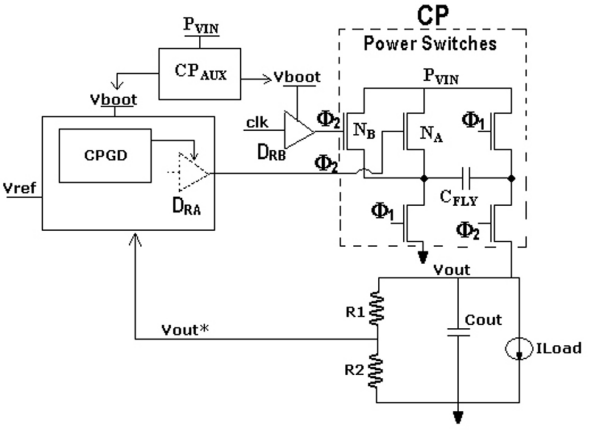


Figure 1. Charge-pump applied to linear regulation.

$CP_{\_AUX}$ is required to ensure that NMOS power switches are properly turned on in triode region, which is accomplished by maximizing the value of V_{GS_SW} in CPGD. The $CP_{\_AUX}$ block comprises a 4-stage Charge-Transfer Switch (CTS) charge-pump. Alternately, V_{OUT} could be used as the supply voltage to CPGD, at expense of a lower V_{GS_SW}, however. $CP_{\_AUX}$ would thus become unnecessary, as long as the on-resistance of the switches is kept sufficiently low.

Power switches in the main charge-pump block are arranged as two composite arrays N_A and N_B of paralleled unity transistors, respectively driven by D_{RA} and D_{RB}. The driver D_{RA} is internal to CPGD and powered by an adaptive rail voltage V_{GS_SW}, which takes into account variations in V_{OUT}^* due to loading. Switches in the CP output stage are sized for relatively high-current rates and usually made up of a large array of unity transistors. Whereas the bulky portion N_A of the array is conditionally turned on/off by the CPGD, as imposed by steady and dynamic characteristics of I_{LOAD}, the remaining part N_B is always commuted, ensuring adequate start-up and V_{OUT} settling. Upon light loads, only a fraction of the total switches contributes to power consumption, therefore.

Due to the finite on-resistance (R_{DS_ON}), ohmic losses develop across the switches, lowering V_{OUT} from its regulated value with increase of I_{LOAD}. This effect is nonetheless counteracted in the CPGD by increasing V_{GS_SW}, keeping V_{OUT} within the specified tolerance.

A. Charge-Pump (CP) and Gate Driver (CPGD)

The main charge-pump works with two non-overlapping phases Φ_1 and Φ_2, as shown in Figure 2**.** During Φ_1, C_{FLY} is connected in parallel to PV_{IN}, whereas in Φ_2, C_{FLY} is connected in series to PV_{IN}, so that C_{OUT} is charged with $2PV_{IN}$.

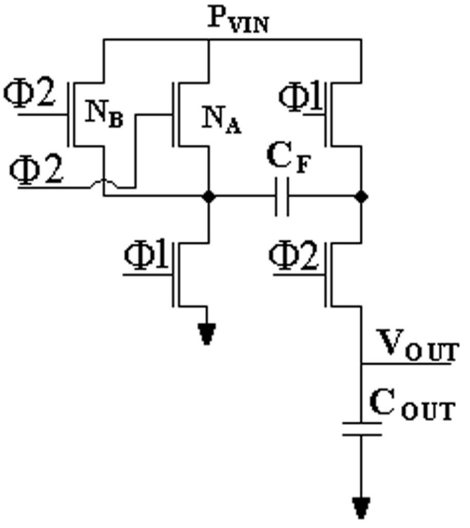


Figure 2. Main Charge Pump schematic**.**

The voltage at the converter output is given by [3,7].

$$V_{OUT} = 2PV_{IN} - I_{LOAD}\left(2\sum_{i=1}^{n} R_{DS\_ON} + \frac{1}{2 f_{SW} C_{OUT}}\right) \quad (1)$$

where f_{SW} is the switching frequency and R_{DS_ON} is the switch on-resistance, for *n* switches in series. Charge-pump losses are twofold: i) the ohmic drop, which appears multiplied by a factor of 2, as switches deliver I_{LOAD} to the load, as well as recharge C_{OUT}, with a charge equivalent to I_{LOAD}, during Φ_1 off-time and ii) the voltage drop across the CP output impedance $1/[f_{sw}C_{OUT}]$. Therefore, the CPGD partially counteracts the increase of I_{LOAD} by decreasing R_{DS_ON} to maintain V_{OUT} inside its tolerance interval. Since the switch transistors operate on low-V_{DS} triode region, one has

$$R_{DS\_ON} = \frac{1}{\left(\frac{W}{L}\right)_{SW} \mu_n C_{ox}\left(V_{GS\_SW} - V_{TH\_SW}\right)} \quad (2)$$

where $(W/L)_{SW}$ is the aspect-ratio of the compound switch. Therefore, V_{GS_SW} should accommodate variations on R_{DS_ON} to keep VOUT properly regulated. Such an adjustment is carried out by the CPDG, whose schematic is shown in Figure 3. According to its topology, V_{GS_SW} is made inversely proportional to V_{OUT}, and since its adjustment does not rely on large-capacitor averaging techniques [5-6,8], relatively fast transient responses can be attained. Combining (2) and (1), for n = 4 and rearranging to isolate V_{GS_SW} as function of V_{OUT}, it turns out

$$V_{GS\_SW} = V_{TH\_SW} + \frac{8I_{LOAD}}{\left(\frac{W}{L}\right)_{SW} \mu_n C_{ox}}\left(\frac{1}{2PV_{IN} - V_{OUT} - \frac{I_{LOAD}}{2\,f_{SW}C_{OUT}}}\right) \quad (3)$$

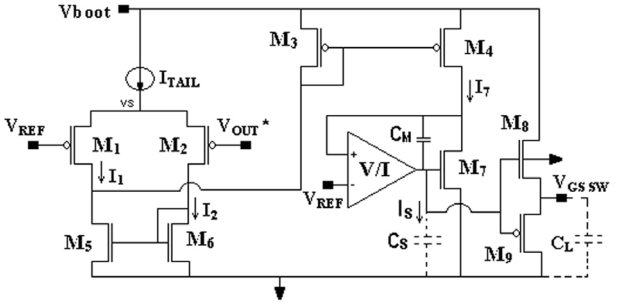


Figure 3. CPGD schematic.

The CPGD comprises a differential pair (M_1-M_2), current mirrors (M_3-M_4, M_5-M_6), a voltage-to-current converter (V/I) and output stage (M_8-M_9). Transistors M_1-M_2 instantaneously senses the unbalance condition $V_{OUT}^* > V_{REF}$, and the resulting difference $I_2 - I_1$ enters into the current subtractor M_3-M_4, being mirrored to M_7 and converted to V_{GS_SW} through M_8-M_9 push-pull transistors. The V/I converter is implemented as a single gain-stage OTA, with sufficient current capability to drive the push-pull input capacitance. Internal frequency compensation is guaranteed by Miller capacitor C_M. The CPGD is supplied by a rail V_{BOOT}, which is provided by the auxiliary charge-pump.

Let´s assume that V_{OUT}^* offsets V_{REF} by an amount large enough to drive the differential-pair away from its linear operation, so that large-signal equations should be employed. As soon as M_1 turns off, I_{TAIL} is fully diverted through M_2 and then to M_5, to be ultimately copied to M_7 by a ratio $(W/L)_4/(W/L)_3$. Denoting $\beta = (W/L)\mu C_{ox}$, one has

$$V_{GS\_SW} = V_{TH7} + |V_{TH9}| + \sqrt{\frac{2}{\left(\frac{W}{L}\right)_{SW} \mu_n C_{ox}} \frac{W_4}{W_3}\frac{L_3}{L_4} I_{TAIL}} \quad (4)$$

so that ground-referred V_{GS_SW} is ideally confined to interval $[V_{TH7} + |V_{TH9}|,\ V_{BOOT} - V_{TH8}]$. The upper limit could eventually reach V_{BOOT} if M_8 corresponded to a depletion-mode transistor. Such an option is found in some smart-power integration processes.

B. Auxiliary Charge-Pump (CP_AUX)

The schematic of $CP_{\_AUX}$ is shown in Figure 4. P_{VIN} is multiplied by 4 to generate the required value of V_{BOOT} to power CPGD. Transistors M_A - M_D and M_{BT} operate in triode region during turn-on phase, to avoid threshold voltage drops on V_{BOOT}. The transistors are turned on/off by their forward and backward stages, i.e. M_A is turned on by V_B voltage (forward stage) and it is turned off by P_{VIN} (backward stage). Diode-connected transistors are used to correctly start up the circuit and their effective areas are very small as compared to the switches ones.

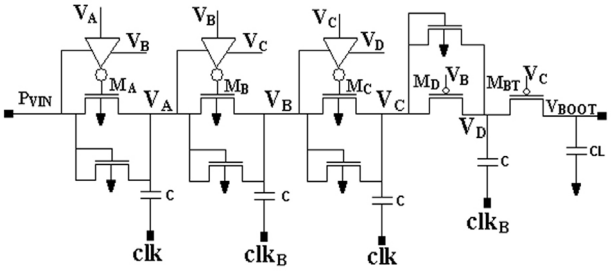


Figure 4. $CP_{\_AUX}$ schematic.

V_{BOOT} value is given by equation (5), where R_{SW} is the channel resistance of transistors M_A to M_{BT}, I_{LBOOT} is the DC current load associated with V_{BOOT} and $C = C_L$ is an external capacitor, added to each stage. V_{BOOT} is ideally $4PV_{IN}$, in case of no DC current sunk from the circuit. However, accounting for non-idealities and finite load current, and still achieve $V_{BOOT} \geq 3PV_{IN}$, as required for CP operation, the $CP_{\_AUX}$ has to multiply PV_{IN} by a factor of 4.

$$V_{BOOT} = 4PV_{IN} - I_{LBOOT}\left(5R_{SW} + \frac{4}{f_{SW}C}\right) \quad (5)$$

3. DESIGN AND SIMULATION RESULTS

The SCC was designed in accordance with a standard 0.35μm n-well CMOS fabrication process. Supply voltages are V_{DD}=5.0V, PV_{IN}=1.5V, V_{BOOT}=5V and V_{REF}=1.45V. Typically, process parameters are V_{THN} = 0.7V, V_{THP}=-0.9V, $\mu_n C_{ox}$=143μA/V², $\mu_p C_{ox}$=41μA/V², t_{ox}=7.7e-3μm and ?$_{ox}$=3.276e-17 F/μm. The charge-pump has to sustain V_{OUT} within 80% of nominal value ($2PV_{IN}$). Simulation data were obtained with PSPICE and Bsim3v3 models.

A. Gate Driver CPGD

Transistor sizing listed in Table I ensures that the clamping voltage of V_{OUT} is close to 2.3V. The specified slew-rate SR of CPGD is higher than 5V/µs and limited by the smallest value between I_S/C_S and I_7/C_M, where C_S is the input capacitance of output stage. For maximum I_S = 30µA and C_S=2.9pF, one has SR = 10.3V/µs. For a power switch with $(W/L)_{SW}$ = (8000µm/0.5µm) and C_{ox}=4.255fF/µm², it turns out a 17pF-load capacitance at CPGD output. The CPGD power consumption is lower to 475µW.

Figure 5 displays the CPGD transfer V_{OUT} x V_{GS_SW}, within the interval 2V ≤ V_{GS_SW} ≤ 3V. The characteristic can be split into three zones (A, B and C), all of them showing distinct behavior. In Section-A, the CPGD output approaches V_{BOOT} and clamping occurs at 2.35V. Section-B reflects equation (5), where M_7 still operates in saturation. Finally, the minimum V_{GS_SW}, imposed by V_{TH7} + |V_{TH9}|, is shown on Section-C. The CPGD dynamic response is displayed in Figure 6, for a pulsed PV_{IN} from 1.5V to 1.15V, following a 20µs-transient. The V_{GS_SW} voltage reacts as soon as V_{OUT} decreases, demanding 20µs to rise from 1V to 4.7V.

Load regulation is shown in Figure 7. It´s worthy noticing that during the charge-pump start-up, V_{OUT} remains below 2.35V, so that the CPGD operates at low head-room and V_{V/I^+} ≅V_{BOOT}. At 40µs, V_{OUT} goes above 2.35V, and the circuit functions normally, with V_{V/I^+} = V_{REF}. At 120µs, a 2µs-load step occurs, varying I_{LOAD} from 0 to 20mA, as depicted in Figure 7a, whereas a slower transition is presented in Figure 7b.

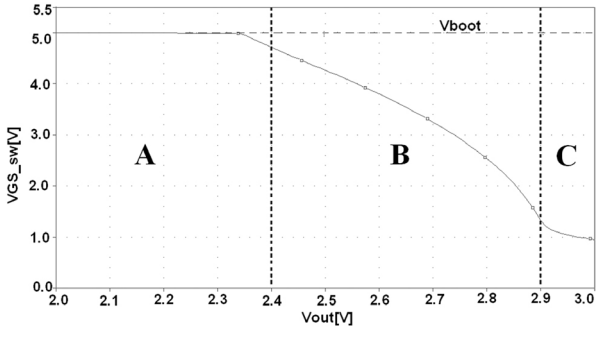


Figure 5. Simulated V_{GS_sw} x V_{OUT} characteristic.

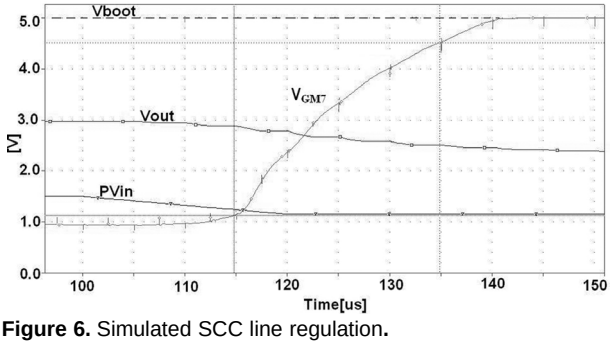
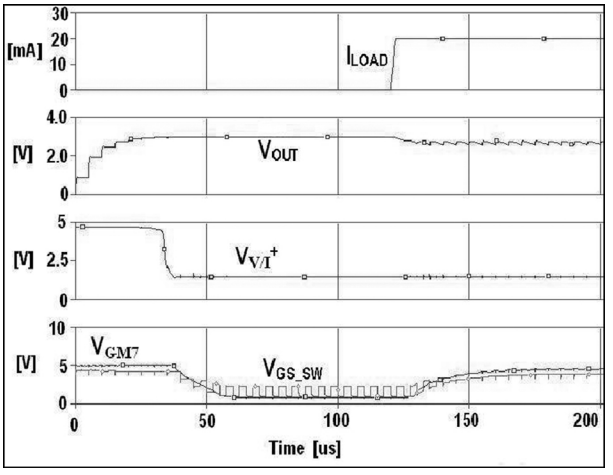
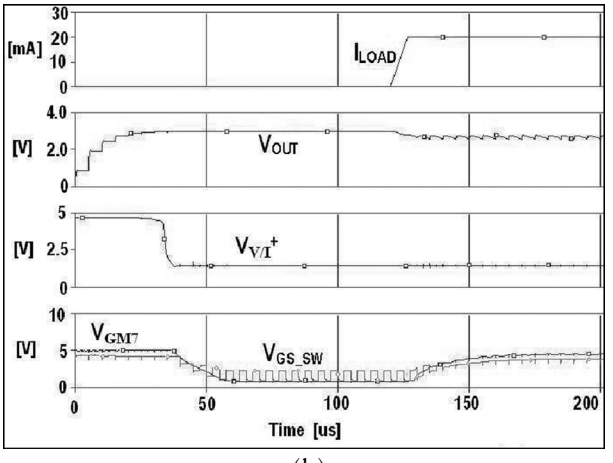


Figure 6. Simulated SCC line regulation.



(a)



(b)

Figure 7. Load regulation (a) 2µs-step current and (b) 20µs-step current.

Excellent response from the CPGD can be observed, as V_{GS_sw} grows from 1V to 5V in 20µs, counteracting the rise in switches on-resistance. In case of a more stringent load regulation, with V_{OUT} still kept above 80% of its nominal value, the aspect-ratio of CP switches could be made larger, impacting layout area, however. Increasing V_{BOOT} above 5V to further decrease R_{DS_on} would nevertheless stress the gate-oxide, as this voltage is the limit for the sort of transistor employed in the switches design. Therefore, a good trade-off has been achieved between V_{OUT} regulation tolerance and die size.

Table I. CPGD Transistor Sizing.

Transistor	W[um]	L[um]	Transistor	W[um]	L[um]
M1	2x10	5	M5	2x2.5	2
M2	2x10	5	M6	2x2.5	2
M3	1x5	3	M7	1x1	25
M4	2x5	3	M8	4x100	1.5
M9	2x80	0.5			

B. Auxiliary Charge-Pump (CP_AUX)

The designed $CP_{\_AUX}$ has a nominal voltage gain of 4, obtained through a time constant $R_{SW}C$, imposed smaller than $0.5/f_{SW}$ by

$$\frac{L}{W}\frac{1}{\mu_n C_{ox}(V_{GS}-V_{TH})} \le \frac{0.5}{f_{SW}C} \quad (6)$$

so that, the output resistance R_{BOOT} of $CP_{\_AUX}$ is

$$R_{BOOT} = \frac{4}{f_{SW}C} \quad (7)$$

For f_{SW} = 200kHz, I_{LBOOT} = 1mA and $\Delta V_{BOOT} \le 0.02$V, it tuns out C ≅1μF, whereas the aspect-ratio of transistors must be roughly 400. $CP_{\_AUX}$ transistor sizing is presented in Table II.

From $CP_{\_AUX}$ transient data for $CP_{\_AUX}$ illustrated in Figure 8, V_{BOOT} reaches 5.5V at no load current. Internal voltage levels at each $CP_{\_AUX}$ stage (A, B, C and D) are also indicated.

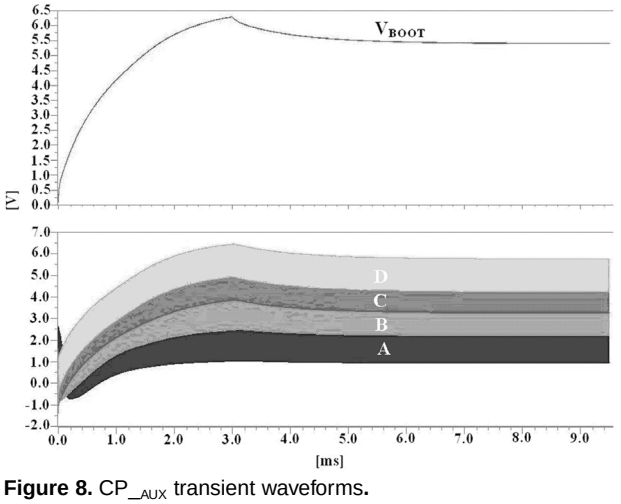


Figure 8. $CP_{\_AUX}$ transient waveforms.

Table II. $CP_{\_AUX}$ Transistor Sizing.

Transistor	W[μm]	L[μm]
NMOS_switch	400	0,5
NMOS_diode	50	0,5
PMOS_switch	900	1
NMOS_inverter	5	1
PMOS_inverter	5	1

C. Charge-Pump (CP)

The voltage ripple V_{RP} superimposed to CP output voltage V_{OUT} corresponds to

$$V_{RP} = \frac{I_{LOAD}}{2f_{SW}C_{OUT}} \quad (8)$$

Assuming V_{RP} = 5mV for I_{LOAD}=20mA and f_{SW} = 200kHz, C_{OUT} should be 10μF. Regarding eqn. (1), the $1/(2f_{SW}C_{OUT})$ term is then equivalent to 250mΩ. Therefore, to achieve V_{OUT} = 2.4V at 20mA-load and n=4, R_{DS_on} must attain 3.75Ω, which implies in switches with a calculated aspect-ratio of (6000μm/0.5μm), for V_{GS_SW} = 5V. Since sizing is based on first-order equations, the channel-width was re-adjusted to 8000μm, after simulation.

4. EXPERIMENTAL RESULTS

The photomicrography of the prototyped SCC is depicted in Figure 9. The CPGD occupies a small effective area of 0.014mm², while the SCC die size corresponds to 4.0mm², which includes pads. Figure 10 shows the experimental CPGD transfer function. Similarly to simulated results of Figure 5, it also exhibits three distinct sections. The clamping voltage is around 2.4V, only 50mV to [1.65V, 4.8V]. Figure 11 presents the CPGD transient response to a 20μs-load step of 20mA. As it can be seen, V_{OUT} abruptly falls from 3V to 2.4V, although still remaining within

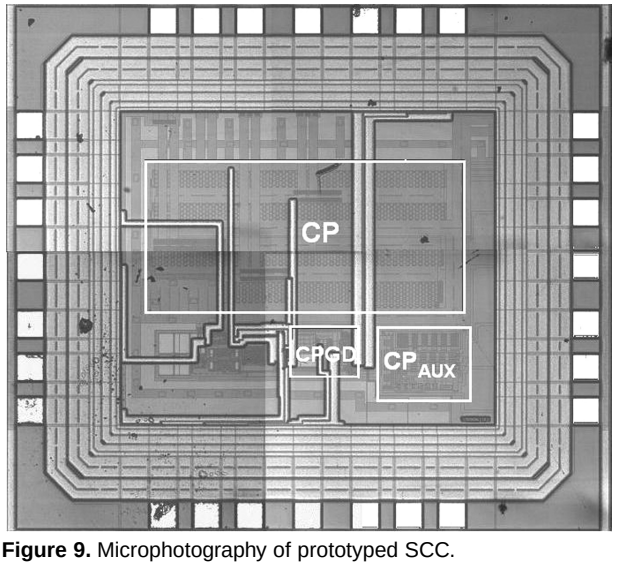


Figure 9. Microphotography of prototyped SCC.

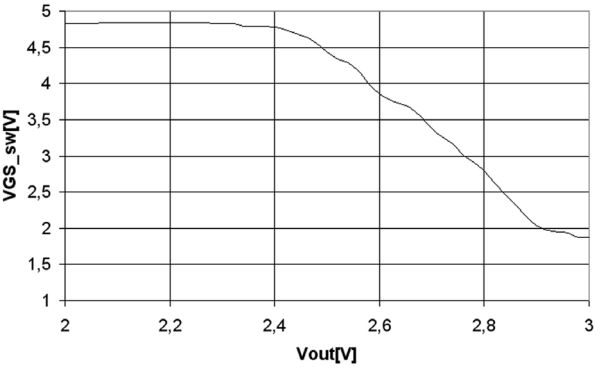


Figure 10. Measured CPGD transfer function.

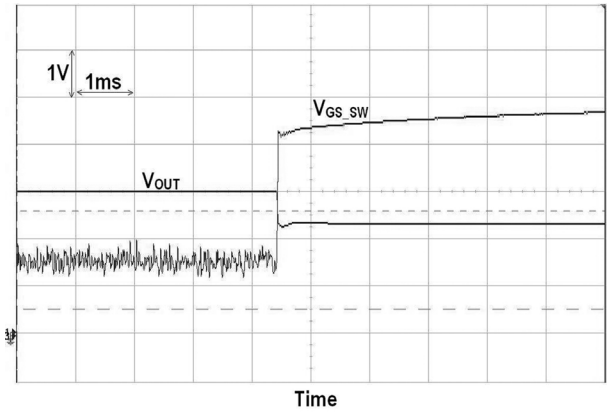


Figure 11. CPGD transient response.

Table III. Qualitative Comparison.

Deployed Circuit	Efficiency Light Load	Efficiency High Load	Transient Response
CPGD	Slightly lower than [5,6,8]	High	Fast
[1,2]	Low	High	NA
[5,6,8]	High	High	Slow

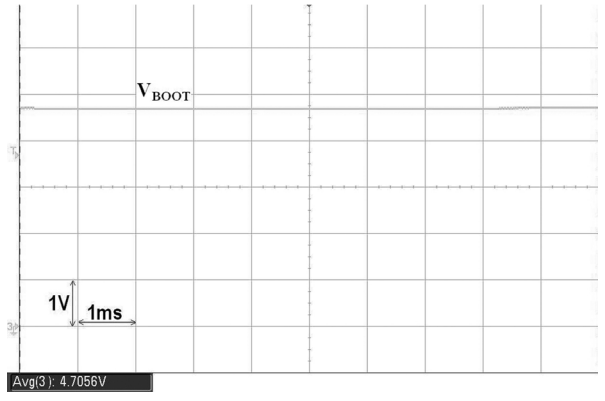


Figure 12. V_{BOOT} for I_{LBOOT} = 1mA**.**

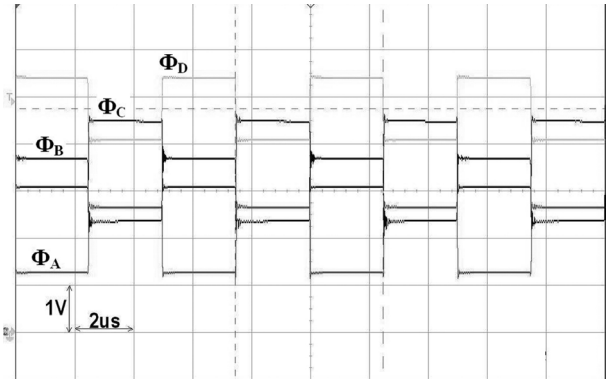


Figure 13. V_{BOOT} for I_{LBOOT} = 1mA**.**

80% of its nominal during the load transient. Reacting to V_{OUT} dropping, V_{GS_SW} goes up from 1.65V to 4.8V, after 20μs. Such a behavior is in good accordance with simulation data of Figure 7b and reenforces the advantage that the CPGD does not require the settlement of V_{OUT} to star the adjustment of V_{GS_SW}. Table III summarizes a qualitative comparison between the CPGD and prior art.

Figure 12 shows V_{BOOT}, for I_{LBOOT} = 1mA. Its value 4.7V, inside specified range 4.5V ≤ V_{BOOT} ≤ 5.5V. Figure 13 displays waveforms of CP_{AUX} internal phases.

The charge-pump output voltage is shown in Figure 14, with V_{OUT} achieving 3V, for PV_{IN} =1.5V. As expected, PV_{IN} is correctly doubled by CP. Load regulation is presented in Figure 15. With respect to simulation, V_{OUT} exhibits a value 12% smaller, for a 20mA-load current. Such a departure can be credited to process spread on R_{DS_ON}, PCB parasitic resistances and equivalent series resistance (ESR) of external capacitors.

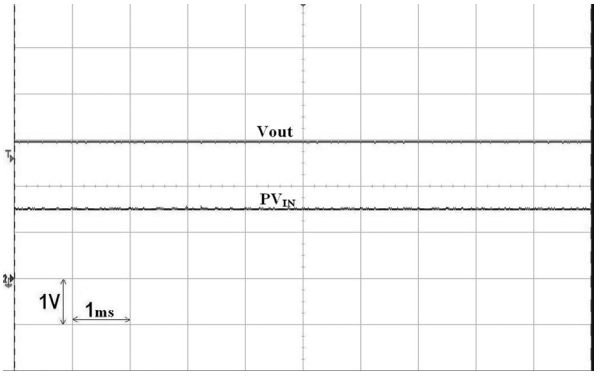


Figure 14. Experimental PV_{IN} and V_{OUT} **.**

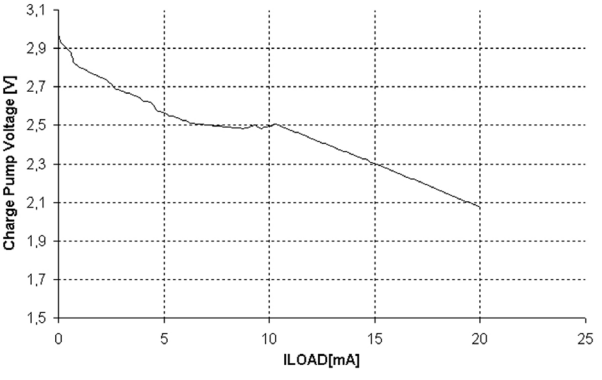


Figure 15. CP load regulation**.**

5. CONCLUSIONS

A charge-pump gate driver (CPGD) for linear regulation operation has been introduced. Its simple topology allows fast response to load transients, as perturbations on output voltage V_{OUT} are instantaneously sensed. To maintain switches on triode

region, the CPGD is supplied by V_{BOOT}, obtained from an auxiliary charge-pump $CP_{\_AUX}$.

As a building part of a switched-capacitor converter (SCC), the CPGD was prototyped in AMS H35 process, and occupies an area of only $0.014mm^2$. Close agreement between simulation and experimental data is remarked, which attests the good performance of the proposed driver.

Measurements indicate that the CPGD responds within 20μs to a 20mA-step load, sustaining V_{OUT} within 80% of $2PV_{IN}$. The CPGD consumption is limited to 475μW, whereas its output voltage V_{GS_SW} ranges from 1.65V to 4.8V. The voltage V_{BOOT} from $CP_{\_AUX}$ is kept between 4.5V and 5.5V, for 1mA-load current. The main charge-pump (CP) duplicates the input voltage (PV_{IN}), as expected. With respect to load regulation, V_{OUT} is nearly 10% below its simulated value, for 20mA-load current. Such a deviation can be attributed to process spread on switches resistance, PCB stray components and ESR of external capacitors.

Since there is no dependence on V_{OUT} settling time, as well as the need for an averaging capacitor, the CPGD is a valuable alternative to charge-pump circuits that demand a fast response to load transients, while keeping power consumption at satisfactory levels.

ACKNOWLEDGMENTS

Authors would like to express their thankfulness to FAPESP for financial support on chip integration.

REFERENCES

[1] Wang C. and Wu J., “Efficiency Improvement in Charge Pump Circuits.” In IEEE Journal of Solid-State Circuits, vo1.32, No.6, June, 1997, pp. 852-860.

[2] Cheong S.V., Chung H., Ioinovici A, “Inductor-less DC-to-DC Converter with High Power Density.” In IEEE Transactions on Industrial Electronics, vol.41, No.2, April, 1994, pp. 208-215.

[3] Kormann B., “High-Efficiency, Regulated Charge Pump for High-Current Applications.” Unitrode Design Seminar, 2001.

[4] Gregoire B., “A Compact Switched-Capacitor Regulated Charge Pump Power Supply.” In IEEE Journal of Solid-State Circuits, vol. 41, no. 8, August, 2006, pp. 1944-1953.

[5] Bayer, E. and Schmeller, H., “Charge pump with Active Cycle regulation-closing the gap between linear and skip modes.” In Proc. of IEEE 31st Annual Power Electronics Specialists Conference, vol.3, 2000, pp.1497-1502.

[6] Bayer, E. and Schmeller, H., “A high efficiency single-cell cascaded charge pump topology-the competitive alternative to inductive boost converters.” In Proc. Of IEEE 32nd Annual Power Electronics Specialists Conference, vol. 1, 2001, pp. 290-295

[7] F. Pan and T. Samaddar, “Charge Pump Circuit Design” McGraw-Hill, 2006.

[8] Bayer E., Schmeller H. and Sporer G., “Charge Pumps Become Differentiated.” In Proc. of Wireless Symposium Portable by Design, Feb 22-25, 2000.