Carbon Nanotube Circuits: Living with Imperfections and Variations

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Abstract

Carbon Nanotube Field-Effect Transistors (CNFETs) can potentially provide significant energy-delay-product benefits compared to silicon CMOS. However, CNFET circuits are subject to several sources of imperfections. These imperfections lead to incorrect logic functionality and substantial circuit performance variations. Processing techniques alone are inadequate to overcome the challenges resulting from these imperfections. An imperfection-immune design methodology is required. We present an overview of imperfection-immune design techniques to overcome two major sources of CNFET imperfections: metallic Carbon Nanotubes (CNTs) and CNT density variations.

1. Introduction

Carbon Nanotubes (CNTs) are cylindrical nanostructures of carbon with exceptional electrical, thermal and mechanical properties [Saito 98]. CNTs can be used to fabricate Carbon Nanotube Field-Effect Transistors (CNFETs). A representative device structure for a CNFET is shown in Fig. 1.1. Multiple semiconducting Single-Walled Carbon Nanotubes (SWCNTs, or simply CNTs) are grown on or transferred to a substrate. These CNTs act as transistor channels which can be modulated by a gate. The regions of the CNTs under the gate are undoped, while the source and drain regions of the CNTs are heavily doped. The gate, source and drain contacts, and interconnects are defined by conventional lithography. Simulation results show that CNFET circuits can provide significant energy-delay-product benefit compared to silicon CMOS [Deng 07, Patil 09a, Wei 09b]. These improvements over silicon CMOS are primarily due to superior electrostatics and near-ballistic carrier transport in CNTs [Guo 04, Javey 03].

![Image 1.1. Carbon Nanotube Field-Effect Transistor.](image)

There has been significant progress in CNFETs at the single-CNT level [Chen 05, Javey 03, 05]. Despite encouraging prospects, CNFET technology is subject to significant imperfections in addition to those in silicon CMOS. Major sources of these imperfections include metallic CNTs, mis-positioned CNTs and CNT density variations (Sec. 2). State-of-the-art CNT processing techniques alone cannot overcome these CNT imperfections. Hence, an imperfection-immune design paradigm is required, together with advances in CNT processing, to overcome these barriers.

Recent advances in CNFET design and fabrication have enabled the first experimental demonstration of VLSI-compatible imperfection-immune multi-stage CNFET logic circuits. Figure 1.2 shows a multi-stage XNOR logic circuit (half-adder sum generator) reported in [Patil 09c] which is immune to mis-positioned and metallic CNTs, fabricated in a VLSI-compatible manner. In addition, CNFETs can be integrated into monolithic CNFET 3D ICs [Wei 09a].

In Sec. 2, we introduce the major sources of imperfections in CNFET circuits and variations caused by these imperfections. In Sec. 3 and 4, we focus on imperfection-immune CNFET design techniques to overcome two major CNFET imperfections: metallic CNTs and CNT density variations. Section 5 concludes this paper.

![Image 1.2. Fabricated CNFET XNOR function (half-adder sum generator) immune to metallic and mis-positioned CNTs.](image)

2. CNFET Imperfections and Variability: An Overview

One possible benefit of the CNFET technology is that a large portion of the existing manufacturing and design infrastructure for FET-based VLSI can be reused. However, in addition to defects and process variations observed in conventional CMOS processing [Agarwal 07, Bernstein 06], CNFET circuits are subject to sources of imperfections and variations that are unique to CNTs. Most of these imperfections and variations arise from non-idealities in the CNT synthesis process:

- Metallic CNTs (\textit{m-CNTs}). Metallic CNTs create source-drain shorts in CNFETs causing excessive leakage and reduced noise margins in CNFET circuits. About 5%-50% of grown CNTs are metallic [Li 04]. Even though techniques have been developed to selectively remove m-CNTs from an ensemble of m-CNTs and s-CNTs [Collins 01, Zhang 06], the removed CNTs cause density variations in the remaining predominantly semiconducting CNTs (s-CNTs).
- CNT density variations caused by non-uniform spacing between CNTs. As a result, the number of CNTs in CNFETs with a fixed width may have a large variance.
- CNT diameter variations. CNT diameter determines the bandgap of a CNT; thus, CNT diameter variations can cause threshold voltage variations.
- Mis-positioned and mis-aligned CNTs. Mis-positioned and mis-aligned CNTs can cause incorrect logic functionality and reduced drive current [Patil 08a].
The aforementioned imperfections can also result in variations in circuit performance. Figure 2.1 shows simulation results of on-current variations caused by these imperfections (assumptions listed in Table 1). These on-current variations are significantly greater than those reported for conventional silicon CMOS ([Agarwal 07], [Aikawa 08]).

Table 1. Magnitude of CNFET specific variations used in Fig. 2.1 with related references.

<table>
<thead>
<tr>
<th>Variation Source</th>
<th>Distribution</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT Diameter</td>
<td>Normal</td>
<td>[Patil 09a]</td>
</tr>
<tr>
<td>Misalignment</td>
<td>Normal</td>
<td>[Raychowdhury 09]</td>
</tr>
<tr>
<td>Metallic CNTs</td>
<td>Binomial (1/3 m-CNT)</td>
<td>[Saito 98]</td>
</tr>
<tr>
<td>Density Variations</td>
<td>Model from [Zhang 09a]</td>
<td>[Zhang 09a]</td>
</tr>
</tbody>
</table>

Next, we examine the individual contributions of the variation sources to the CNFET on-current variations. As shown in Fig. 2.1, m-CNTs and CNT density variations are dominant contributors to the on-current variations. This is because they directly contribute to the number of conducting CNTs (channels) in a given CNFET. Variations in CNT diameters can result in a significant change in the on-current of a single CNT. However, statistical averaging effects resulting from the multi-CNT CNFET structure substantially suppress the overall variations caused by CNT diameter variations.

The following sections focus on joint co-optimization of design and processing for imperfection-immune CNFET circuits that are immune to metallic CNTs and CNT density variations. CNFET logic circuit design immune to mis-positioned CNTs is discussed in [Patil 08a]. This technique guarantees correct functionality even in the presence of a large number of mis-positioned CNTs with significantly lower cost in area, delay and energy compared to traditional defect tolerance. Hardware prototypes of such immune logic structures at full wafer-scale are demonstrated in [Patil 08b].

3. Metallic CNTs

An m-CNT in a CNFET acts as a conductive channel whose resistance cannot be controlled by the transistor gate. This behavior is undesirable in CNFET-based logic circuits. As discussed in [Zhang 09b], an ensemble of m- and s-CNTs poses major challenges to CNFET-based digital VLSI due to:

1) Excessive leakage: Since m-CNTs cannot be turned off, CNFETs with a typical fraction of 1/3 m-CNTs [Saito 98] can have more than 2,000 times worse $I_{on}/I_{off}$ compared to state-of-the-art CMOS technology.

2) Noise margin degradation: The presence of m-CNTs can result in conducting paths through pull-up and/or pull-down networks of logic gates. Hence, even a small number of m-CNTs in a logic gate can severely degrade its noise margin.

3) Variations in circuit performance: The respective counts of m-CNTs and s-CNTs in a particular CNFET are unpredictable. This leads to performance (e.g. delay) variations in CNFET-based digital circuits.

3.1 Processing Options for Metallic CNTs

The most natural processing option to tackle the m-CNT problem is to grow predominantly s-CNTs. A preferential s-CNT growth technique used by [Li 04] yields 90% s-CNTs. More recently, a growth technique by [Qu 08] reported an even higher s-CNT fraction of 96%. Enriched s-CNTs have also been demonstrated using self-sorting when CNTs are deposited onto the wafer ([LeMieux 08]). While such improvement in enriching s-CNTs is definitely helpful, it alone is not enough for VLSI-scale digital circuits (see Sec. 3.1.1).

The other processing option is to remove m-CNTs after CNT growth from an ensemble of m-CNTs and s-CNTs. Removal can be performed either chemically or electrically. Chemical removal techniques are based on reagents that selectively react with m-CNTs ([Yang 06, Zhang 06]). Even if high removal rates may be achieved, a significant fraction of s-CNTs may also be inadvertently removed.

[Collins 01] introduces a current-induced breakdown technique to remove m-CNTs from individual CNFETs. We refer to this technique as Single-Device electrical Breakdown or SDB. In SDB, s-CNTs are switched off using the gate so that current only flows through m-CNTs. At high current levels, oxidation is induced by self-heating of m-CNTs causing them to break down. SDB achieves ~100% m-CNT removal, but suffers from the following key VLSI challenges:

1. It is impractical to contact gate, source and drain of each CNFET individually in gigascale ICs.

2. m-CNT fragments can produce incorrect logic functionality because internal contacts cannot be accessed for gigascale ICs [Patil 09c].

3. SDB requires top-gate oxide of CNFETs to be thick enough to withstand the high voltage required for m-CNT breakdown (5V-10V [Pop 08]) resulting in reduced circuit performance.

In summary, processing techniques alone are inadequate to overcome m-CNT challenges. Imperfection-immune design, together with processing techniques, is required.

3.1.1. Requirements for Metallic CNT Processing

A key question associated with processing techniques to overcome the m-CNT challenge is: what requirements do they have to satisfy in order to meet practical constraints on circuit performance metrics such as leakage, noise margin, and delay variations?

Probabilistic analysis is necessary in order to answer the above question. Here we list some key results from [Zhang 09b]. The parameters used in this analysis are as follows:

- $p_m$ ($p_s = 1 - p_m$) is the probability that a grown CNT is metallic (semiconducting).
- $p_{Rm}$ ($p_{Rs}$) is the conditional probability that a CNT is removed given it is an m-CNT (s-CNT). An ideal m-CNT removal technique is one for which $p_{Rm} = 1$ and $p_{Rs} = 0$ (i.e., all m-CNTs are removed and all s-CNTs remain intact).
Among these, $p_m$ and $p_{Rm}$ ($p_{Rs}$) are examples of processing parameters, whereas $N$ is a circuit design parameter. Figure 3.1 shows how $P_{Rm}$ affects the average $I_{on}/I_{off}$ ratio of CNFET circuits. The $I_{on}/I_{off}$ ratio is a good indicator of the fraction of leakage power dissipation [Nose 00]. We can determine guidelines for $P_{Rm}$ by applying practical leakage constraints using the probabilistic analysis framework described in [Zhang 09b]. The target $I_{on}/I_{off}$ value of $10^4$ is obtained from [ITRS 07]. It is shown that this target value can be achieved with $P_{Rm} > 1/3$ for $p_m = 1/3$. Compared to $P_{Rm}$, it is much harder to improve the $I_{on}/I_{off}$ ratio using parameters $p_m$ or $P_{Rs}$. For example, even for CNT growth techniques with the lowest achievable $p_m$ to date ($p_m = 5\%$), the desired $I_{on}/I_{off}$ cannot be achieved without the help of m-CNT removal.

![Figure 3.1. $\mu(I_{on})/\mu(I_{off})$ vs. survival probability (1-$p_{Rm}$) (assuming s-CNTs have $I_{on}/I_{off} = 10^5$).](image)

Such probabilistic analysis of processing and design can also quantify the impact of m-CNTs on the noise immunity of logic gates. We use *Probability of Noise Margin Violation (PNMV)* as a metric, which is defined as the probability that a pair of cross-coupled inverters violates a given noise margin requirement (set at $V_{dd}/4$ in the following discussion). Figure 3.2 presents key results from such analysis by showing how PNMV can be affected by different processing and design parameters ($P_{Rm}$, $p_m$, and $N$). CNFETs with larger $N$ have reduced amount of variations. Hence, it is possible to improve the noise immunity of logic gates by using wider CNFETs that contain more CNTs. However, increasing the size of the CNFETs in this way can impose penalties in terms of area, power and delay, and should be performed judiciously. We define $N_{min}$ as the minimum number of CNTs per CNFET prior to removal, for which the PNMV constraint is satisfied. With a target PNMV of $10^8$ as shown in Fig. 3.2, $N_{min}$ should be 28 for $p_m = 1/3$ and $P_{Rm} = 99.99\%$.

![Figure 3.2. PNMV vs. $N$ (details in [Zhang 09b]).](image)

For a particular design, enforcing the $N_{min}$ constraint requires that the sizes all CNFETs that contain fewer than $N_{min}$ CNTs be increased so that they contain at least $N_{min}$ CNTs. For example, if the CNT pitch is 4 nm [Deng 07], then all CNFETs of widths less than $4 \times 28 = 112$ nm need to be sized up. The circuit-level penalty associated with such CNFET sizing depends on the technology node and specific design. An OpenRISC processor design ([OpenCores 09]) synthesized with Nangate 45nm Open Cell Library ([Nangate 09]) incurs total gate capacitance increase of about 2% when this $N_{min}$ constraint is enforced.

### 3.2. VMR: Imperfection-Immune Design Combining Design Techniques with Processing

A new imperfection-immune design technique, called *VLSI-compatible Metallic-CNT Removal (VMR)* [Patil 09c], combines new CNFET circuit design techniques with processing to overcome the challenge of m-CNTs.

A special layout called *VMR structure* is fabricated on a silicon wafer with back-gate oxide (Fig. 3.3). The VMR structure consists of inter-digitated electrodes at minimum metal pitch. VLSI-compatible m-CNT electrical breakdown is performed by applying high voltage across m-CNTs all at once using the VMR structure. The back-gate is used to turn off the s-CNTs.

![Figure 3.3. Top view (a) and cross-sectional view (b) of VMR structure consisting of 6 inter-digitated VMR electrodes. (c) SEM Image of VMR structure (top view).](image)

VMR retains the benefits of SDB while overcoming VLSI challenges faced by SDB:

1. VMR does not require any top-gate because the back-gate is used for m-CNT breakdown. This enables a thin top-gate oxide that can be fabricated for high performance CNFETs after m-CNT breakdown. The effect of the back-gate capacitance during normal circuit operation can be minimized by using a thick back-gate oxide since the back-gate is not needed during normal circuit operation.

2. VMR does not require any mechanism to contact each CNFET separately.

3. The problem of m-CNT fragments is overcome since all internal contacts can be accessed using the VMR structure (parts of which are etched to create the final intended design).

The VMR structure is independent of the final intended design. Regions of the VMR structure to be etched out are predefined during layout design and no die-specific customization is required. Any arbitrary final design (e.g., Fig. 3.4c) can be created by etching out parts of the VMR structure as long as an additional contact (at minimum metal pitch) is added for series-
connected CNFETs for logic library cells [Patil 09c]. This incurs < 2% area penalty and 3% delay penalty at the chip level, based on synthesis results of large designs (OpenRISC processor, Ethernet controller [OpenCores 09]).

To restore the drive current, CNFETs are connected in parallel along the y-direction (i.e., direction of CNT growth), where the CNFETs are identical. Since connecting statistically correlated CNFETs together does not change the probabilities, current drive can be restored without compromising m-CNT tolerance. An example of such an implementation is shown in Fig. 3.5c and Fig. 3.5d.

3.3. ACCNT: Imperfection-Immune Design Technique with Minimal Reliance on Processing

ACCNT (Asymmetrically Correlated CNT) [Lin 09] is a technique to achieve m-CNT tolerance with minimal reliance on processing (e.g., directional CNT growth). Even in the presence of a significant fraction of m-CNTs, ACCNT CNFETs attain a high on-off ratio comparable to CNFETs with only s-CNTs.

Figure 3.5 summarizes the basic concepts of the ACCNT technique. First, multiple statistically independent CNFETs are connected in series along the x-direction (i.e., perpendicular to the direction of CNTs), with the gates of all CNFETs connected together, such that the entire series operates as one transistor with one gate. If at least one CNFET in the series consists of only s-CNTs, the overall series will exhibit high on-off ratio. By connecting several independent CNFETs in series, the probability that all the CNFETs contain m-CNTs decreases exponentially, and thus the series chain achieves m-CNT tolerance. However, by connecting CNFETs in series, the overall drive current is proportionally reduced.

Using ACCNT, high $I_{on}/I_{off}$ is achieved, similar to that of CNFETs with s-CNTs only, despite the presence of m-CNTs (Fig. 3.6a). We also successfully demonstrated ACCNT CNFETs and PMOS-logic inverters, at wafer-scale, that satisfy the requirements of digital logic (Fig. 3.6b).

ACCNT, being an entirely design-based solution with minimal reliance on processing, will, in some scenarios, incur expensive design costs. In particular, when the percentage of m-CNTs is very large (>10%), the ACCNT area overhead can become quite large. This also translates into significant delay and power overheads (e.g., from larger device capacitances and longer interconnects). Combining ACCNT with a processing solution can potentially overcome this problem.

4. CNT Density Variations

Both CNT density and CNT density variations pose significant challenges to CNFET-based VLSI circuits. [Deng 07, Wei 09b] show that, for optimal energy-delay tradeoffs, we need CNFETs with CNT density of 100-250 CNTs/µm. In
In contrast, state-of-the-art CNT growth techniques yield typical densities of only 10-50 CNTs/μm [Kang 07]. To increase average CNT density, technology advances are essential. In addition to the need for high CNT density, CNT density variation is also a major challenge for a viable CNFET technology. CNT density variations result in large delay variations and a significant probability of complete failure in cases where there might be CNFETs with no CNTs.

In the presence of CNT density variations, the quantity \( N \) (i.e., the number of CNTs in a CNFET prior to m-CNT removal) introduced in Sec. 3 must be treated as a random variable. Instead of directly controlling \( N \), designers can only control the width of a CNFET (defined by lithography), denoted by \( W \), which contains a random number of CNTs. [Zhang 09a] presents a parameterized model that relates the probability distribution of \( N \) with the distribution of CNT spacing (Fig. 4.1). This model greatly simplifies the characterization process since CNT spacing is independent of CNFET width.

While ACCNT CNFETs (Sec. 3.3) use asymmetric correlation to overcome the challenge of m-CNTs, such asymmetric correlation is also of great importance (even in the absence of m-CNTs) when designing CNFET circuits in the presence of density variations. Here, correlation refers to the number of CNTs contained in different CNFETs \((N)\), in addition to the type of CNT (m-CNT or s-CNT). Experimental proof for such correlation in CNT count is presented in [Zhang 09a].

Figure 4.2 shows possible layout design options for optimizing delay variations of multi-stage inverter chains in the presence of CNT count correlation. In Fig. 4.2a, all 3 inverters contain uncorrelated CNTs since the CNFETs are laid out perpendicular to the direction of CNT growth. On the other hand, Fig. 4.2b shows a correlated inverter chain where all 3 inverters have correlated CNFETs laid out along the direction of the CNTs. The delay variations of these two designs are analyzed with Monte Carlo simulations using a CNFET SPICE model [Deng 06]. The results are shown in Fig. 4.2c. The correlated inverter chain has smaller delay variations when the number of stages is small, because the load and current drive are both proportional to CNT count. As the number of inverter stages increases, statistical averaging decreases the delay variations of the uncorrelated inverter chain.

CNT correlation can also be utilized to improve the noise immunity of CNFET circuits. Consider five possible layouts of a pair of cross-coupled inverters shown in Fig. 4.3. The different layout styles have varying degrees of correlation among the four CNFETs comprising the cross-coupled inverters. The symmetries in the voltage transfer curves (VTCs) caused by such correlation are also shown in Fig. 4.3. Given CNT density distribution, CNT processing parameters \( (\rho_{Rms}, \rho_{R}) \) and the width of the CNFETs \((W)\), we can calculate the PNMV as defined in Sec. 3.1.1.
Figure 4.4 shows the simulated PNMV for the 5 layout styles as a function of the removal probability of m-CNTs ($p_{Rm}$). Symmetry in the VTCs of the two inverters, introduced by correlation among CNFETs, plays an important role in determining the PNMV. Layout styles 1, 2 and 3 ensure symmetry between the two “eye-openings” of the VTC curves and therefore have low PNMV values. Style 4 has the highest PNMV for all values of $p_{Rm}$ because of the anti-symmetry in the VTC curves (Fig. 4.3d). Style 5 has no inherent symmetry because all the CNFETs are uncorrelated and have intermediate values of PNMV.

5. Conclusions

CNFET technology shows big promise as an extension to silicon CMOS. Processing techniques alone are inadequate to overcome the challenges resulting from CNFET imperfections such as metallic CNTs, mis-positioned CNTs, and CNT density variations. Hence, an imperfection-immune CNFET-based circuit design methodology, in conjunction with advances in CNFET processing, is required. An imperfection-immune technique called VMR is described. VMR combines layout design with processing to overcome metallic CNT challenges for CNFET circuits. Large degree of CNT correlation is observed in directional CNT growth. Such correlation can be successfully used to overcome the challenges from metallic CNTs and CNT density variations.

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References