



## Analysis of DDR3 SDRAM Standard Technology

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### Abstract

With requirements of high data transmission efficiency, as the new SDRAM standard, DDR3 has gradually entered into our views. This article will analyze main functions of DDR3 and mainly compare DDR3 with DDR2.

**Keywords:** DDR3, ODT

### 1. Introduction

After long-term waiting, EMS memory standard organization JEDEC claimed that drafting, development and publication of DDR3 standard had been completely ended and this standard had normally been the industry standard. The data transmission efficiency of present DDR2 can achieve 800MHz, and its core work frequency has achieved 200MHz, so it is more and more difficult to realized higher data transmission efficiency through continually enhancing the core work frequency. And because the developments of market and technology require continual enhancements of data transmission efficiency, so DDR3 is the production to big extents when the market faces this sort of corner.

### 2. Basic functions of DDR3

DDR3 has no subversive designs, and it is ameliorated on the bases of DDR2. DDR3 adopts lower voltage of 1.5V according with the standard of JEDEC SSTL-1.5, and because it adopts the prefetch design of 8bit, comparing with DDR2 core with the prefetch design of 4bit, the work frequency of DDR3 is half reduced. For example, when the exterior data transmission efficiency is 800Mb, the work frequency of DDR3 is only 100MHz and DDR2 is 200MHz, so DDR3 can realize higher data transmission efficiency. Table 1 shows explanations of various DDR3 signals.

### 3. Similarities and differences between DDR3 and DDR2

Comparing with DDR2, DDR3 has been adjusted in many aspects such as encapsulation, work voltage, ODT, heat sensor, output control, the quantity of bank and so on. The detailed ameliorations are introduced as follows.

#### 3.1 Low voltage and low power

On the base that the work voltage of DDR2 is 1.8V, the work voltage of DDR3 is reduced to 1.5V, 16% of original voltage, which will compensate power increase brought by enhancement of work frequency. And DDR3 adopts new technique and makes its kernel size smaller than original one, which will also bring the effect of power decrease. Some relative data forecast DDR3 will save 30% of power than present DDR2. Balancing bandwidth and power consumption, comparing with present DDR2-800, the power consumptions of DDR3-800, 1066 and 1333 are respectively 0.27 times, 0.83 times and 0.95 times, and the DDR3-800 not only possesses wider bandwidth, but also has less power consumption. The reference voltage signal VREF which is very important for the work of EMS memory system is divided into two signals. The reference voltage which can order, control and address signal is VREFCA, and VREFDQ services for data signals. This design can be similarly thought in one same reference voltage surface, instantaneous currents brought by large of signals are reduced, and accordingly the signal-to-noise class of system data bus can be effectively enhanced.

The tolerable degree of voltage signals to the uprush area and undershoot area is reduced comparing with DDR2, for example, classical VDD and VDDQ voltage of DDR3 is  $1.5V \pm 0.75V$ , and the maximal uprush and undershoot peak value of address/order/control/data/clock signals is  $\pm 0.4V$ . Considering various factors such as DDR3 grain topological structure, actual situation of layerout trace, equivalent resistance, PCB material, the quality requirement to signal is higher than DDR2. In addition, we can rewrite ODT Register of DDR3 EMS memory controller to restrain the uprush and undershoot on the data and address lines. The definitions of the uprush area and the undershoot area for voltage signal are seen in Figure 1.

#### 3.2 Increase the quantity of logic bank

DDR2 has designs of 4 Banks and 8 Banks, which aim is to face future demands for large capability CMOS chip. But the initiative logical Bank has eight ones, which aim is to offer technological repertory for the CMOS chip possesses 16 logical Banks, thus DDR3 can start from higher capability.

#### 3.3 Encapsulation

The biggest breakthrough of DDR2 technology is actually not the ability of double transmission to DDR thought by

users, but it can acquire higher frequency enhancement and break through the limitation of 400MHz of standard DDR under lower heat and power consumption. The DDR EMS memory usually adopts encapsulation of TSOP chip, and this encapsulation form can work on 200MHz well, and when the frequency is higher, its overlong pins will produce high impedance and parasitical capacitance, which will influence its stability and the difficulty of frequency enhancement. DDR2 adopts the encapsulation form of FBGA which can offer better electric performance and heat elimination (but when the form of the positive and negative chip is adopted, FBGA can not adopt ICT test, so the new problem of test occurs.) and make grains more stably work and offer good guarantees for the developments of future frequency. DDR3 inherits the encapsulation advantage of DDR2, and it adopts new technology small than  $0.1 \mu\text{m}$ , which makes kernel size smaller than original one, saves power consumption, reduces encapsulation heat and possesses better electric performance.

Because DDR3 increases some functions, so it increases some pins and improves pin distribution and signal reference. The 8bit chip adopts 86 ball FBGA encapsulation (because the encapsulation forms of Micron and Samsung are different, this article takes Micron as the example.), and 16bit chip adopts 96 ball FBGA encapsulation, and DDR2 has the encapsulation standard of 60/84 ball FBGA. DDR3 must adopt the green encapsulation without lead and accord with the standard of RoHs. In addition, the pin distribution of DDR3 encapsulation is symmetrical, which can enhance pin use rate and have more power pin distribution comparing with DDR2.

### 3.4 New function of "Reset"

"Reset" is an important new function of DDR3, and DDR3 specially prepares a pin for that. This pin makes the initialization processing of DDR3 become simple. When the order of "Reset" is effective, DDR3 memory will stop all operations and switch to least activity status to save electric power. In the process of "Reset", DDR3 memory will close most interior functions, all data receivers and transmitters will be closed, all interior program sets will be reset, DLL (Delay Locked Loop) and clock circuit will stop working and ignore any changes on the data but, which can reduce power consumption for DDR3.

### 3.5 New function of "ZQ adjustment"

DDR2 uses OCD to enhance the signal integrality through reducing the incline of DQ-DQS and enhance signal quality through controlling voltage. OCD realizes the function through adjusting the values of pull-up resistance and pull-down resistance. But DDR3 increases one ZQ pin which joints one low tolerance reference resistance of 240 ohm. This pin can automatically test on-resistance of data output driver and end resistance of ODT through an order set and On-Die Calibration Engine (ODCE). When the system sends this order, it will use corresponding clock cycle (512 clock cycles are used after electricity and initialization, 256 clock cycles are used after exiting self-refresh operation, 64 clock cycles are used under other conditions.) to readjust on-resistance and ODT resistance for actualizing better matching, which is more precise comparing with DDR2 which uses voltage and current thresholds to confirm the value of RTT. The on-resistance adjustment principle of output driver is seen in Figure 2, where, the enabling pull-up resistance  $R_{ON_{PU}} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$ , and the enabling pull-down resistance  $R_{ON_{PD}} = (V_{DDQ} - V_{OUT}) / |I_{OUT}|$ .

### 3.6 Burst Length, BL

The Burst Length (BL) of DDR3 is fixed at 8, and the prefetch operation is also 8bit. Relative to DDR2 and early DDR structure, the BL in common use for the system is 4, and DDR3 increases a 4bit Burst Chop pattern, i.e. a read-write operation with  $BL=4$  and a write operation with  $BL=4$  compose a data Burst Length with  $BL=8$ , and this burst pattern can be controlled by A12 address line. And any burst interrupt operation will not be supported in DDR3, and more flexible burst transmission control will be used.

### 3.7 Timing

Just like that the delay cycle of DDR2 would be increased when it is transformed from DDR, the CL cycle of DDR3 will be also enhanced comparing with DDR2. The CL range of DDR2 is usually in 2 to 5, and this range of DDR3 is in 5 to 11, and the design of additional delay (AL) changes. The AL range of DDR2 is in 0 to 4, and the AL of DDR3 has three forms which respectively are 0, CL-1 and CL-2. In addition, DDR3 also increase a timing parameter, CWD, which is confirmed by concrete work frequency.

### 3.8 Refresh of timing characteristic

The CL cycle of DDR3 is enhanced comparing with DDR2, the CL range of DDR2 is usually in 2 to 5, this range of DDR3 is in 5 to 11, and the design of additional delay (AL) changes. The AL range of DDR2 is in 0 to 4, and the AL of DDR3 has three forms which respectively are 0, CL-1 and CL-2. In addition, DDR3 also increase a timing parameter, CWD, which is confirmed by concrete work frequency. The CAS delay time of the memory has close relations with access time. The so-called CAS time is the response time of lengthways address pulse of the memory. The CAS delay time is one of important signs to measure the memories supporting different standards under certain frequency. According to these data, we likely find that the CAS time of DDR3 is worse than DDR2's, but through referring concrete delay parameter time, we find that the CAS time of DDR3 presents downtrend, i.e. the CL time of DDR3 is shorter than DDR2's. For example, the CL/RCD/RP values of DDR2-533 are respectively 4-4-4, so the CL time is 15ns,

and the CL/RCD/RP values of DDR3-1066 are respectively 7-7-7, so the CL time is reduced to 13.125ns, and if the CL/RCD/RP values of DDR3-1600 are respectively 9-9-9, so the CL time can be reduced to 11.25ns.

### 3.9 Design of automatic refresh

To ensure that the saved data can not be lost, DRAM must implement refresh at a certain time, and DDR3 can not be exceptional too. But for saving maximal electric power, DDR3 adopts a sort of new automatic self-refresh (ASR) design. When ASR begins, the refresh frequency is controlled by a temperature sensor inside DRAM chip, and because the refresh frequency is high, the power consumption will increase and the temperature will increase with it. And the temperature sensor can try to reduce refresh frequency and work temperature and ensure the data can not be lost at the same time. The ASR of DDR3 is a selectable design, and not all DDR3 memories in the market can support this function, so there is an additional function, self-refresh temperature (SRT). Through pattern register, two temperature ranges can be selected, and one is common temperature range (for example 0 centigrade degrees to 85 centigrade degrees), and the other is extended temperature range, for example, the highest temperature can achieve 95 centigrade degrees. To these sorts of temperature ranges set in the DRAM, DRAM will implement refresh operation with constant frequency and current.

## 4. Conclusions

This article emphasize the new characters and advantages of DDR3 comparing with DDR2. In the day that DDR2 is extensively applied, people expect it can quit the historical stage as soon as possible and continue to lead the step of SDRAM family. In the road map published by Intel at present, the series chips of Bearlake-X will integrate DDR3 memory controller, and with the support of CPU manufacturers, various chip groups and network processors supporting DDR3 will also occur continually. Therefore, we have enough reasons to believe the age of DDR3 will come soon.

## References

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 MICRON. (2007). *MT41J512M4/MT41J256M8JE*.

Table 1. Explanations of various DDR3 signals

Signals	Type	Explanation
CK/CK#	I	Difference clock signal: all addresses and control input signals are sampled on the ascending border of CK and the descending border of CK#.
CKE	I	Clock enabling signal: high efficiency, the high voltage must be kept in the process of read-write.
CS#	I	Interrupt signal: when many DDR3 grains exist in the system, this signal can be one part of control orders through signal selection.
ODT	I	Interior end: the interior terminal resistance of DDR3 can effectively restrain the reflected noises in the transmission path and improve the integrality of the signal.
RAS#/CAS#/ WE#	I	Order input signal: when the signal is effective, the order is thought it has been inputted.
DM/(DMU)/ (DML)	I	Data input sign: in the write operation process, the data input is thought that the sampling is high.
BA0-BA2	I	Block address input: deciding which block is activated, read-written, pretreated.
A0-A15	I	Address line: providing row and list addresses for various operations.
A10/AP	I	Pretreatment: sampling read-write order cycle A10 to decide whether implementing automatic pretreatment after read-write operation.
A12/BC#	I	Burst break: sampling read-write order cycle and deciding whether burst break exists.
RESET#	I	Reset signal: low efficiency, CMOS voltage.
DQ	I/O	Data input and output: bidirectional data signals.
DQU/DQL/DQS/ DQS#/DQSU/ DQSU#/DQSL/ DQSL#	I/O	DQS/DQS #: referring edge intersection of CK/CK#.
TDQS/TDQS#	O	Terminal data check: it only is used in grain X8, and can realize the function similar to the terminal resistance of DQS/DQS# through pattern register enabling.

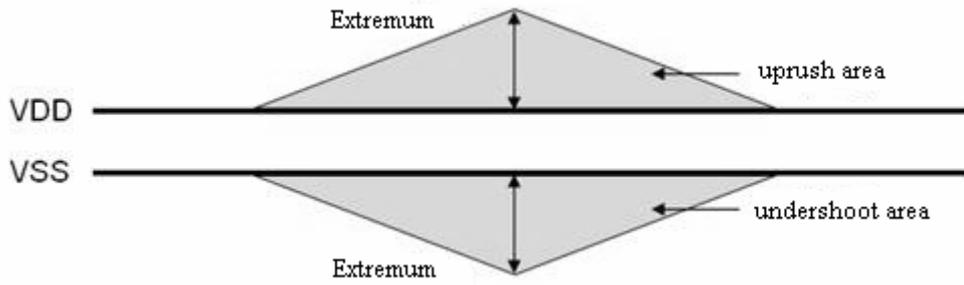


Figure 1. Definitions of the Uprush Area and the Undershoot Area for Voltage Signal

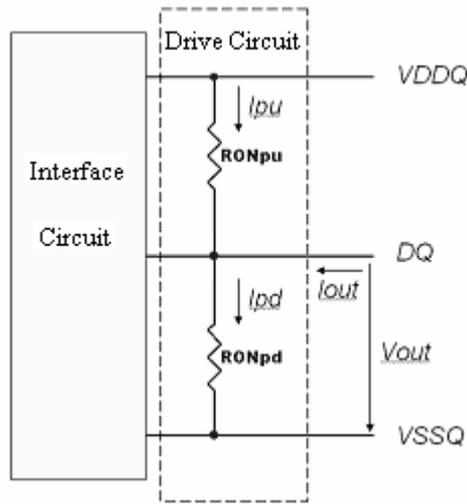


Figure 2. Output Drive Circuit