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Al_2O_3-Dielectric InAlN/AlN/GaN Γ-Gate MOS-HFETs with Composite Al_2O_3/TiO_2 Passivation Oxides

Ching-Sung Lee, Xue-Cheng Yao, Yi-Ping Huang, and Wei-Chou Hsu

***Abstract*—Novel Al_2O_3-dielectric InAlN/AlN/GaN Γ-Gate metal-oxide-semiconductor heterostructure field-effect transistors (MOS-HFETs) with composite Al_2O_3/TiO_2 passivation oxides formed by using ultrasonic spray pyrolysis deposition (USPD)/RF sputtering, respectively, are investigated. The Γ-gate includes a 1-μm long active gate on the Al_2O_3 dielectric and a 1-μm long field-plate (FP) on the composite Al_2O_3/TiO_2 oxides. The present Γ-Gate MOS-HFET has demonstrated excellent on/off current ratio (I_{on}/I_{off}) of 8.2 × 10^{10}, subthreshold swing (SS) of 102.3 mV/dec, maximum extrinsic transconductance of ($g_{m,\,max}$) of 210.1 mS/mm, maximum drain-source saturation current density ($I_{DS,\,max}$) of 868.3 mA/mm, two-terminal off-state gate-drain breakdown voltage (BV_{GD}) of -311.2 V, three-terminal drain-source breakdown voltage (BV_{DS}) of 237 V at V_{GS} = -10 V, and power-added efficiency *(P.A.E.)* of 39.9% at 2.4 GHz. A conventional Schottky-gate HFET and TiO_2-dielectric MOS-HFET were also prepared in comparison. The present design has shown superior DC/RF device performance. It is suitable for high-power RF circuit applications.**

***Index Terms*—MOS-HFET, InAlN/AlN/GaN, Al_2O_3/TiO_2, ultrasonic spray pyrolysis deposition, RF sputtering, on/off current ratio, subthreshold swing, field-plate, passivation, P.A.E..**

I. Introduction

GAN heterostructure field-effect transistors (HFETs) having superior properties of large breakdown field (~5 MV/cm), wide bandgap (3.4 eV), and high electron mobility (~1500 cm^2/V-s) are advantageous to high-power circuit applications. The two-dimensional electron gas (2DEG) can be induced within the AlGaN/GaN heterointerface by the piezoelectric and spontaneous polarization effects [1-2]. A thin AlN spacer was commonly inserted to reduce the alloy scattering [3] and to improve the carrier confinement and transport property. Lately, InAlN/GaN heterostructures have been applied to the HFET designs [4-7]. $In_{0.18}Al_{0.82}N$, lattice-matched to the GaN channel, has larger bandgap than AlGaN and can also provide higher 2DEG concentration. Reduced gate leakage current, improved interface, and enhanced current densities can be obtained at the same time. On the other hand, the metal-oxide-semiconductor gate (MOS-gate) structure has been widely studied [8-14] to improve the gate insulation, reduce the effective oxide thickness (EOT), and provide surface passivation. Various oxide formation techniques were employed, including e-beam evaporation [15], atomic layer deposition (ALD) [16], sputtering [17], chemical vapor deposition (CVD) [18], and hydrogen peroxide oxidization [19]. This work presents a novel Al_2O_3-dielectric Γ-gate $In_{0.17}Al_{0.83}N$/AlN/GaN MOS-HFET with composite Al_2O_3/TiO_2 passivation oxides formed by using USPD/RF sputtering, respectively. The Γ-gate [20] structure includes a 1-μm long active gate on the wide-gap Al_2O_3 dielectric and a 1-μm long field-plate (FP) formed on the composite Al_2O_3/TiO_2 oxides. Effective passivation for the $In_{0.17}Al_{0.83}N$ barrier surface was achieved by growing Al_2O_3 using the ultrasonic spray pyrolysis deposition (USPD) technique. The high-k wide-gap Al_2O_3 gate dielectric is beneficial to improving the channel modulation and gate insulation. Besides, the composite Al_2O_3/TiO_2 oxides below the FP can reduce the gate-drain leakage within the high-field gate-drain region and reduce the parasitic capacitance at the same time. In comparison, a conventional Schottky-gate HFET and a TiO_2-dielectric MOS-HFET formed by the RF sputtering have been fabricated on the same epitaxial structure. Various characterizations of C-V measurement, TEM, energy-dispersive X-ray spectroscopy (EDS), low-frequency noise spectra, and Hooge's coefficient (α_H) have been performed to investigate the material and interface property.

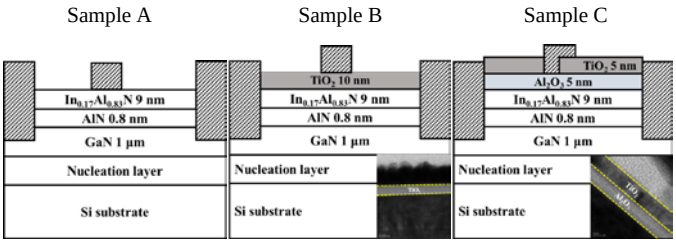

Fig. 1. Schematic diagrams of the studied samples A-C. The insets show the corresponding TEM photos for the grown oxides in samples B-C.

II. Material Growth and Device Fabrication

Fig. 1 shows the schematic device diagrams for the studied devices, including the control Schottky-gate HFET (sample A),

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the reference TiO_2-dielectric MOS-HFET (sample B), and the present Al_2O_3-dielectric Γ-gate MOS-HFET with composite Al_2O_3/TiO_2 passivation oxides (sample C). All three devices have the identical epitaxial structure grown by using a low-pressure metal-organic CVD (LP-MOCVD) system. Upon the Si substrate, the layer structure consists of a 1-μm thick GaN channel, a 0.8-nm thick AlN spacer, and a 9-nm thick $In_{0.17}Al_{0.83}N$ barrier layer. Standard photolithography and lift-off techniques were used for device fabrication [21]. For the present sample C, mesa etching was performed by using an inductively coupled-plasma reactive ion etcher (ICP-RIE) The mixed etching gases are Cl_2 and Ar with the flow rates of 30 sccm and 10 sccm, respectively. The power settings for ICP and RIE are 70 W and 120 W. Metal stacks of Ti (10 nm)/Al (100 nm)/Au (50 nm) were evaporated as the source and drain electrodes. The sample was annealed at 900°C for 30 seconds to form ohmic contacts by using the ULVAC MILA-5000 rapid thermal annealing (RTA) system. A 5-nm thick Al_2O_3 and a 5-nm thick TiO_2 were grown within the exposed gate-drain/source regions by using USPD and RF sputtering, respectively. Then, a 1-μm wide active window was defined after photolithography. Ni was used as etching barrier. Gate recess was formed by dry-etching away TiO_2 to expose the Al_2O_3 oxide surface. The etching time is 10 seconds. Finally, Ni (100 nm)/Au (50 nm) were deposited and lift-off after gate photolithography to form the Γ-gate electrode for sample C, as shown in Fig. 1.

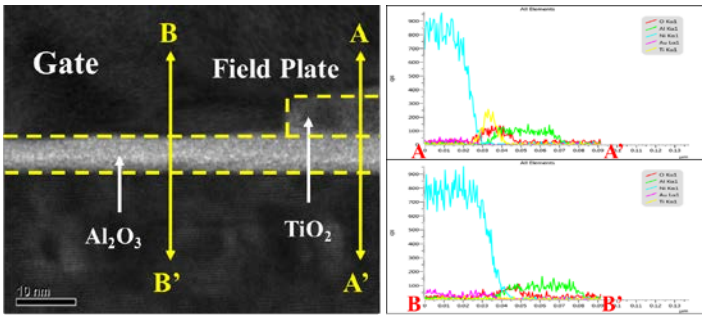

Fig. 2. Cross-sectional TEM photo and the EDS profiles along A-A' and B-B' directions for the MOS Γ-gate structure in sample C.

For sample C, the gate length (L_G) deposited on the Al_2O_3 dielectric is 1 μm. A 1-μm long FP structure was also formed on the composite oxides. For sample A, the gate electrode was directly evaporated on the $In_{0.17}Al_{0.83}N$ barrier without oxide formation. For sample B, a 10-nm thick TiO_2 layer was sputtered within the entire gate-drain region before gate deposition. L_G is 2 μm for both samples A-B. The gate-drain separation is 10 μm and the gate-drain (source) spacing is 4.5 (3.5) μm for all three devices. Post device annealing (PDA) was performed for sample C (B) at 600 °C for 1 (3) minute. With respect to the device configuration, comparisons between samples A and B was intended to manifest the MOS-gate design with RF-sputterred TiO_2 gate dielectric and surface passivation. Comparisons of sample C with respect to samples A-B was devised to investigate the present Γ-gate design with USPD-grown Al_2O_3 gate dielectric and composite Al_2O_3/TiO_2 passivation oxides. Especially, L_G of sample C can be reduced to be 1 μm by using the same 2-μm gate mask as in fabricating samples A and B. The insets of Fig. 1 shows the TEM photos for the grown oxides in samples B-C, respectively. The thicknesses for Al_2O_3 and TiO_2 were confirmed as described. The cross-sectional TEM photo for the MOS Γ-gate structure of sample C is shown in Fig. 2. The EDS profiles along A-A' and B-B' directions have verified the devised Γ-gate structure in sample C.

III. Experimental Results and Discussion

Fig. 3 shows the measured C-V hysteresis characteristics for samples A-C at 1 MHz and 300 K. The corresponding biases were increased from -7/-5/-5 V to -2/-3.5/-3.5 V for samples A/B/C and then swept back to the starting point immediately. The C-V curves were measured between gate and shorted source/drain electrodes from two adjunct devices. The C-V hysteresis is caused by the trapping and detrapping phenomena associated with interface states or oxide trapped charges [22]. The hysteresis was determined by the voltage difference (ΔV) between the mid-points of the C-V curves. The ΔV values are 0.36 V, 0.22 V, and 0.11 V for samples A-C. Lower ΔV of sample B than sample A is attributed to the surface passivation effect by the RF-sputtered TiO_2 oxide. Furthermore, sample C has lower ΔV than sample B is due to the improved surface passivation of the present composite Al_2O_3/TiO_2 passivation oxides formed by USPD and RF sputtering. This indicates that the present USPD technique may avoid the surface damage caused by the sputtering bombardment. The ΔV in sample C is also lower than 0.16 V of the ALD-grown Al2O3 [23]. It is noted that the capacitances measured for sample A swept back from -2 V to -7 V are higher than those when biased from -7 V to -2 V. It was suggested [24] to be due to the electron emissions from the traps within InAlN/AlN interface. As for samples B-C, lower capacitances were observed, instead, when swept back the bias. It was believed to be caused by the negative charges due to oxygen interstitials [25-26] within the grown oxides. The depletion capacitance (C_{dep}) in sample A and the equivalent MOS capacitance (C_{MOS}) in sample B were measured to be 155.9 pF and 93.7 pF. C_{MOS} for an Al_2O_3-dielectric MOS-HFET, similar to the device structure sample B, was measured to be 86.8 pF. The oxide thickness is 10 nm and the area for the adjunct devices is 2000 μm^2. By $1/C_{MOS} = 1/C_{ox} + 1/C_{dep}$, where C_{ox} is the oxide capacitance, C_{ox} was extracted to be 234.8 (195.8) pF for device with TiO_2 (Al_2O_3) dielectric. The relative permittivity (k) was determined to be 11.1 and 132.7 for the grown Al_2O_3 and TiO_2, respectively. The interface density (D_{it}) can be calculated by using the high/low-frequency method [27-28]. The C-V characteristics measured at 1 M and 10 kHz for samples B-C are shown in Fig. 4. The insets show the extracted D_{it} profiles. Lower D_{it} in average of 2.2×10^{11} cm^{-2}-eV^{-1} in sample C than 9.3×10^{11} cm^{-2}-eV^{-1} in sample B indicates the improved interfacial quality by the devised composite Al_2O_3/TiO_2 passivation layers. Fig. 5

compares the low-frequency noise (1/*f*) spectra measured by using an Agilent 35670A amplifier and a BTA 9812B spectrum analyzer. Samples B-C (A) were biased at V_{GS} = -2 (-1) V and V_{DS} = 3 (3) V. The α_H at f = 100 Hz was determined to be 7.7 × 10^{-5}, 4.9 × 10^{-7}, and 9.7 × 10^{-8}. The lowest α_H of sample C shows its best improved interfacial quality [29]. The composite Al_2O_3/TiO_2 oxides have effectively passivated the recombination centers [30] on the InAlN barrier surface.

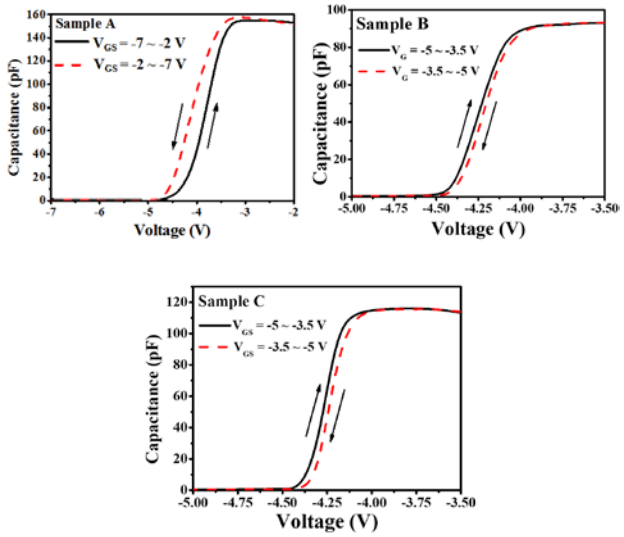

Fig. 3. C-V hysteresis characteristics for samples A-C at 1 MHz and 300 K.

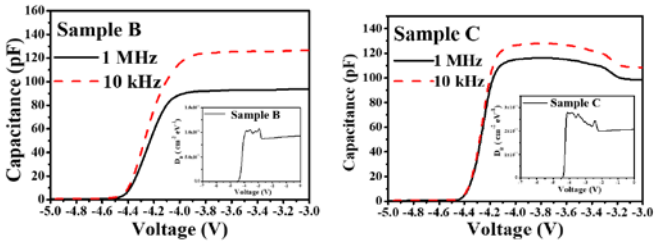

Fig. 4. C-V characteristics measured at 1 M and 10 kHz for samples B-C. The insets show the extracted D_{it} profiles.

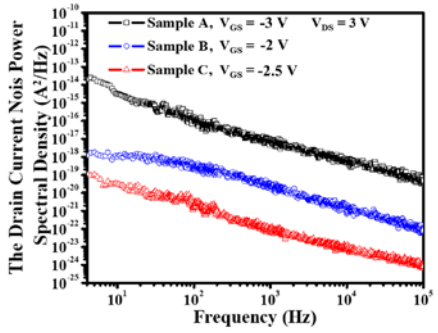

Fig. 5. Comparisons of 1/*f* spectra for samples A-C.

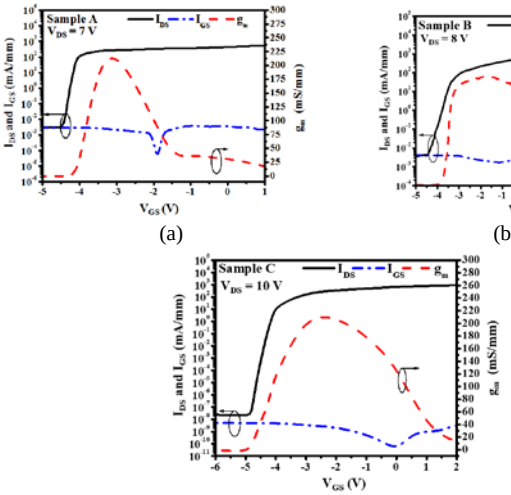

Fig. 6. Transfer g_m, I_{DS}, and the associated I_{GS} characteristics for samples A-C at 300 K.

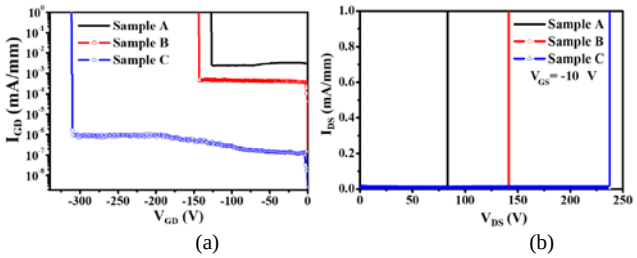

Fig. 7. Two-terminal off-state I_{GD}-V_{GD} and the three-terminal on-state I_{DS}-V_{DS} characteristics at V_{GS} = -10 V for samples A-C at 300 K.

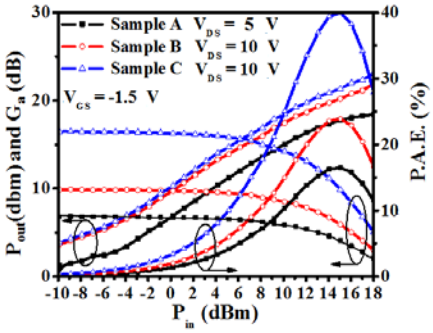

Fig. 8. P_{out}, G_a, and P.A.E. characteristics at 2.4 GHz for samples A-C at 300 K.

The transfer extrinsic transconductance (g_m), saturated I_{DS}, and the associated gate current density (I_{GS}) characteristics at 300 K and V_{DS} = 7/8/10 V for the samples A/B/C are shown in Figs. 6(a)-(c), respectively. The maximum I_{DS} ($I_{DS,\ max}$) densities of samples A-C were found to be 544.2 mA/mm at V_{GS} = 3 V, 815.7 mA/mm at V_{GS} = 5 V, and 868.3 mA/mm at V_{GS} = 5 V. As described before, the gate configurations in samples A-C are different. Higher V_{GS} bias can be applied in samples B-C than sample A is due to enhanced gate insulation of the MOS-gate design. It is favorable to induce higher I_{DS} densities. Besides, sample C has higher $I_{DS,\ max}$ than sample B at the same V_{GS} voltage. It is mainly due to the reduced L_G of the present

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Γ-gate design. About 60% (50%) improvement in $I_{DS,\,max}$ has been achieved in sample C (B), as compared to sample A. Due to the increased gate-to-channel distance by the insertion of gate oxide, sample C has lower $g_{m,\,max}$ of 210.1 mS/mm than 221.2 mS/mm in sample A, though both devices have the same L_G of 1 μm. Lower $g_{m,\,max}$ of 194.7 mS/mm than samples A and C are mainly due to the L_G difference. The subthreshold swing (SS) and on/off current ratio (I_{on}/I_{off}) for samples A-C were characterized to be 125.2 mV/dec and 1.7×10^5, 117.5 mV/dec and 6.4×10^5, and 102.3 mV/dec and 8.2×10^{10}, respectively. It can be seen that the I_{GS} leakage was deteriorated in sample B. It was believed to be caused by the surface damage by bombardment during TiO_2 sputtering. The USPD-grown Al_2O_3 has demonstrated improved interfacial quality to keep I_{GS} leakage around 10^{-9} mA/mm. Consequently, sample C has shown superior SS and I_{on}/I_{off} performances.

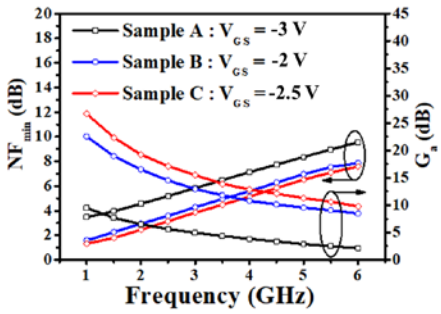

Fig. 9. Nosie characteristics at 2.4 GHz for samples A-C at 300 K.

Figs. 7(a)-(b) show the two-terminal off-state I_{GD}-V_{GD} and the three-terminal on-state I_{DS}-V_{DS} characteristics at V_{GS} = -10 V for samples A-C at 300 K. The two-terminal gate-drain breakdown/three-terminal on-state drain-source breakdown voltages (BV_{GD}/BV_{DS}) were defined as the corresponding V_{GD}/V_{DS} biases where the I_{GD}/I_{DS} magnitudes were equal to 1 mA/mm. BV_{GD}/BV_{DS} of samples A-C were determined to be -126/83, -143.5/162, and -311.5/237 V. Excellent improvements of 147%/186% (117%/46%) in BV_{GD}/BV_{DS} have been achieved in the present sample C with respect sample A (B). It is contributed by (1) the enhanced gate insulation by the wide-gap Al_2O_3 gate dielectric, (2) decreased peak electric field modulated by the FP of the Γ-gate design, and (3) effective surface passivation by the composite Al_2O_3/TiO_2 oxides. The microwave power characteristics for the studied devices measured at 2.4 GHz by using a load-pull system with automatic tuners are shown in Fig. 8. Samples A/B/C were biased at V_{GS} = -1.5/-1.5/-1.5 V and V_{DS} = 5/10/10 V, respectively. The output power (P_{out}), associated power gain (G_a), and power-added efficiency (*P.A.E.*) were characterized to be 6.8/9.85/16.5 dBm, 18.4/21.9/23/2 dB, and 16.5%/23.9%/39.9% for samples A/B/C, respectively. Enhanced I_{DS} densities and improved breakdown voltages of the present Γ-gate MOS-HFET design have led to the superior power performances. Fig. 9 shows the noise and the associated gain characteristics for samples A-C measured at 2.4 GHz by using an HP 8970B noise figure meter. Minimum noise figure (NF_{min})/the corresponding gain were determined to be 5.2 dB/5.6 dB, 4.4 dB/7.8 dB, and 3.1 dB/17.1 dB for samples A-C, respectively. Improved noise characteristics of samples C (B) with respect to sample A is mainly attributed to the effective surface passivation by using the composite Al_2O_3/TiO_2 (TiO_2) oxides to reduce trapping/detrapping phenomena as discussed before. Improved NF_{min} performance of sample C as compared to sample B is further contributed by its enhanced g_m performance.

IV. Conclusion

Novel Al_2O_3-dielectric InAlN/AlN/GaN Γ-gate MOS-HFETs with composite Al_2O_3/TiO_2 passivation oxides formed by using USPD and RF sputtering are successfully investigated. TEM photos, EDS, C-V, 1/*f* spectra, and α_H coefficients have been comprehensively characterized for the studied devices. Enhanced gate insulation, effective surface passivation, and reduced gate-drain peak electric field have been achieved in the present design. The devised Γ-gate MOS-HFET has demonstrated superior I_{on}/I_{off} ratio of 8.2×10^{10}, SS of 102.3 mV/dec, $I_{DS,\,max}$ of 868.3 mA/mm, BV_{GD}/BV_{DS} of -311.5/237 V, and *P.A.E.* of 39.9% at 2.4 GHz and 300 K. The present design is promisingly for high-power or power-switching MMIC applications.

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