A Natural ZVS Medium-Power Bidirectional DC–DC Converter With Minimum Number of Devices

Hui Li, *Senior Member, IEEE*, Fang Zheng Peng, *Senior Member, IEEE*, and J. S. Lawler, *Senior Member, IEEE*

***Abstract*—This paper introduces a new bidirectional, isolated dc–dc converter. A typical application for this converter can be found in the auxiliary power supply of hybrid electric vehicles. A dual half-bridge topology has been developed to implement the required power rating using the minimum number of devices. Unified zero-voltage switching was achieved in either direction of power flow with neither a voltage-clamping circuit nor extra switching devices and resonant components. All these new features allow high power density, efficient power conversion, and compact packaging. Complete descriptions of operating principle and design guidelines are provided in this paper. An extended state-space averaged model is developed to predict large- and small-signal characteristics of the converter in either direction of power flow. A 1.6-kW prototype has been built and successfully tested under full power. The experimental results of the converter's steady-state operation confirm the soft-switching operation, simulation analysis, and the developed averaged model. The proposed converter is a good alternative to full-bridge isolated bidirectional dc–dc converter in medium-power applications.**

***Index Terms*—Bidirectional dc–dc converter, half-bridge converter, zero-voltage switching (ZVS).**

I. Introduction

THE necessity of medium-power isolated bidirectional dc–dc converters can be found in wide applications from uninterrupted power supplies, battery charging and discharging systems, to auxiliary power supplies for hybrid electrical vehicles. However, most of the existing dc–dc converters are of low power [1] or unidirectional [2], and cannot meet the requirements of the above applications.

Recently, some medium-/high-power dc–dc converters with soft-switching operation and isolated bidirectional operation have been introduced in the literature [3]–[6]. These converters are regarded as ideal candidates for such applications because they have the advantages of reduced switching losses, improved electromagnetic interference (EMI) and increased efficiency. However, these converters are not appropriate to achieve high power density, high reliability, and low cost because of extra devices and/or complicated control circuitry resulting in bulky and costly implementation.

This paper introduces a new bidirectional, isolated dc–dc converter for medium-power applications. A dual half-bridge topology is developed to achieve higher power rating. In addition, a unified zero-voltage switching (ZVS) is possible in either direction of power flow without using voltage-clamping circuit or extra switching devices and resonant components. Therefore, only the minimum number of devices is required in the proposed topology. Like ZVS phase-shifted full-bridge topologies, the proposed converter has achieved a natural ZVS by only defining the dead time of gate signals. All these features allow efficient power conversion, high power density, low cost, easy control, and compacted packaging. In this paper, the operation of the proposed converter is explained and analyzed. An averaged model is developed and design guidelines are given to select the components of the converter. A 1.6-kW prototype of the converter has been built and successfully tested under full power. The experimental results of the converter's steady-state operation confirm the simulation analysis and the averaged model. The proposed converter is a good alternative to the full-bridge isolated bidirectional dc–dc converter in medium-power applications.

II. Circuit Description and Operation Principles

A. Circuit Description

The proposed bidirectional dc–dc converter is shown in Fig. 1. This circuit is operated with dual half bridges placed on each side of the isolation transformer T_r. When power flows from the low-voltage (LV) side to the high-voltage (HV) side, the circuit works in boost mode to power the HV-side load; otherwise, it works in buck mode to recharge the LV-side battery. A dual half-bridge topology is used instead of a dual full-bridge configuration for the following reasons.

- The total device rating is the same for the dual half-bridge topology and the dual full-bridge topology at the same output power.
- Although the devices of the LV side are subject to twice the dc input voltage, this is an advantage because the dc-input voltage in the anticipated application is 12 V.
- The dual half-bridge topology uses only half as many devices as the full-bridge topology.

B. Principles of Operation

The primary-referred equivalent circuit is shown in Fig. 2. The interval t_1–t_{12} of Fig. 3 describes the various stages of op-

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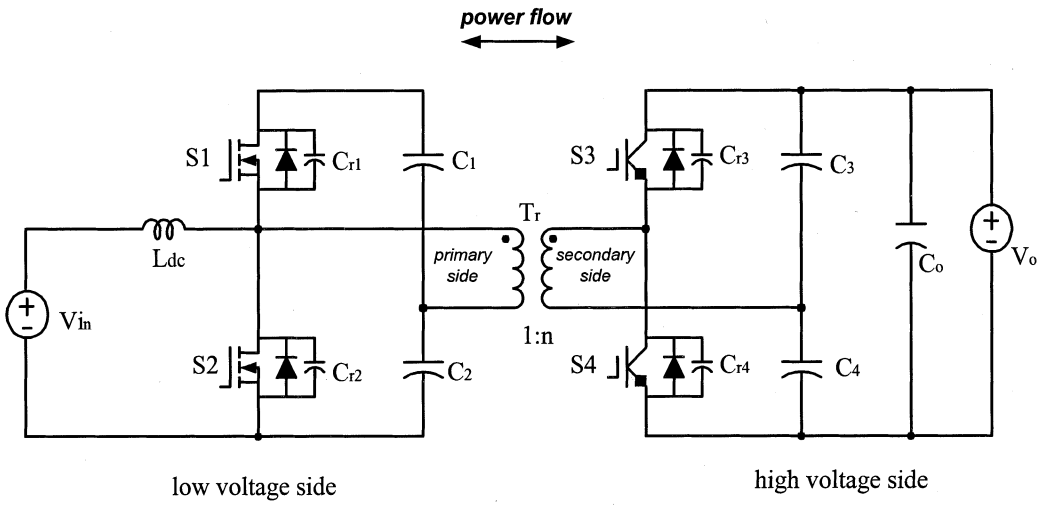


Fig. 1. Soft-switched bidirectional half-bridge dc–dc converter.

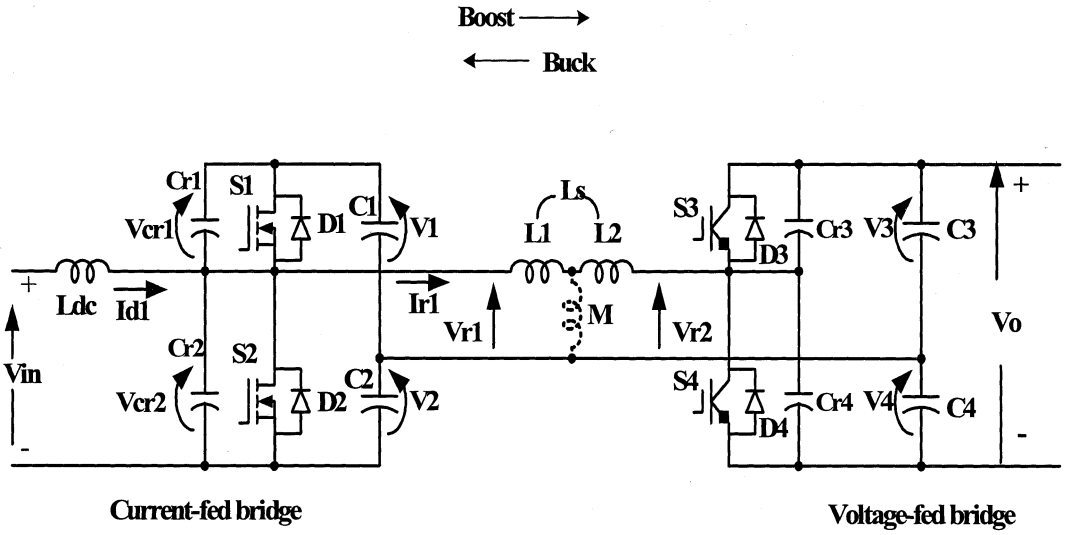


Fig. 2. Primary-referenced equivalent circuit.

eration during one switching period in boost mode. One complete switching cycle is divided into 13 steps. Each step is described briefly below. Commutation procedure in buck mode can be analogously inferred.

Step 1) (before t_1): Circuit steady state. S1 and D3 are conducting.

Step 2) $(t_1 - t_2)$: At t_1, S1 is turned off. C_{r1}, C_{r2} and L_S begin to resonate, making V_{cr2} fall from $V_1 + V_2$. V_{r1} also drops from V_1. The rate of change depends on the magnitude of I_{off}, which is the difference between I_{r1} and I_{d1} at t_1.

Step 3) $(t_2 - t_3)$: At t_2, V_{cr2} attempts to overshoot the negative rail. D2 is therefore forward biased. During this period, S2 can be gated on at zero voltage.

Step 4) $(t_3 - t_4)$: From t_3, I_{r1} is less than I_{d1}, so S2 begins to transfer current from D2. I_{r1} keeps on decreasing until it is equal to 0 at t_4. D3 is thereby still conducting until t_4.

Step 5) $(t_4 - t_5)$: From t_4 to t_5, I_{r1} begins to change polarity and current is commutated from D3 to S3.

Step 6) $(t_5 - t_6)$: At t_5, S3 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged, respectively. The rate of change of the voltage depends on I_{r1} at t_5.

Step 7) $(t_6 - t_7)$: At t_6, when V_{cr4} attempts to overshoot the negative rail, D4 is forward biased. During this period, S4 can be gated on at any time at zero voltage.

Step 8) $(t_7 - t_8)$: At t_7, S2 is gated off. C_{r1}, C_{r2} and L_S begin to resonant again, making V_{cr1} discharge from $V_1 + V_2$. V_{r1} therefore increases from $-V_2$. The rate of change now is decided primarily by the sum of the magnitude of I_{d1} and I_{r1}.

Step 9) $(t_8 - t_9)$: At t_8, when V_{cr1} attempts to overshoot the negative rail, D1 is forward biased. I_{r1} increases until it equals 0 at t_9. During this period, S1 can be gated on at zero voltage.

Step 10) $(t_9 - t_{10})$: From t_9 to t_{10}, I_{r1} begins to change its polarity and continue to increase until it equals I_{d1}. The current is commutated from D4 to S4.

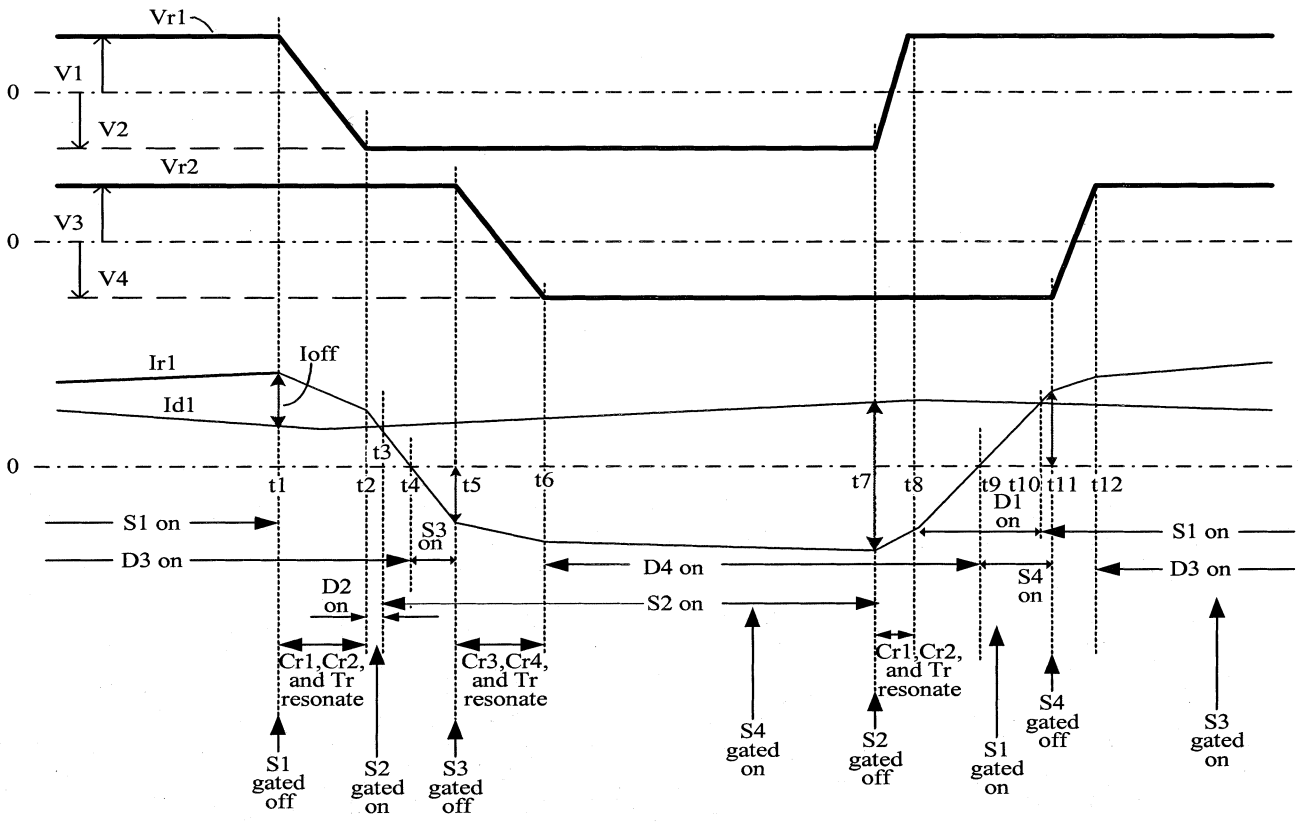


Fig. 3. Waveforms and switching timing of boost mode.

Step 11) $(t_{10} - t_{11})$: From t_{10} to t_{11}, I_{r1} begins to exceed I_{d1}. The current is transferred from D1 to S1.

Step 12) $(t_{11} - t_{12})$: At t_{11}, S4 is gated to turn off. C_{r3} and C_{r4} begin to be charged and discharged again. The charge/discharge rate depends mainly on the magnitude of I_{r1} at t_{11}.

Step 13) $(t_{12} - t_1)$: At t_{12}, when V_{cr3} attempts to overshoot the positive rail, D3 is forward biased. The circuit returns to the original steady state. During this period, S3 can be gated on any time at zero voltage.

Commutation in the proposed circuit is similar to the diode-to-switch commutation mode of the Auxiliary Resonant Commutated Pole Converter (ARCP) converter [7], i.e., turn-off of the main conducting device diverts the current to the corresponding snubber capacitors to charge one and discharge another, resulting in a zero-voltage turn-off. The zero-voltage turn-on is achieved by gating on the incoming device while the antiparallel diode is conducting. However, unlike the ARCP converter, the proposed circuit does not require an auxiliary circuit to achieve soft switching. From Fig. 2, it is clear that the conditions of soft switching in boost mode depend on the magnitude of I_{r1} and I_{d1} at t_1, t_5, t_7, and t_{11}, respectively. This is summarized in (1). The soft-switching conditions in buck mode can be derived similarly

$$\begin{cases} I_{r1}(t_1) > I_{d1}(t_1) \\ I_{r1}(t_5) < 0 \\ I_{r1}(t_7) < I_{d1}(t_7) \\ I_{r1}(t_{11}) > 0. \end{cases} \tag{1}$$

III. Steady-State Analysis

A. Output Characteristics

The analysis of output characteristics is based on the primary-referenced equivalent circuit in Fig. 2 and the idealized waveforms in Fig. 4. The transferred power can be found to be

$$P_o = \frac{\int_0^{T_s} I_{r1} \cdot V_{r1} dt}{T_s} = \frac{\phi_1 \frac{1}{D}\left[4\pi(1-D) - \frac{1}{D}\phi_1\right]}{4\pi\omega L_s} \cdot V_{\text{in}}^2 \tag{2}$$

where T_s is the period of the switching frequency and $D = \phi_2/2\pi$. The output power or output voltage can be regulated by phase-shift angle ϕ_1, duty cycle D, and switching frequency ω. If $D = 50\%$ is assumed and the switching frequency is set at 20 kHz, then the output power equation can be simplified further as

$$P_o = \frac{V_{\text{in}}^2}{\omega L_s} \frac{\phi_1(\pi - \phi_1)}{\pi}. \tag{3}$$

B. Design Equations

According to (3), the output power is related to phase-shift angle and leakage inductance of the transformer when duty cycle and switching frequency are fixed.

Fig. 5 illustrates the output power curves of $L_s = 0.6$ μH and $L_s = 0.3$ μH. It is interesting to notice that if the leakage inductance is selected differently, the phase-shift angle of the same output power is changed. The smaller leakage inductance results in the smaller phase-shift angle. Therefore, the leakage

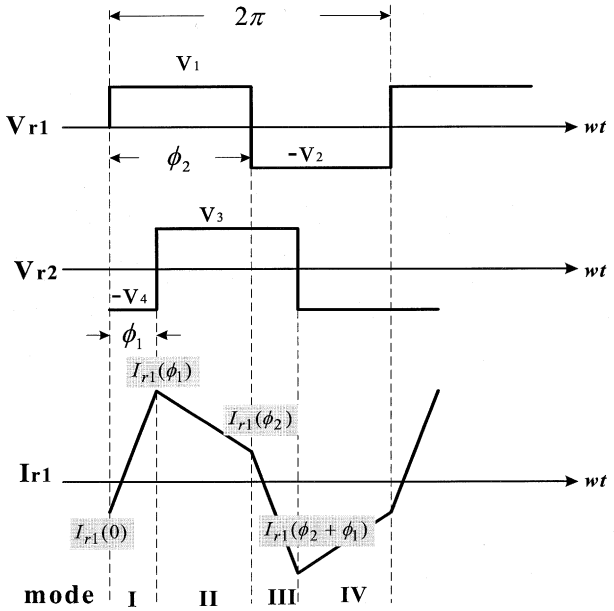


Fig. 4. Idealized voltage and current waveforms of transformer.

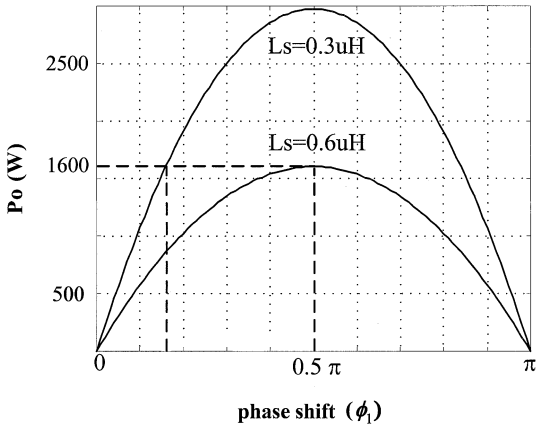


Fig. 5. Output power ϕ_1 and leakage inductance L_s.

inductance of the transformer can be designed according to the expected phase-shift angle at the required power rating.

Assuming that the maximum output power is P_o, the input dc voltage is V_{in}, the switching frequency is ω, the expected phase-shift angle at P_o is ϕ_1, L_s can be calculated as follows:

$$L_s = \frac{V_{\text{in}}^2 \cdot \phi_1 \cdot (\pi - \phi_1)}{P_o \omega \pi}. \tag{4}$$

Referring to Fig. 4, the initial states $I_{r1}(0)$, $I_{r1}(\phi_1)$, $I_{r1}(\phi_2)$, and $I_{r1}(\phi_2 + \phi_1)$ of current I_{r1} during one complete switching cycle can be derived based on the boundary conditions

$$\begin{cases} I_{r1}(0) = -I_{r1}\phi_2 \\ I_{r1}(\phi_1) = -I_{r1}(\phi_2 + \phi_1). \end{cases} \tag{5}$$

When $D = 50\%$ and $\phi_2 = \pi$, the initial conditions of I_{r1} are calculated in (6)

$$\begin{cases} I_{r1}(0) = \frac{V_3 - V_1}{2\omega L_s}(\pi - \phi_1) - \frac{V_1 + V_4}{2\omega L_s}\phi_1 \\ I_{r1}(\phi_1) = \frac{V_1 + V_4}{2\omega L_s}\phi_1 + \frac{V_3 - V_1}{2\omega L_s}(\pi - \phi_1) \\ I_{r1}(\pi) = -I_{r1}(0) \\ I_{r1}(\pi + \phi_1) = -I_{r1}(\phi_1). \end{cases} \tag{6}$$

The average current I_{d1} provided by the power supply can be found to be

$$I_{d1} = \frac{P_o}{V_{\text{in}}}. \tag{7}$$

The device ratings of the LV side can be calculated as

$$\begin{aligned} I_{\text{peak}} &= I_{d1} - I_{r1}(0) \\ V_{\text{peak}} &= 2V_{\text{in}}. \end{aligned} \tag{8}$$

The maximum and minimum voltage change rates happened at $\theta = 0$ and $\theta = \pi$, respectively. The corresponding turn-off currents are calculated as: $I_{\text{off}}|_{\max,\theta=0} = |I_{r1}(0)| + |I_{d1}|$ and $I_{\text{off}}|_{\min,\theta=\pi} = |I_{r1}(\pi)| - |I_{d1}|$. Assuming snubber capacitors are selected as 1 μF, $I_{\text{off}} = C_{r1} \cdot dv/dt$, the range of dv/dt is derived as

$$C_{r1} I_{\text{off}}|_{\min} \le \frac{dv}{dt} \le C_{r1} I_{\text{off}}|_{\max}. \tag{9}$$

If ΔI of I_{d1} is selected as 12 A, then L_{dc} is designed to be

$$L_{\text{dc}} = \frac{V_{\text{in}} \cdot \Delta t}{\Delta I}. \tag{10}$$

Finally, the soft-switching condition will be verified in (11)

$$\text{boost} \begin{cases} I_{r1}(0) - I_{d1} < 0 \\ I_{r1}(\phi_1) > 0 \\ I_{r1}(\pi) - I_{d1} > 0 \\ I_{r1}(\pi + \phi_1) < 0 \end{cases} \text{and buck} \begin{cases} I_{r1}(0) > 0 \\ I_{d1} > I_{r1}(\phi_1) \\ I_{r1}(\pi) < 0 \\ I_{r1}(\pi + \phi_1) > I_{d1}. \end{cases} \tag{11}$$

C. Characteristic Curves

The characteristic curves are derived based on the design equations. Figs. 6–8 describe the system behavior when transformer leakage inductance is selected as 0.6 μH.

Fig. 6(a)–(d) plots the input current, transformer current, dv/dt (max), and dv/dt (min) over the full output power range. The purpose of these figures is to show that the soft-switching conditions are satisfied during the whole operating range. According to (11), soft switching is maintained at any output power in the boost mode. Soft switching of the buck mode can be similarly inferred.

Fig. 7 shows the current stress of the main switches of the LV side and the HV side versus output power. The current stress of the HV side is calculated based on the primary-referenced circuit. Fig. 8 plots the current stress as a function of phase shift ϕ_1 instead of output power.

An interesting feature can be brought to light by examining Fig. 8, which shows that the current stresses of the devices are proportional to the phase-shift angle. As a result, if the phase shift is decreased for the same output power, the current stress

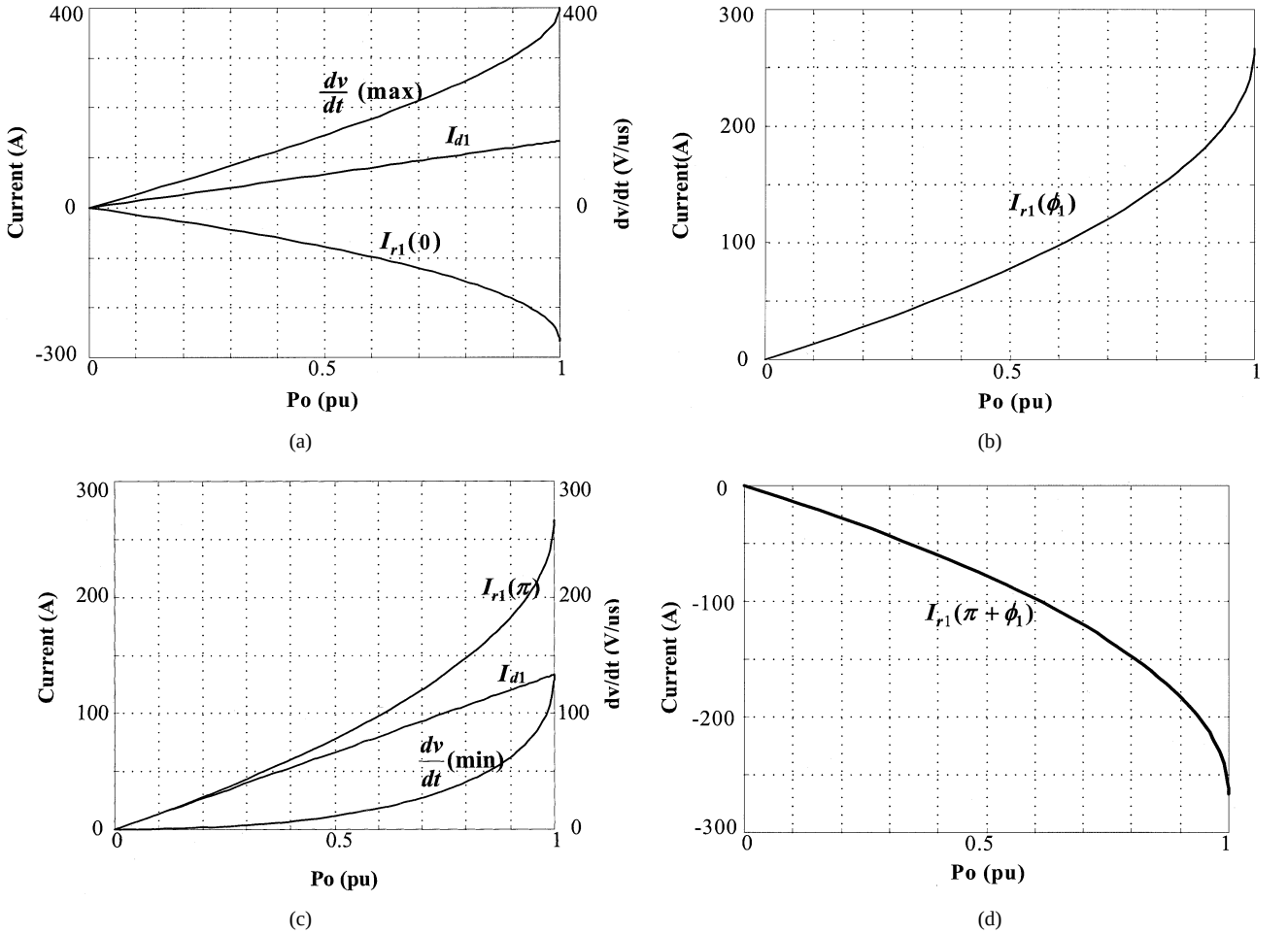


Fig. 6. Soft-switching conditions versus output power when $L_s = 0.6\ \mu$H. (a) I_{d1}, $I_{r1}(0)$, $dv/dt\ (max)$ versus output power. (b) $I_{r1}(\phi_1)$ versus output power. (c) I_{d1}, $I_{r1}\ (\pi)$, $dv/dt\ (min)$ versus output power. (d) $I_{r1}\ (\pi + \phi_1)$ versus output power.

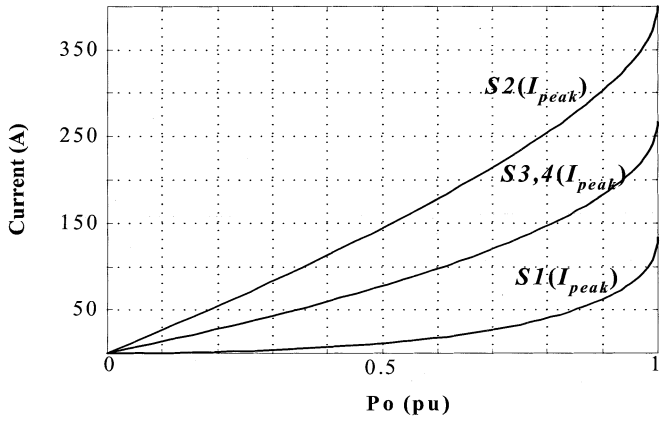


Fig. 7. Current stresses of devices versus output power.

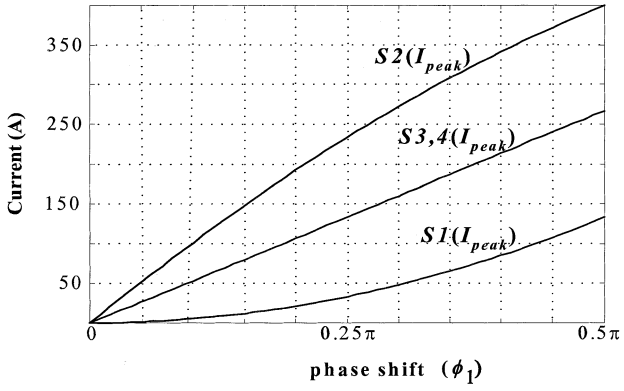


Fig. 8. Current stresses of devices versus phase shift ϕ_1.

becomes less. This is important to improve the system efficiency because the conduction loss will become the main loss for soft-switching converters.

IV. Modeling and Control System Design

In this section, the development of the averaged model and control system design is provided for the proposed converter. The traditional state-space averaging technique [8] and circuit-

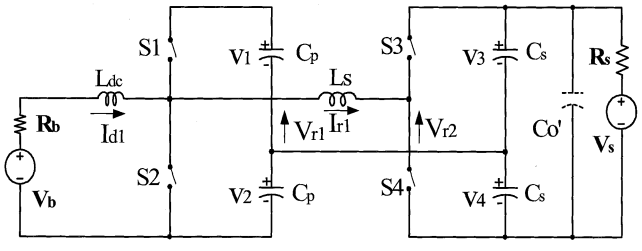


Fig. 9. Primary-referenced equivalent circuit.

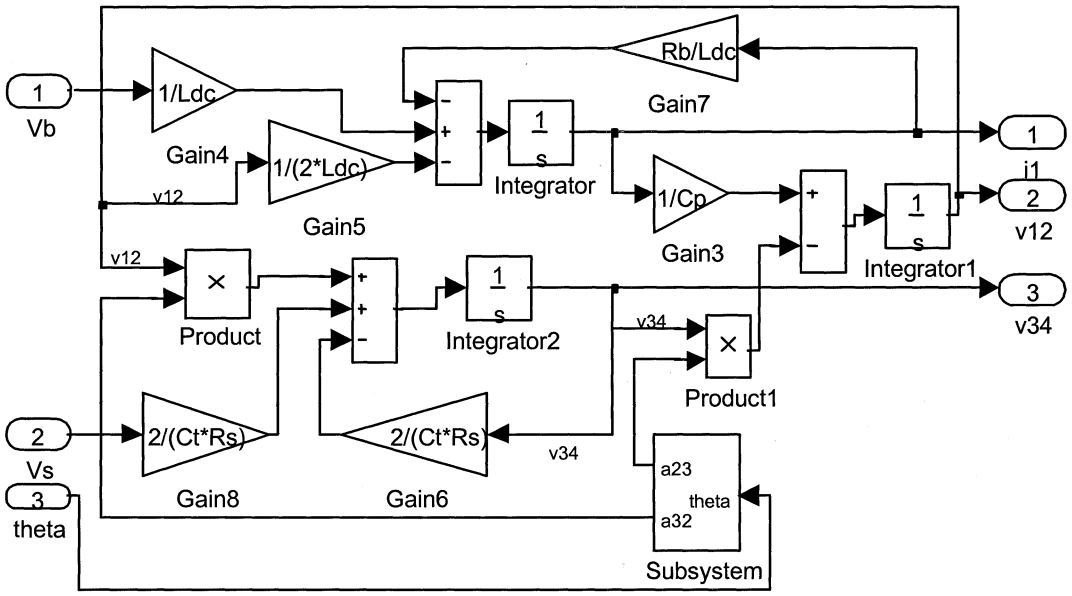


Fig. 10. Matlab/Simulink simulation block diagram of average model.

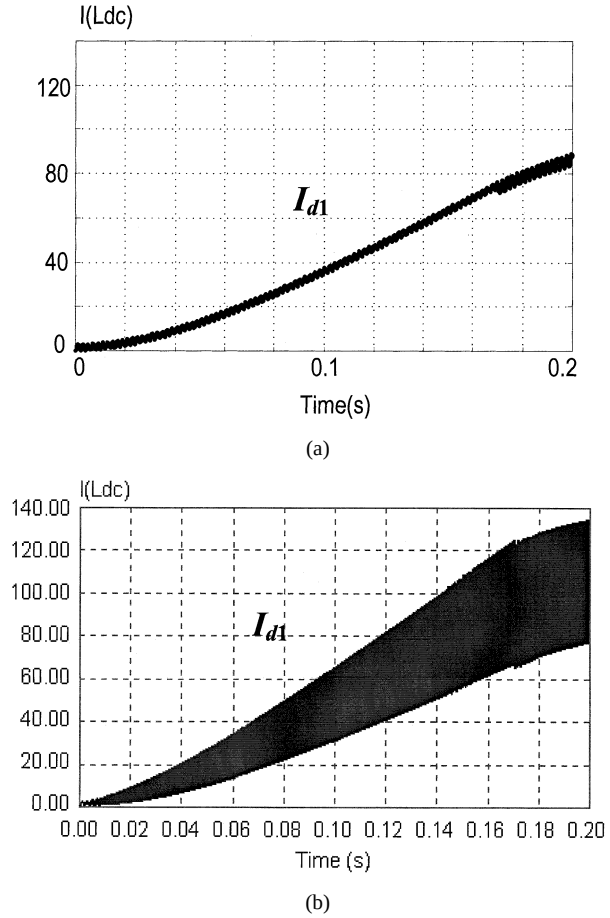


Fig. 11. Simulation and comparison of I_{d1} in boost mode. (a) I_{d1} of average model. (b) I_{d1} of detailed circuit simulation.

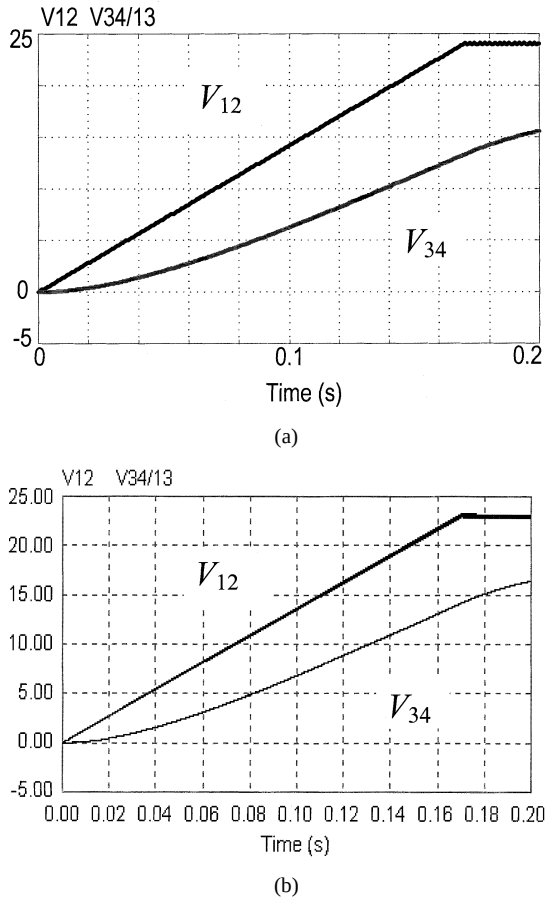
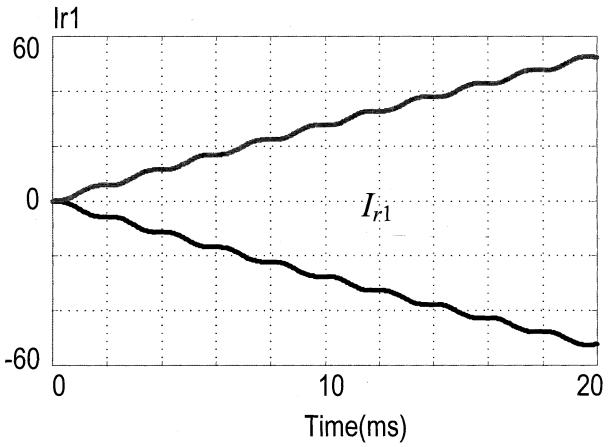
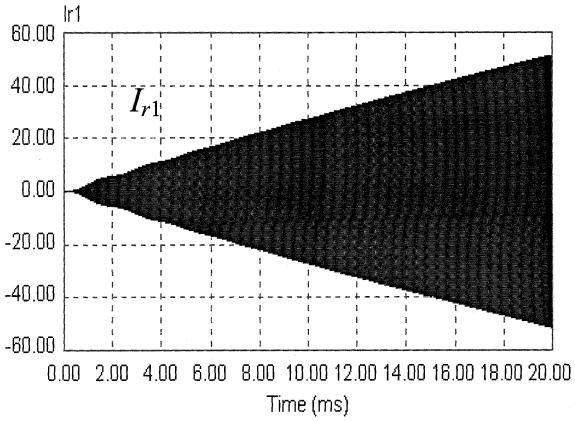


Fig. 12. Simulation and comparison of V_{12} and V_{34} in boost mode. (a) V_{12} and V_{34} of average model. (b) V_{12} and V_{34} of detailed circuit simulation.

averaged approach [9] are difficult to be applied to the circuit. Therefore, a switching-frequency-dependent average model and a linearized small-signal model have been derived to predict large- and small-signal characteristics of the converter in both directions of power flow. The simulated waveforms of the average model have been compared with the detailed circuit simulation to verify the accuracy of the modeling. The experimental verifications will be illustrated in Section V. The control-to-output transfer function has been generated to provide the information on the poles, zeros, and the gain of



(a)



(b)

Fig. 13. Simulation and comparison of envelope of I_{r1} in boost mode. (a) Envelope of I_{r1} of average model simulation. (b) Envelope of I_{r1} of detailed circuit simulation.

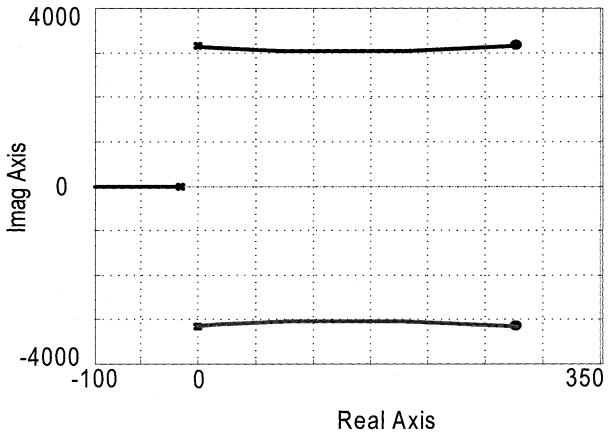


Fig. 14. Root locus plot of $T_2(s)$ of the uncompensated system.

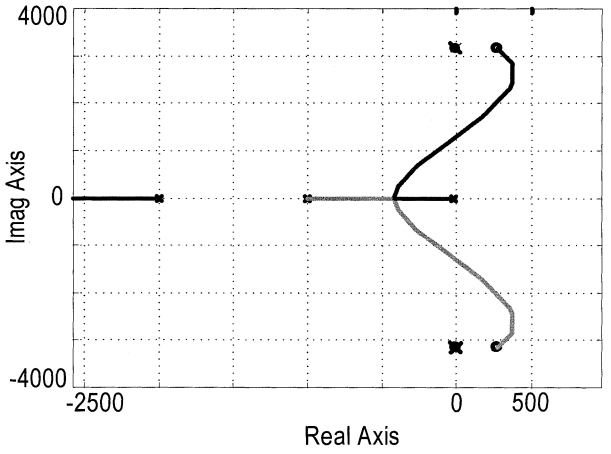


Fig. 15. Root locus of the compensated system.

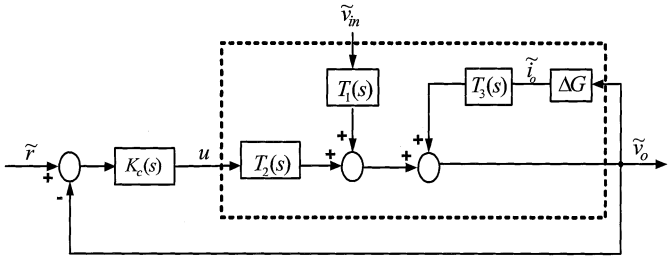


Fig. 16. Closed-loop model of small-signal control system.

the open-loop converter. The controller has been designed to stabilize the system around the nominal operating point and regulate the output voltage against dc input voltage disturbance and/or load variation. The control system is simulated by Matlab/Simulink. The system transient performance is verified by the simulated model.

A. Averaged Model

Assuming that duty cycle equals 50% and the switching processes are instantaneous, the primary-referenced equivalent circuit is redrawn in Fig. 9. The operation modes of one switching cycle at steady state are shown in Fig. 4. The dynamic variables of the converter are chosen to be the inductor current I_{d1}, the transformer current I_{r1}, and the capacitor voltages V_1, V_2, V_3, and V_4. I_{r1} is the ac current flowing through the isolation transformer T_r, so the dc average over each switching cycle is zero. As a result, the key problem of developing the average model for this converter is to exclude I_{r1}, which is possible because I_{r1} can be represented by $I_{r1} = f\ (V_1, V_2, V_3, V_4)$, using circuit analysis of the four modes of operation. However, it is hard to cancel I_{r1} using the ordinary state-space averaging technique. In addition, the conventional averaging techniques are independent of switching frequency. This will not be acceptable for the proposed converter because the switching frequency is a possible control variable. Thus, an extended switching-frequency-dependent averaging technique is applied to solve these problems. The details of the model derivation can be found in [10] and the simplified average model in either direction of power flow can be expressed in (12)

$$\begin{cases} \frac{d(I_{d1\text{avg}})}{dt} = -\frac{R_b}{L_{\text{dc}}} I_{d1\text{avg}} - \frac{1}{2L_{\text{dc}}} V_{12\text{avg}} + \frac{1}{L_{\text{dc}}} V_b \\ \frac{d(V_{12\text{avg}})}{dt} = \frac{1}{C_p} I_{d1\text{avg}} - \frac{2\phi_1(\pi-\phi_1)}{C_p T_s \omega \cdot 2\omega L_s} V_{34\text{avg}} \\ \frac{d(V_{34\text{avg}})}{dt} = \frac{2\phi_1(\pi-\phi_1)}{C_t T_s \omega \cdot 2\omega L_s} V_{12\text{avg}} - \frac{2}{C_t R_s} V_{34\text{avg}} + \frac{2}{C_t R_s} V_s \end{cases} \tag{12}$$

where $C_t = C_s + 2C_o'$, $Cp = C_1 = C_2$, $C_s = C_3 = C_4$, $V_{12} = V_1 + V_2$, and $V_{34} = V_3 + V_4$.

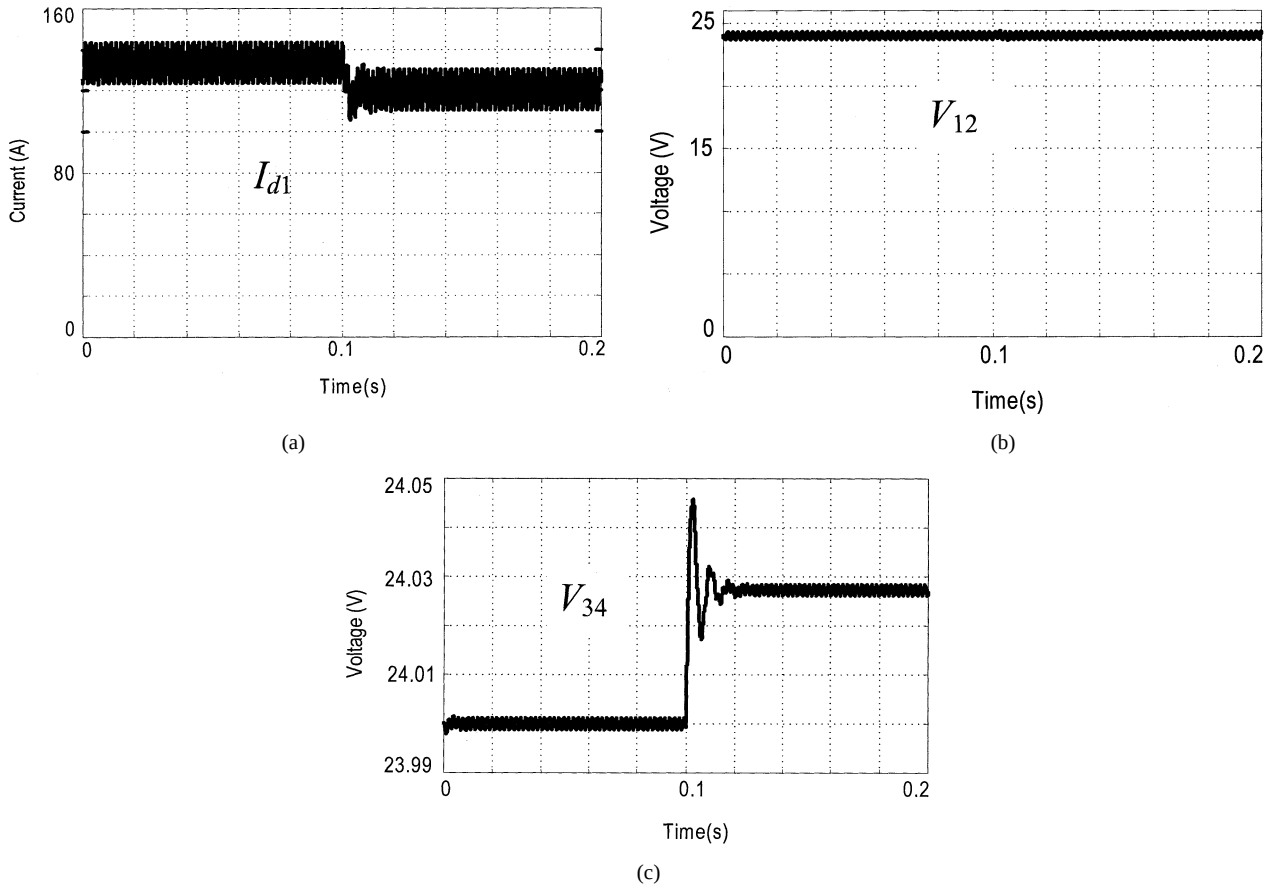


Fig. 17. System response of load step change from 0.36 Ω to 0.4 Ω. (a) I_{d1} response of load step change. (b) V_{12} response of load step change. (c) V_{34} response of load step change.

B. Simulation and Experimental Verification of Averaged Model

The average model can be implemented and simulated using Matlab/Simulink, which is shown in Fig. 10.

A startup process of the open-loop converter system using a ramp input voltage of 12 V is simulated under the conditions below

$$R_b = 0,\ D = 50\%,\ f_s = 20\,\text{kHz},\ L_{\text{dc}} = 5\,\mu\text{H},\ L_s = 0.3\,\mu\text{H},$$
$$C_p = C_s = 10\,\text{mF},\ C_o' = 169\,\text{mF},\ V_s = 0\,\text{V},\ \text{and}\ R_s = 0.27\,\Omega.$$

The waveforms for averaged I_{d1}, V_{12}, and V_{34} of the average model and detailed circuit model are shown in Figs. 11 and 12, respectively. The verification of the ac variable simulation is demonstrated in Fig. 13. The comparison demonstrates their similarity consistence in shape, frequency, and average magnitude.

C. Control System Design and Simulation

By introducing small perturbations: $v_{\text{in}} = V_{\text{in}} + \tilde{v}_{\text{in}}$, $\phi_1 = \Phi_1 + \tilde{\phi}_1$, $i_o = 0 + \tilde{i}_o$, $V_{12\text{avg}} = V_{12} + \tilde{v}_{12}$, $V_{34\text{avg}} = V_{34} + \tilde{v}_{34}$, and $I_{d1\text{avg}} = I_{d1} + \tilde{i}_1$, where i_o is a current source placed across the nominal load, and choosing ($\tilde{i}_1$, $\tilde{v}_{12}$, and $\tilde{v}_{34}$) as state variables, ($\tilde{v}_{\text{in}}$, $\tilde{\phi}_1$, $\tilde{i}_o$) as control inputs and $\tilde{v}_{34}$ as controlled output, the linearized state equations can be derived as follows:

$$\begin{cases} \begin{bmatrix} \dot{\tilde{i}}_1 \\ \dot{\tilde{v}}_{12} \\ \dot{\tilde{v}}_{34} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{2L_{\text{dc}}} & 0 \\ \frac{1}{C_p} & 0 & \frac{-2\Phi_1(\pi-\Phi_1)}{K1} \\ 0 & \frac{2\Phi_1(\pi-\Phi_1)}{K3} & \frac{-2}{C_i R} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_{12}\tilde{v}_{34} \end{bmatrix} \\ \qquad + \begin{bmatrix} \frac{1}{Ldc} & 0 & 0 \\ 0 & \frac{-2(\pi-2\Phi_1)\cdot V_{34}}{K1} & 0 \\ 0 & \frac{2(\pi-2\Phi_1)\cdot 2V_{\text{in}}}{K2} & \frac{-2}{C_i} \end{bmatrix} \begin{bmatrix} \tilde{v}_{\text{in}} \\ \tilde{\phi}_1 \\ \tilde{i}_o \end{bmatrix} \\ \tilde{v}_o = [0 \quad 0 \quad 1][\tilde{i}_1 \quad \tilde{v}_{12} \quad \tilde{v}_{34}]^T \end{cases} \tag{13}$$

where $K1 = 2T_s\omega^2 L_s C_p$, and $K2 = 2T_s\omega^2 L_s C_o{}'$.

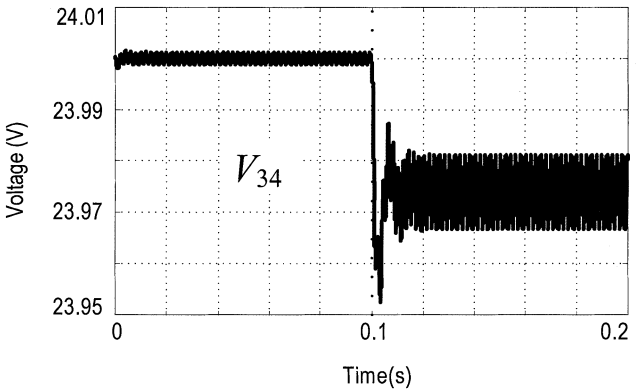


Fig. 18. Output response of input voltage step change from 12 to 11 V.

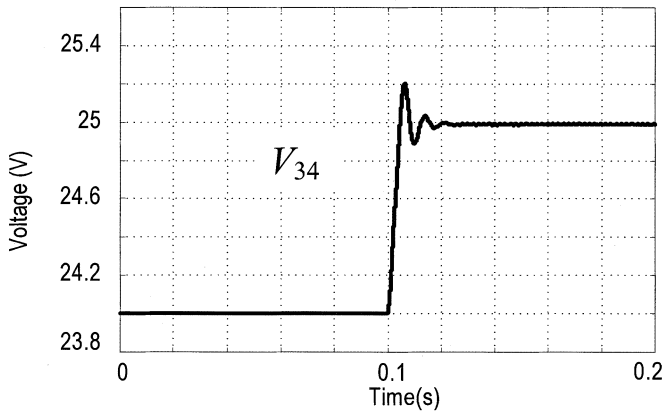


Fig. 19. Output response when reference voltage change from 24 V to 25 V.

Assume the nominal operating point of the dc–dc converter is selected as

$$P_o = 1.6\ \text{kW},\ V_{\text{in}} = 12\ \text{V}\ \Phi_1 = 0.16\,\pi,\ R_s = 0.36\ \Omega,$$
$$L_{\text{dc}} = 5\ \mu\text{H},\ C_p = C_s = 10\ \text{mF},\ C_o' = 169\ \text{mF},\ f_s = 20\ \text{kHz}.$$

L_s is designed as 0.3 μH to have smaller conduction loss at 1.6 kW. The transfer function matrix from input vector to output is calculated as follows:

$$\begin{aligned} T_1(s) &= \frac{\tilde{\nu}_o(s)}{\tilde{\nu}_{\text{in}}(s)} \\ &= \frac{0.319\times 10^9}{s^3 + 15.964s^2 + 0.100\times 10^8 s + 0.159\times 10^9} \\ T_2(s) &= \frac{\tilde{\nu}_o(s)}{\tilde{\phi}_1(s)} \\ &= \frac{617.048s^2 - 0.343\times 10^6 s + 0.617\times 10^{10}}{s^3 + 15.964s^2 + 0.100\times 10^8 s + 0.159\times 10^9} \\ T_3(s) &= \frac{\tilde{\nu}_o(s)}{\tilde{i}_o(s)} \\ &= \frac{-15.964s^2 - 0.159\times 10^9}{s^3 + 15.964s^2 + 0.100\times 10^8 s + 0.159\times 10^9}. \end{aligned} \quad (14)$$

The transfer functions are used to design the controller to allow the converter to meet load regulation and transient response specifications, especially the control-to-output transfer function $T_2\ (s)$. The root locus plot of $T_2\ (s)$ is shown in Fig. 14. The root locus of the compensated system is shown in Fig. 15, in which a controller is obtained by trial and error as shown in (15)

$$K_c(s) = \frac{K(s + 0.008 + 3160i)(s + 0.008 - 3160i)}{(s + 1000)(s + 2000)}. \quad (15)$$

The block diagram of the control system is shown schematically in Fig. 16. To estimate the system performance, a simulation model of the control system was established using Matlab/Simulink. The simulation results are shown in Figs. 17–19.

V. Experimental and Simulation Verification

A 1.6-kW soft-switched bidirectional dc–dc converter has been built and experimentally tested to validate the previous analysis. The prototype is pictured in Fig. 20. In order to compare with the size of a dual full-bridge converter for the similar application, the prototype is laid on a ″ liquid-cooled heat sink with overall size of about 7.5 in width and 13.5 in length. The actual usable area is 7.25 in × 8.5 in, which shows the high-power-density characteristic of the proposed topology.

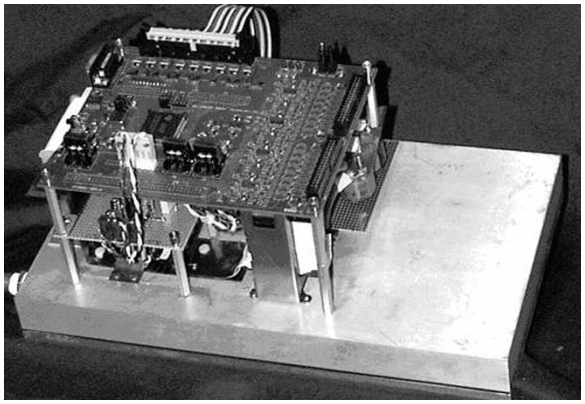
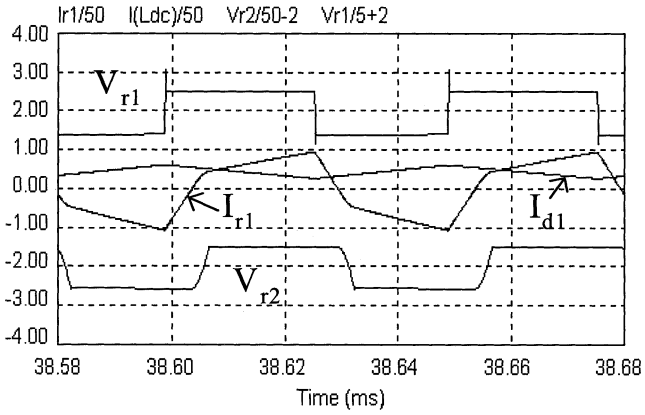
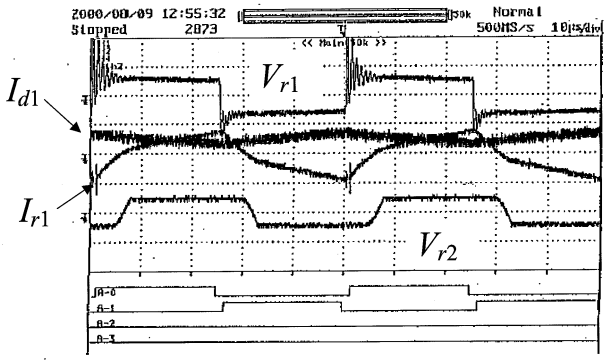


Fig. 20. Photograph of the prototype.



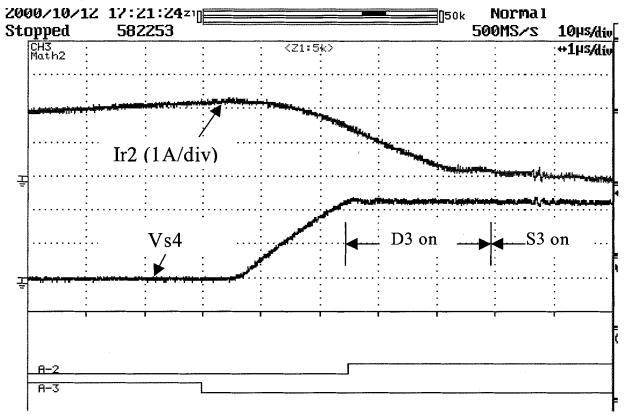
(a)



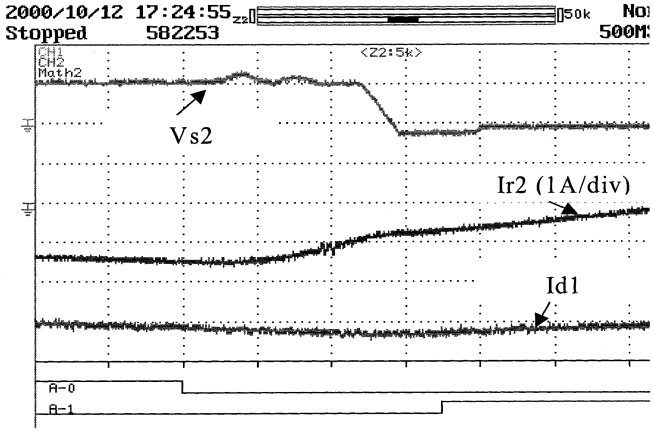
(b)

Fig. 21. Steady-state operation of boost mode ($V_{\text{in}} = 3$ V). (a) Simulation results of V_{r1} (5V/div), I_{d1} (50A/div), I_{r1} (50A/div), and V_{r2} (50V/div). (b) Experimental results of V_{r1}(5V/div), I_{d1} (50A/div), I_{r1}(50A/div), and V_{r2}(50V/div).

The experimental results and circuit simulation results of static performance in boost mode are obtained in Fig. 21. There is a good agreement between simulation results and experimental results. For inductor current I_{d1} and transformer current I_{r1} the wave shapes of simulation and those of experiment



(a)



(b)

Fig. 22. Steady-state operation of buck mode ($v_s = 116$ V). (a) Zero-voltage turn-off of S4 in buck mode. (b) Zero voltage turn-on of S2 in buck mode.

agree with each other. In addition, the peak values of I_{r1} in simulation are $+45$ A and -55 A and those of the experimental values are $+40$ A and -50 A. The average value of I_{d1} in Fig. 21(a) is about 22 A and that of Fig. 21(b) is 25 A. The magnitude of V_{r2} in simulation is 26 V; the experimental magnitude is also about 26 V. In addition, there are also similarities in shape and frequency of V_{r2}. The phase-shift angles between V_{r1} and V_{r2} in the two figures are consistent. Although the magnitude and the shape of V_{r1} are almost the same in the two figures, the experimental result of V_{r1} waveform has a ringing effect. This is because it is hard to measure directly the two terminals of the primary side of the transformer; consequently the measurement loop may be the main reason for this ringing effect. The details of the switching process of S2 and S4 in buck mode are demonstrated in Fig. 22. The voltage source of the HV side is 116 V. The load resistance of the LV side is 0.1 Ω. The phase-shift angle of S3 leading to S1 is 0.04π, namely, 1 μs under 20-kHz switching frequency. The leakage inductance of the transformer in this prototype is measured as 0.4 μH. The soft switching of other devices can be derived symmetrically.

Fig. 23 presents the output characteristics of the converter from 0 to full output power under open-loop control. As indicated in the figure, the "*" trace is the experimental result, the "o" one is of detailed circuit simulation and the "+" one is of average model simulation. The similarity of the three curves con-

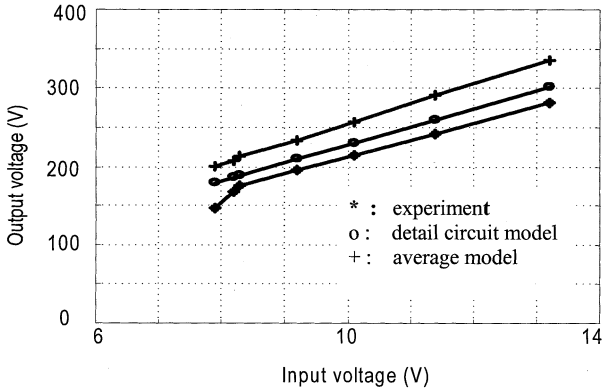


Fig. 23. Output characteristics comparison.

firms the validity of the average model. The difference between the average model, detailed circuit model and prototype can be explained as follows. The average model assumes all switches and components are ideal, there are no losses in switches, capacitors, the inductor or the transformer. The detailed circuit model is a better approximation of the actual circuit. Some of the above losses have been taken into account and the efficiency will be lower than that of average model. The difference between the circuit model and the prototype is likely in the higher device losses and magnetic losses in the prototype due to the imperfect devices and transformer models in detailed circuit simulation. Thereby, the output voltage of average model is higher than that of the detailed circuit model and the detailed circuit model voltage is higher than the prototype.

VI. Summary

This paper has presented a new soft-switched bidirectional dc–dc converter. Compared with other soft-switched bi directional dc–dc converters, this new topology has the following features.

- *Decreased number of devices*—Compared with the full-bridge topologies, this converter has a half bridge on both the LV side and the HV side, decreasing the number of devices by half.
- *Unified soft-switching scheme without an auxiliary circuit*—Unified ZVS is possible for all of the devices in either direction of power flow. Moreover, instead of using an auxiliary circuit, soft-switching conditions are ensured by (11).
- *Low-cost design is lightweight, compact, and reliable.*
- *The design has less control and accessory power needs than converters for the similar applications.*

In addition, a large-signal mathematical model and its linearized small-signal model were developed and verified for the proposed circuit. Moreover, a controller has been designed and the simulation results show the converter system has a satisfactory transient response against load variation and disturbed battery voltage. The averaging technique proposed in this paper also provides a possible solution to the other bidirectional dc–dc converters with a high-frequency isolation transformer. The experimental waveforms confirm the averaged model, soft-switching operation, and good steady-state performance of the converter.

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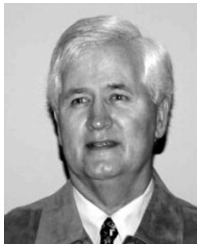

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