Experiences with OpenMP, PGI, HMPP and OpenACC directives on ISO/TTI kernels

Sayan Ghosh [1] Terrence Liao [2] Henri Calandra [2]
Barbara M. Chapman [1]

[1]University of Houston

[2]Total

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Sections

Accelerator directives, testbed and test kernels

Optimizations using accelerator directives and compiler options

Analysis of various CPU/GPU versions of ISO/TTI kernels

Re-evaluation of the directives

Why Accelerator Directives?

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- Improves code maintainability/portability

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- Compiler translates pragma embedded user code (and **optimizes**), according to the specified target hardware

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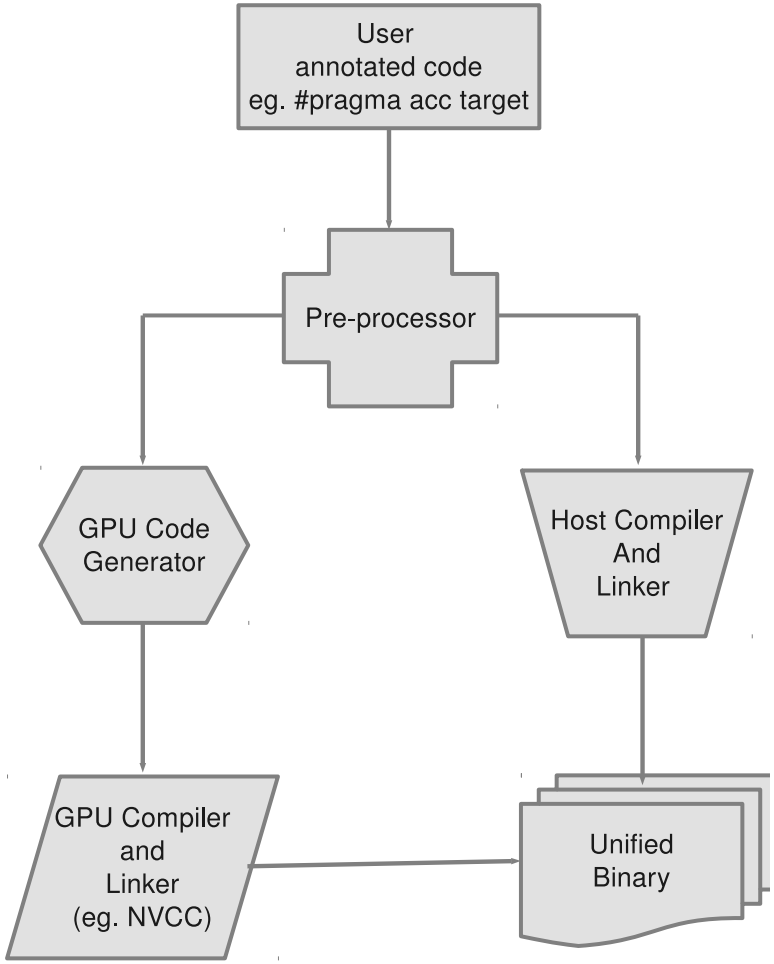

Compilation and code generation process of a high level GPU directive based model

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All of them could be merged into a single statement, of course

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$$\frac{\partial^2 p}{\partial t^2} = v_{px}^2 H_2 p + \alpha v_{pz}^2 H_1 q + v_{sz}^2 H_1 (p - \alpha q)$$

$$\frac{\partial^2 q}{\partial t^2} = \frac{v_{px}^2 H_2 p}{\alpha} + v_{pz}^2 H_1 q + v_{sz}^2 H_1 (\frac{1}{\alpha} p - q)$$

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Evaluation platform

Platform	Facets
CPU	Intel Xeon E5640 @ 2.67 GHz, 8 CPU cores, 12 MB L3 Cache, 96 GB Memory, 16X PCIe2 bus - ideal bandwidth: 8 GB/sec
GPU	Nvidia Tesla M2090, Registers per thread: 63, 512 Compute cores, 6 GB GDDR5 Memory, ECC: disabled
Compilers	Intel Compiler 12.1.5, CAPS HMPP Workbench 3.2.1, PGI Compiler 12.3 / 12.6, Nvidia CUDA 4.0 / 4.2
API	OpenMP 3.1, OpenACC 1.0, PGI Accelerator Model v1.3

ISO/TTI kernels are written in FORTRAN language

CAPS HMPP directives

- A *Codelet* signifies a region where the function to be ported to the hardware accelerator is declared
- A *Callsite* refers to the place in the program where the function is called

HMPP **Codelet** and Callsite

```
!$HMPP fdtd CODELET, TARGET=CUDA, ARGS[V;U].MIRROR, &
...
!$HMPPCG GRIDIFY (j*i,k), BLOCKSIZE 64X8, PRIVATE(a,b,c)
  do k=k0,k1
   do j=j0,j1
    do i=i0,i1
```

HMPP Codelet and **Callsite**

```
!$HMPP fdtd ALLOCATE, DATA["in";"out"], &
...
!$HMPP fdtd ADVANCEDLOAD, DATA["in";"out"]
!$HMPP fdtd CALLSITE
CALL FDTD_base (in, out, dx, dy, dz,
           c[0], c[1], c[2], c[3], c[4]);
...
!$HMPP fdtd DELEGATEDSTORE, DATA["out"]
```

PGI Accelerator directives

The data region - `!$acc data region` encapsulates the accelerator compute region (or kernel) - `$acc region`

```
!$ACC DATA REGION COPY(V,U) COPYIN(c)
!$ACC REGION
!$ACC DO PARALLEL(64) PRIVATE(a,b)
do k=k0,k1
 !$ACC DO PARALLEL(4)
 do j=j0,j1
  !$ACC DO VECTOR(128)
  do i=i0,i1
```

OpenACC directives

- For `!$acc kernels`, the compiler would break a tight loop-nest into a sequence of kernels
- The `!$acc parallel` directive is like `!$omp parallel`, and it generates one kernel
- Expresses concurrency in terms of gangs (*blocks*) of workers (*warp*) of vectors (*threads*)

```
!$ACC DATA COPY(p0,p1)  &
!$ACC COPYIN(c)
!$ACC KERNELS           &
!$ACC PRESENT(p0,p1,c)
!$ACC LOOP INDEPENDENT
do k=k0,k1
 !$ACC LOOP INDEPENDENT
 do j=j0,j1
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Optimizations performed

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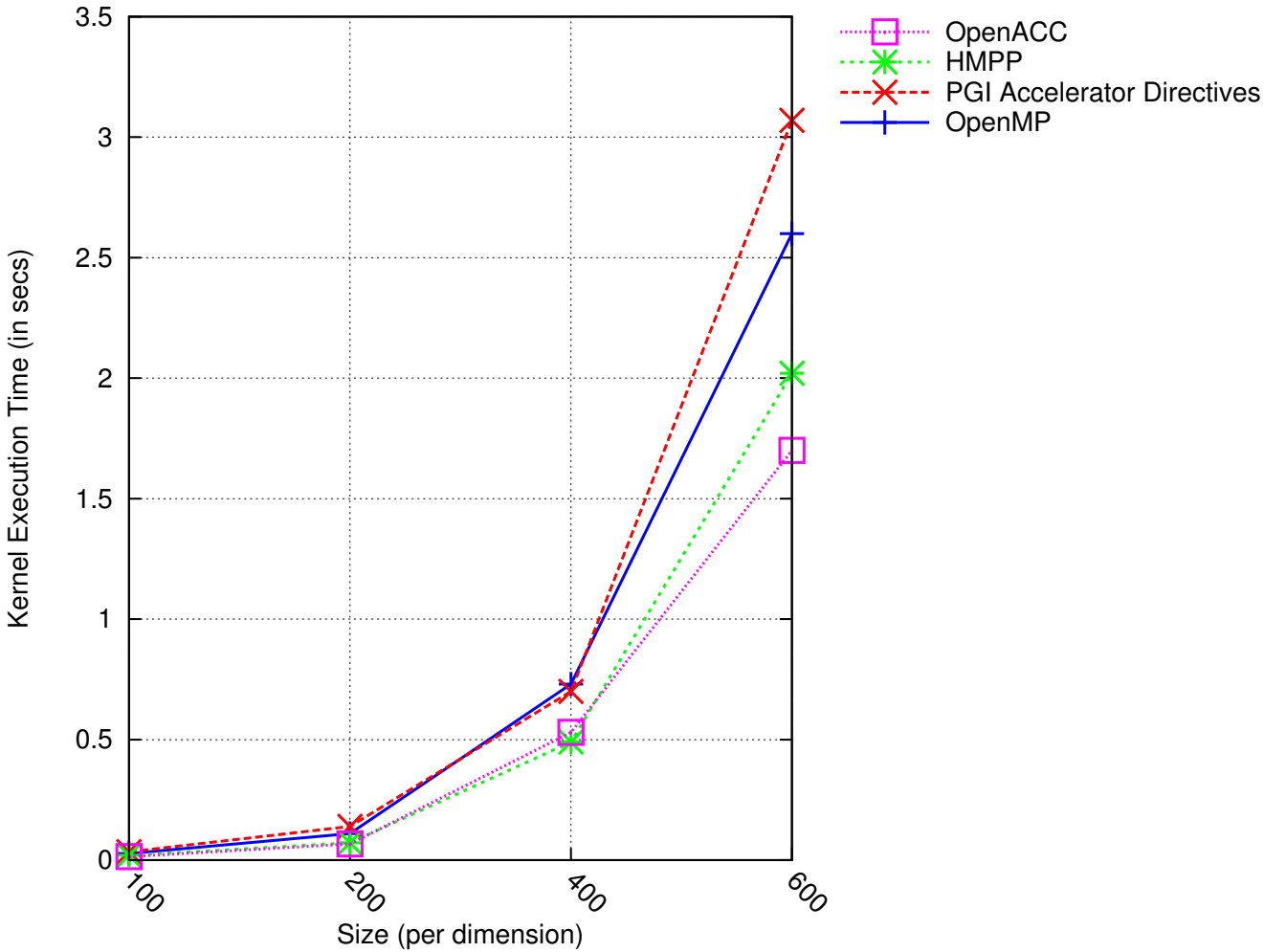
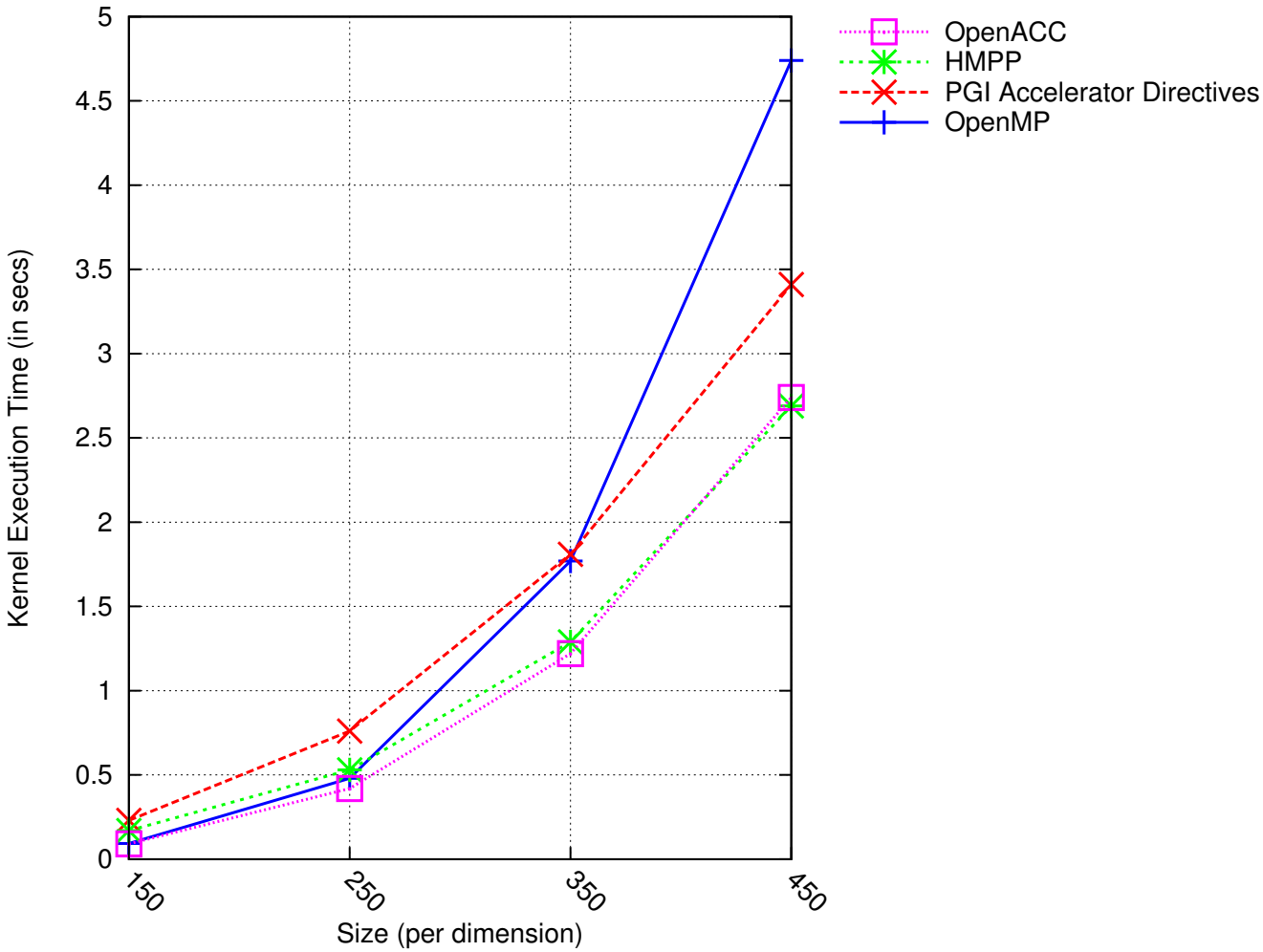
- Asynchronous computation and Data transfers - Current/Past GPUs have two copy engines and one kernel engine

Quick peek at the final results - ISO



Different implementations of ISO using directive-based approaches

Quick peek at the final results - TTI



Different implementations of TTI using directive-based approaches

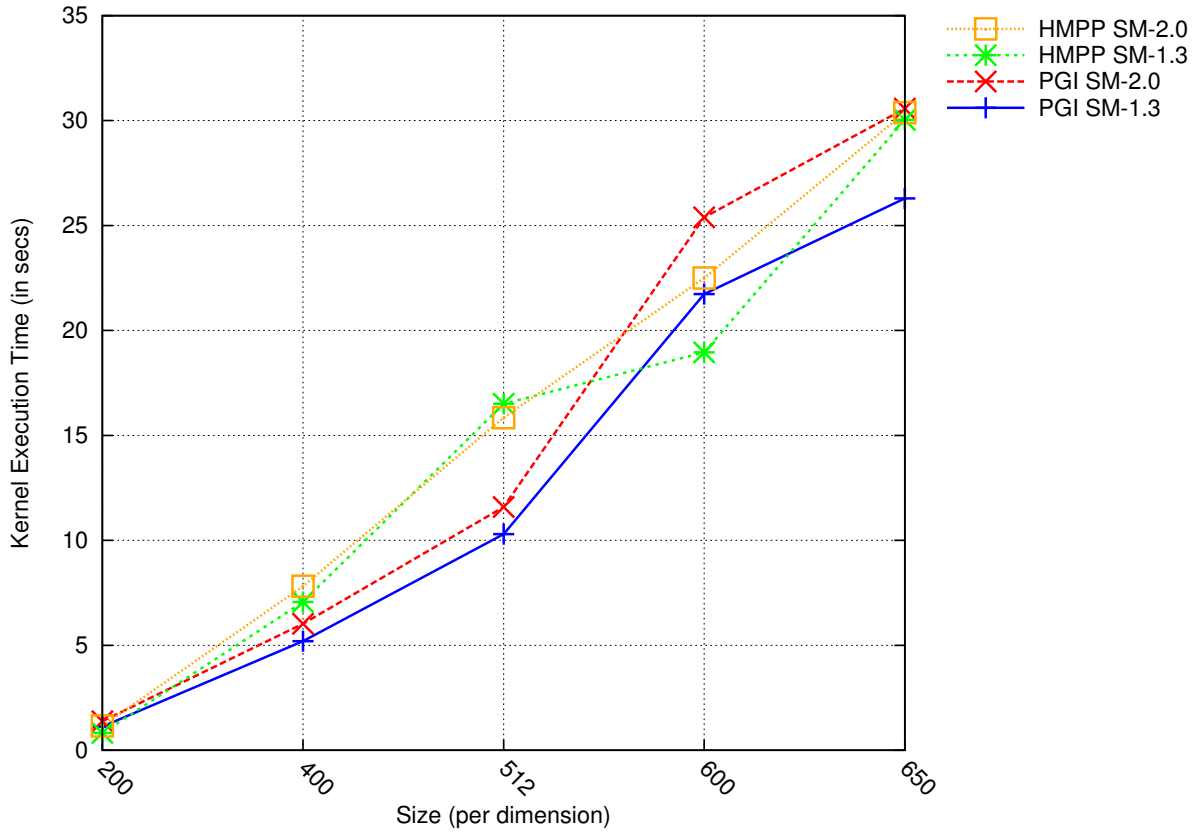
GPU acceleration factor compared to CPU implementation

Acceleration of TTI and ISO kernels compared with directive based approaches on a GPU against multi-threaded OpenMP cache-blocked implementation on an 8-core SMP

Accelerator Directives / Kernels	**ISO**	**TTI**
CAPS HMPP	1.29	1.76
PGI Accelerator	0.85	1.39
OpenACC	1.54	1.73

Differences in compute device 1.3 and 2.0

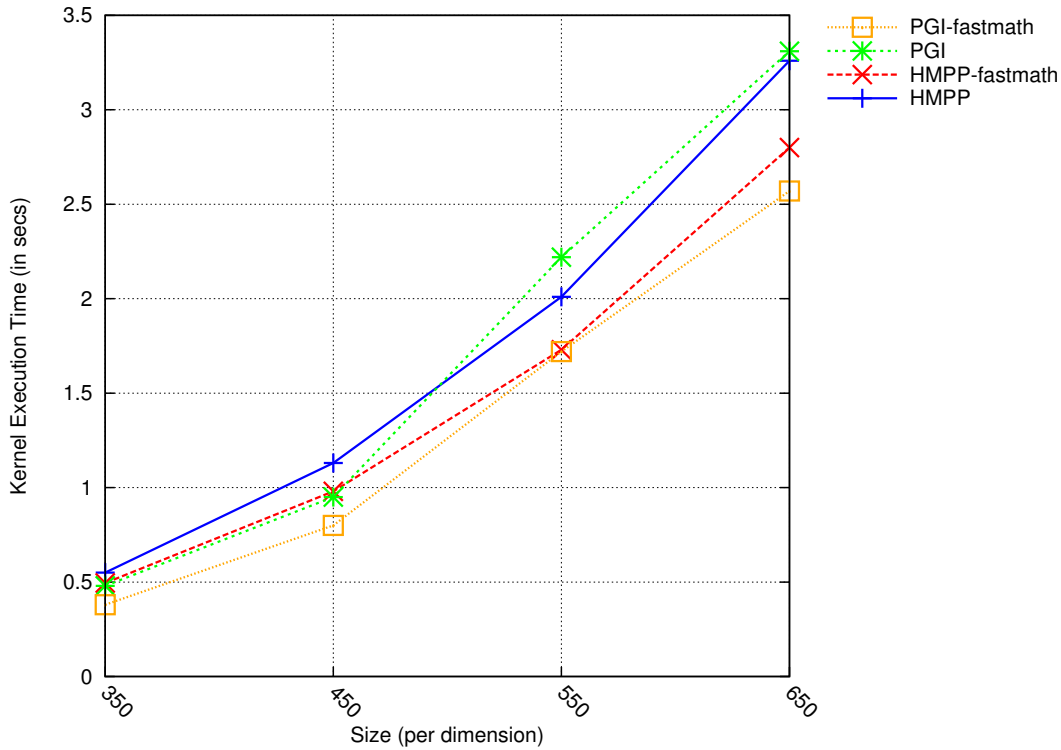
- cc13 implemented a truncated FMAD, which made it faster but inaccurate



Differences between PGI/HMPP sm13 (previous generation) vs sm20 (current generation) device options on ISO

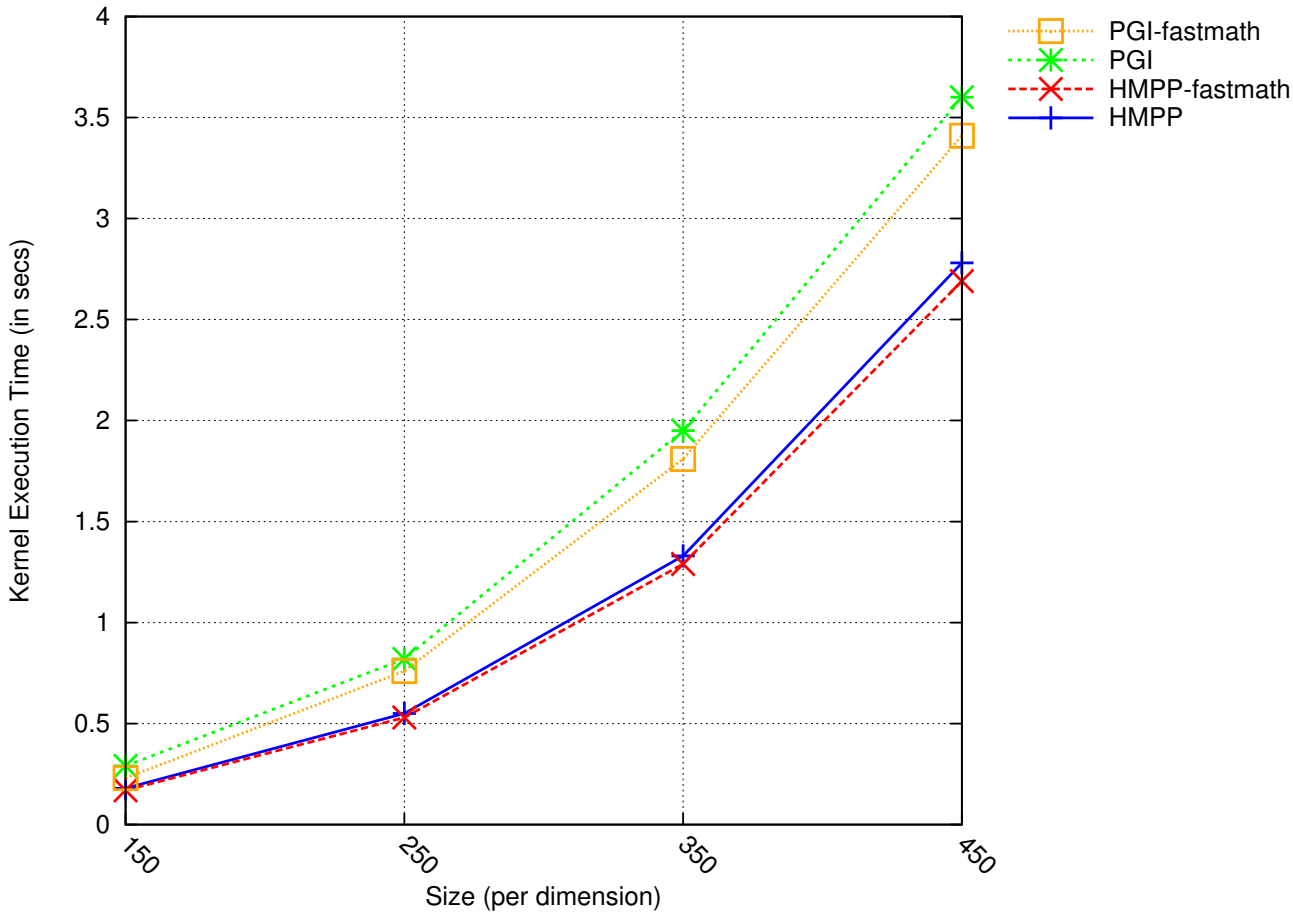
Fast-math compiler option - ISO

- HMPP: `-ftz=true -prec-div=false -prec-sqrt=false -use-fast-math`
- PGI: `-ta=nvidia,cc20,flushz,fastmath`



- This option just substitutes certain math functions with faster less-precise alternatives - independent of compiler front-ends

Fast-math compiler option - TTI



- More multiplications, more scope for fast-math optimizations

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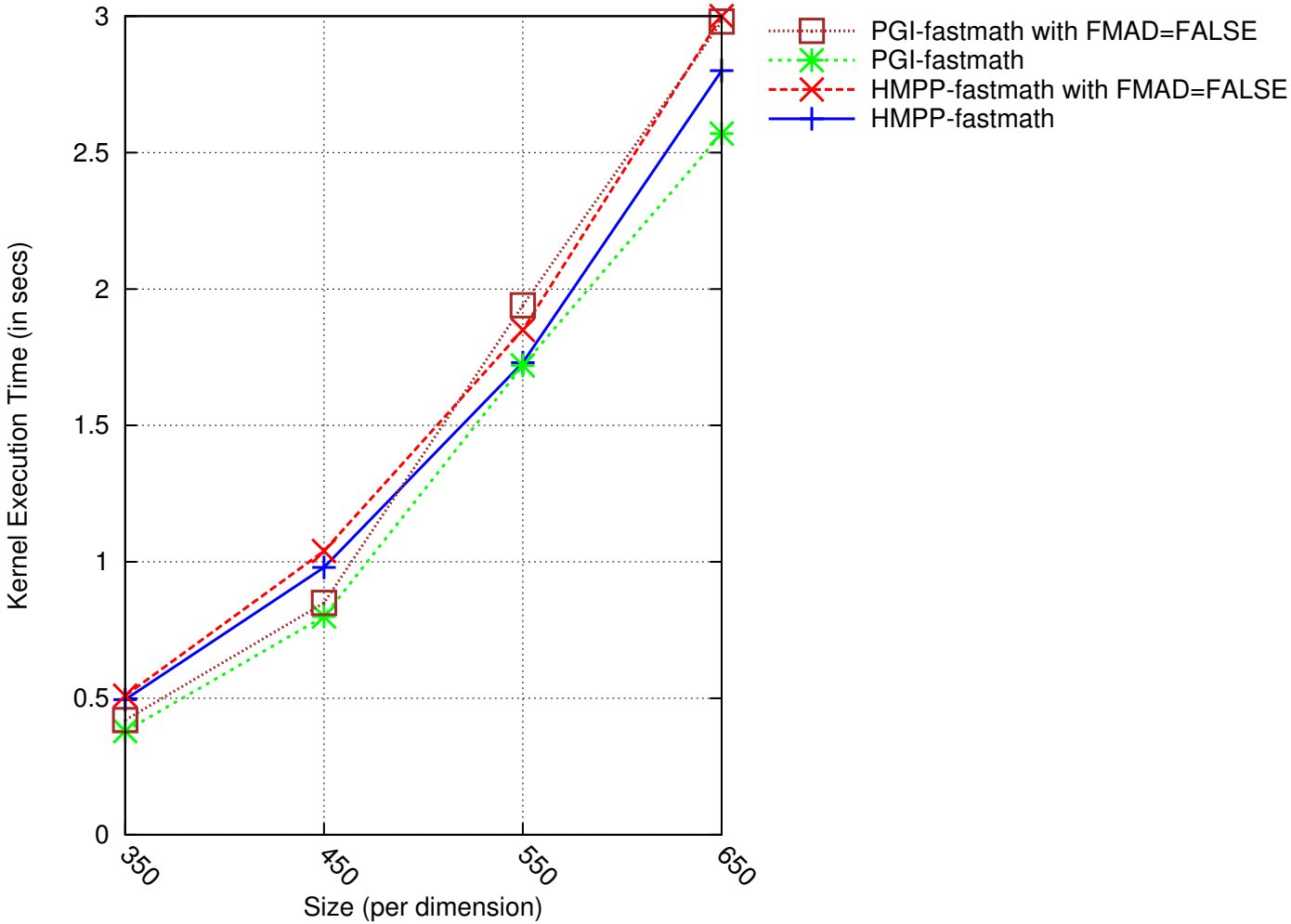
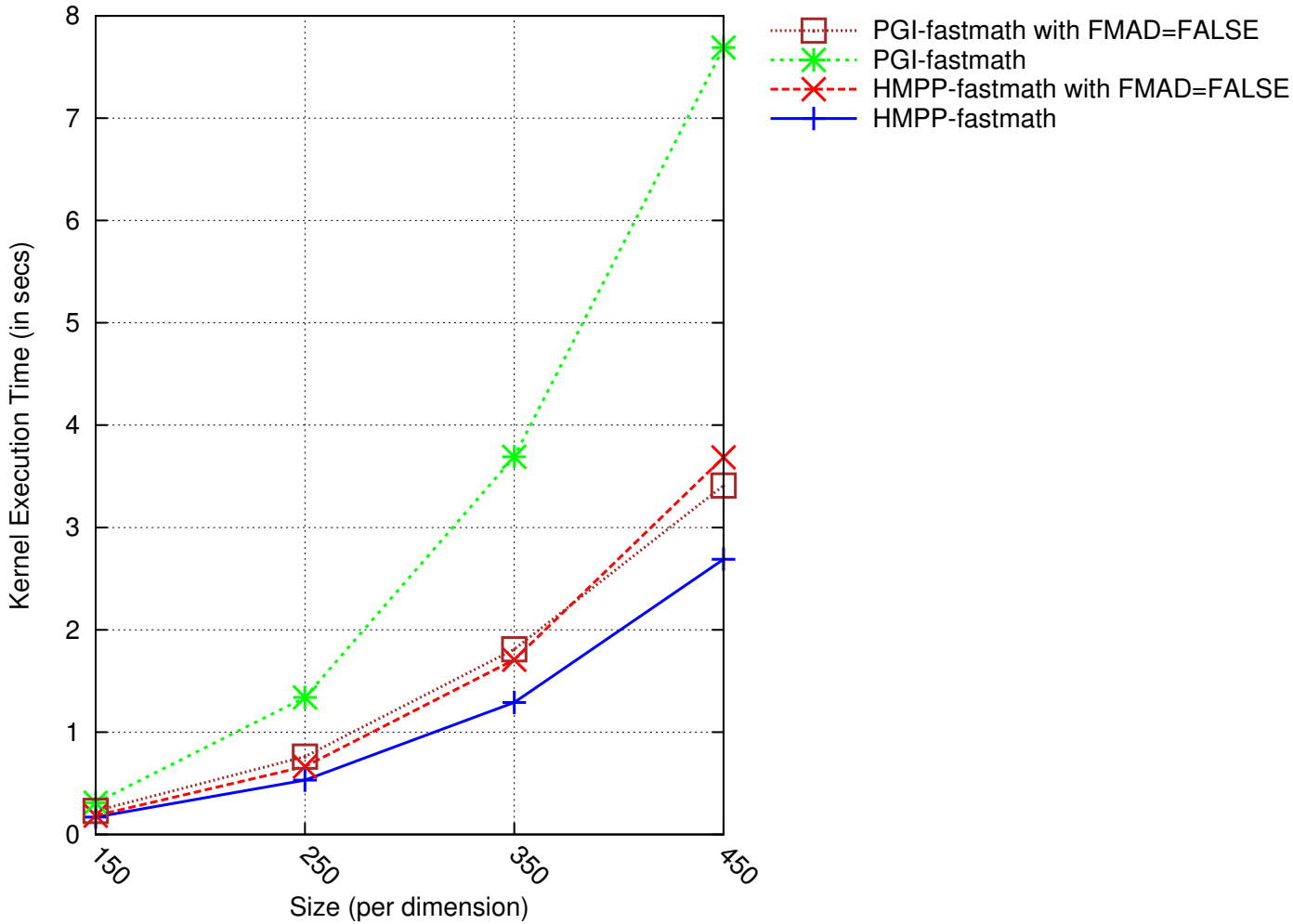


HMPP/PGI with FMA turned OFF Vs FMA turned ON for ISO (memory bound)

Enabling/disabling FMA - ISO and TTI



- For HMPP - performance drops when FMA=FALSE; For PGI - performance increased when FMA=FALSE

Different compiler front-ends of CUDA - NVVM vs Open64

- Prior to CUDA 4.1, NVCC used Open64 front-end; now LLVM front-end, NVVM
- The -open64 flag instructs NVCC to use Open64 front-end

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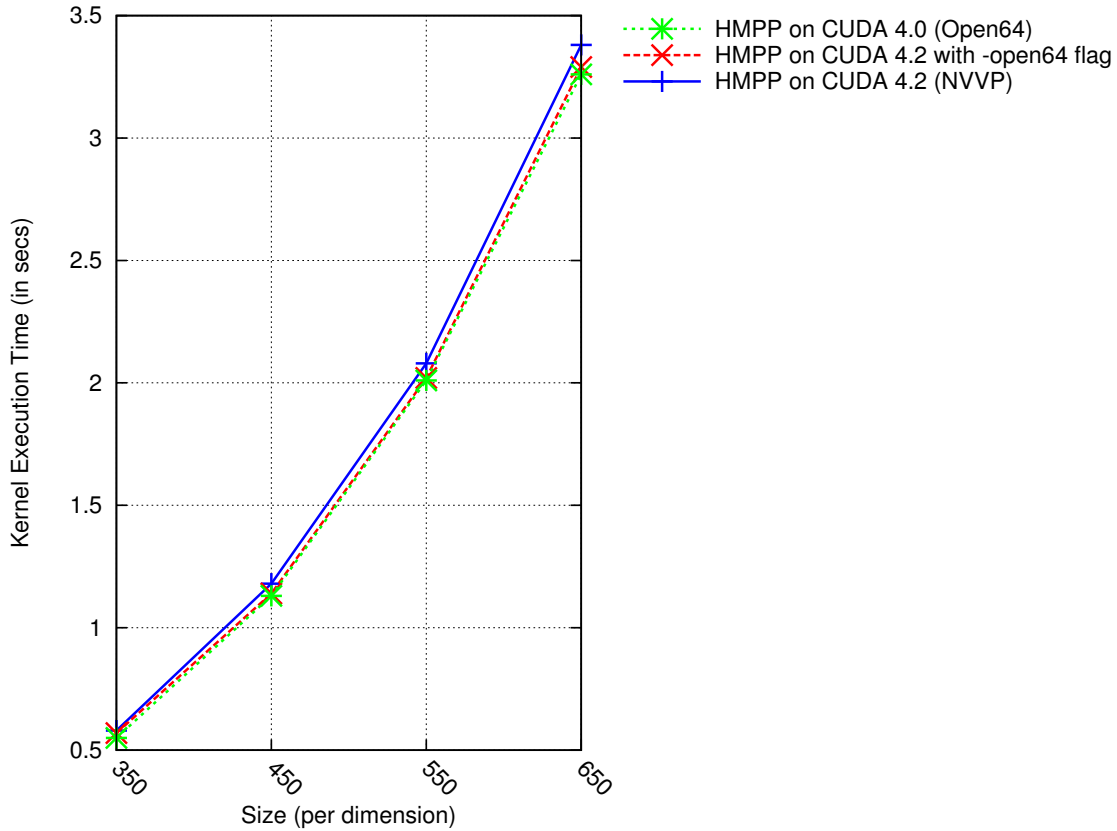

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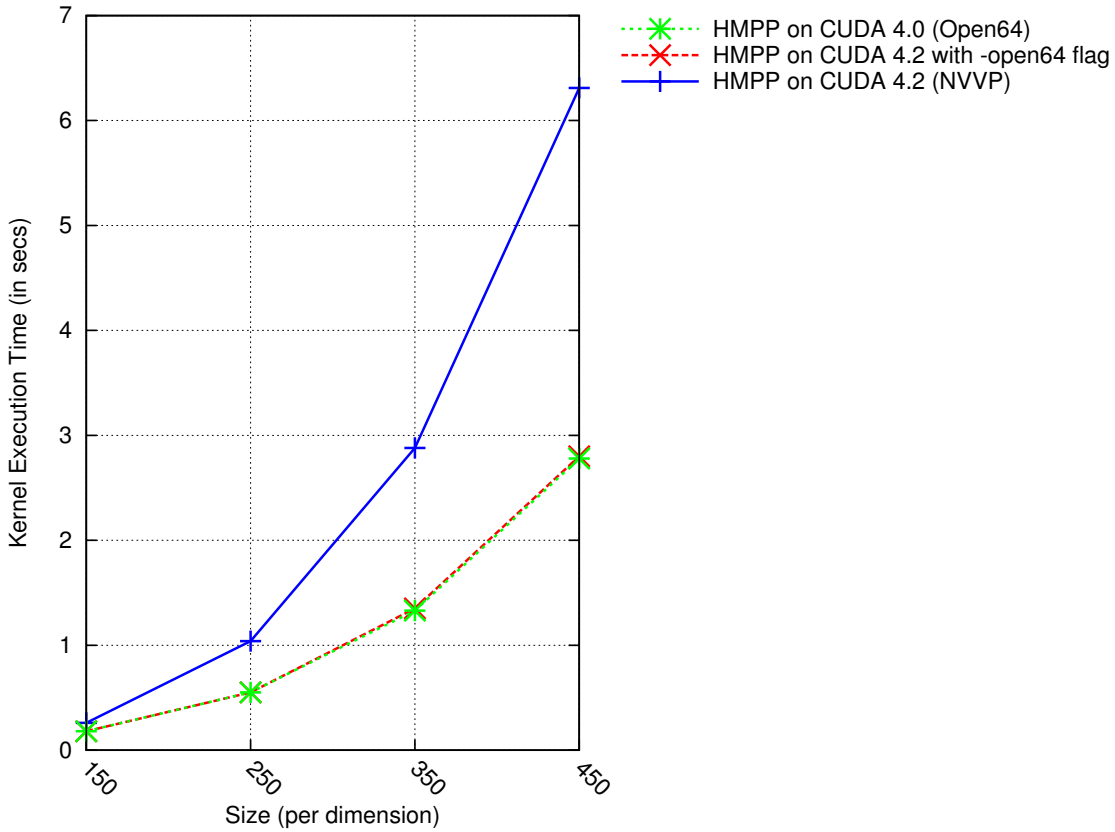

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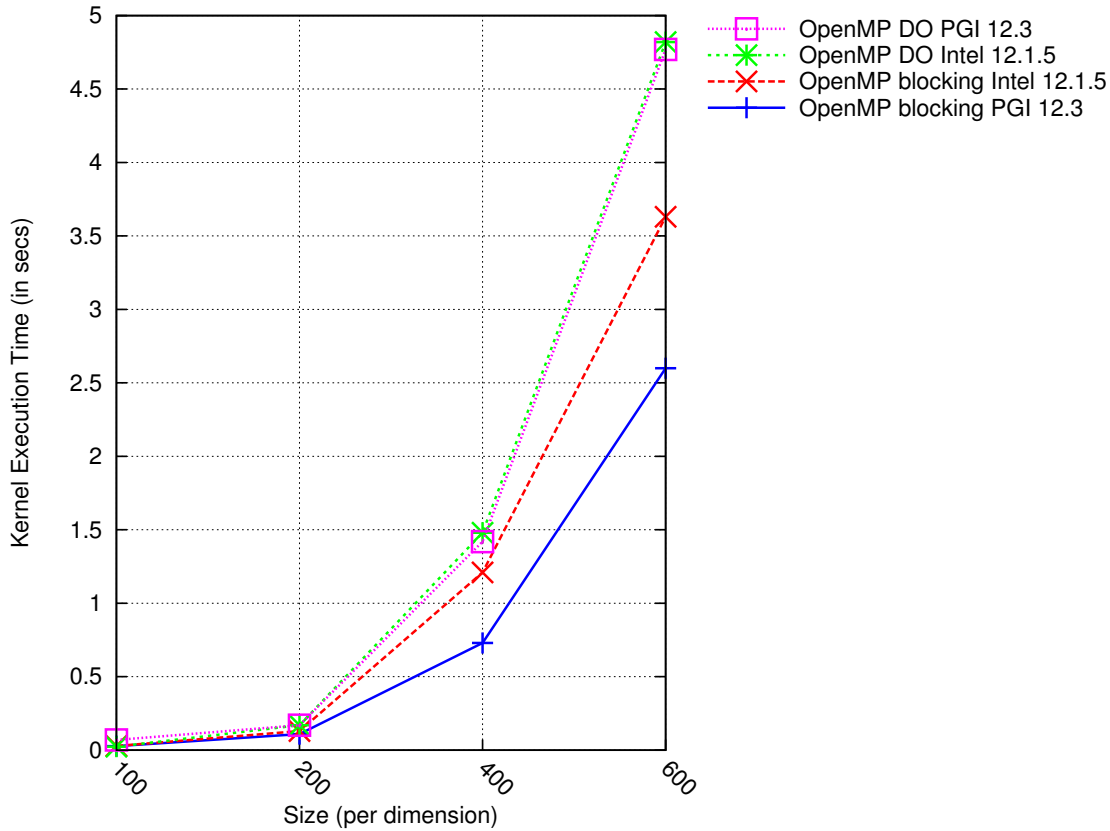
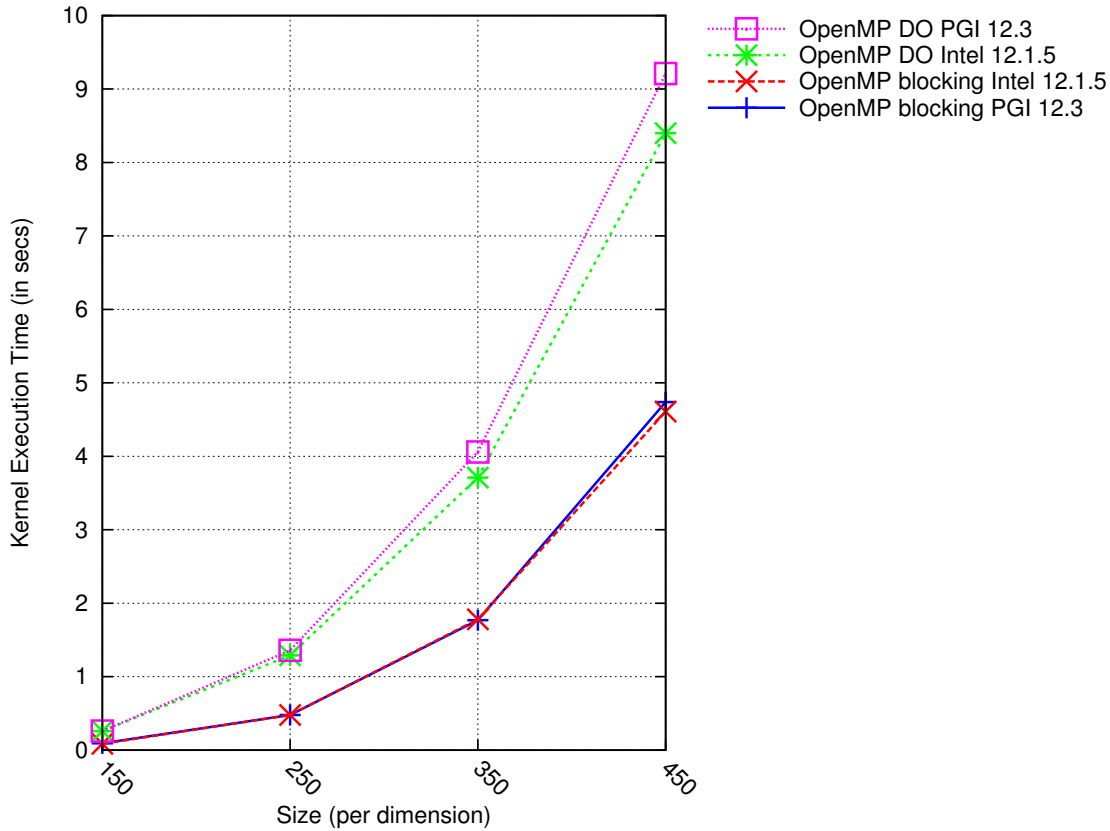
Block sizes for OpenMP cache blocking - ISO and TTI

ISO Data Size	**ISO Block Size(jXk)**	**TTI Data Size**	**TTI Block Size(jXk)**
100	4X4(Intel) / 8X8 (PGI)	150	4X4
200	8X8(Intel) / 16X16(PGI)	250	8X8
400	64X64	350	16X16
600	64X64	450	16X16

OpenMP blocking implementation of ISO on PGI and Intel compiler



OpenMP blocking implementation of TTI on PGI and Intel compiler



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  - Asynchronous clause was found to degrade performance

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  - Pointers may not work in compute region
  - Implicit model (just !$acc kernels) might not yield the best results
  - Unsupported/Unstable clauses (`cache`, `async`)
- **Adaptability**
  - Strong chances of code modification if pointers are used (PGI)
  - Unsupported language features (Fortran async I/O)
  - Compilers might not strictly adhere to specifications (!$acc gang in PGI/CAPS)
- **Performance**
  - Compiler front-ends/Compiler options might significantly affect performance (`-nofma`, `-fastmath`)
  - Asynchronous clause was found to degrade performance
  - `cache` clause might cause overheads as compiler might try to use shared memory anyway

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Future work

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- Target multiple GPUs using Accelerator directives

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- My colleagues at HPCTools lab (University of Houston)

Accelerator Directives / Kernels	ISO	TTI
CAPS HMPP	1.29	1.76
PGI Accelerator	0.85	1.39
OpenACC	1.54	1.73

Questions?