Abstract

This paper enumerates high speed design of RS & D- flip-flop using AlGaAs/GaAs MODFET. The proposed Flip Flop is having less number of transistors than existing designs. Simulation results show lowest average power and least delay than existing designs. This Flip-Flop having less number of transistors. It can be efficiently used in VLSI ICs. In the verification by simulation, the proposed flip-flops appear to have better speed of operation. It is simple and suitable to SPICE simulation of hybrid digital ICs.

References

- Yu Chien-Cheng,, &quot;Low-Power Double Edge- Triggered Flip-Flop Circuit Design,&quot; Third International Conference on Innovative Computing Information and Control
Design of RS and D-Flip-Flop using AlGaAs/GaAs MODFET Technology

(ICICIC'08), IEEE Conference, 2008.


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Keywords
    Flip-Flop  MODFET  delay  PDP  power consumption.