On-chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation

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Outline

1. Introduction
2. Proposed Monitor Circuits
3. Measurements from Corner Chips
4. Parameter Extraction Results
5. Conclusion
Testing of Chip is a Huge Task

- Testing is a must to ensure correct operation.
- Test effort $>$ Design effort
- Need correct strategy.

Fault Types
- Manufacturing fault.
- Parametric fault.

Test Types
- Functional test.
- Delay test.

This research proposes process-sensitive monitor circuits for parametric fault based delay defects.
Delay Defects

- Manufacturing defect or parametric defect?
- If parametric defect, how to debug the defect?
  - What caused the delay defect? Threshold voltage fluctuation? Gate length deviation? etc.
  - The model was not correct? Failed to predict the values. Need to correlate the model to hardware. Continuous feedback required.
Process Variation

Variation in performance

Process variation

Design option

- Design for worst cases.
- Design for typical case and bin the products.
  - Maximum operating frequency?
- Amount of spread for statistical design approach?
How helpful are PCM data?

- Difference in layout.
- Location in the wafer.
- Not product-representative. DC vs. AC.
- Often different sizes due to probing.

Product-representative monitor circuits \(^1\) \(\Rightarrow\) On-chip Detection

\(^1\) Gattiker et al., ITC’2006.
Monitor Circuits

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Monitoring process-characteristics from product chips.

Efficient model-to-hardware correlation methodology.

Distinguish manufacturing fault and parametric fault.
Outline

1. Introduction

2. Proposed Monitor Circuits
   - On-chip Monitor Circuits
   - Model-Hardware Correlation

3. Measurements from Corner Chips

4. Parameter Extraction Results

5. Conclusion
Proposed Monitor Circuits

- Embed monitor circuits.
- Process-sensitive monitor structures.
Parameter-sensitive Monitor Structure

**Conventional**

- Sensitive to both nMOSFET and pMOSFET
- Not-suitable for on-chip detection.

**Proposed**

- Sensitive to either nMOSFET or pMOSFET.
- Suitable for on-chip detection.
Process corners are distinguishable using the proposed monitor circuit outputs.

- Quick detection of process-characteristics.
- Reduce debugging time for delay defects.
Extract parameters from monitor circuit outputs\textsuperscript{2}.

Need parameter-sensitized monitor circuits.

Need to characterize monitor circuits by simulation.

\textsuperscript{2}Mahfuzul et al., ICMTS’2011
Process Shift \( \text{Amount of shifts in process parameters. Global variation.} \)

Parameter Extraction

- Consider RO frequency as a function of \( \Delta V_{thp}, \Delta V_{thn} \) and \( \Delta L \).

\[
F = f(\Delta V_{thp}, \Delta V_{thn}, \Delta L) = F_0 + k_p \Delta V_{thp} + k_n \Delta V_{thn} + k_l \Delta L
\]

- 3 equations from 3 ROs.
- Solve the equations and derive unknown \( \Delta V_{thp}, \Delta V_{thn} \) and \( \Delta L \).\(^a\)

\(^a\)Mahfuzul, et al., ICMTS 2011
Process Spread  Amount of deviation in process parameters within a chip. Local variation.

Parameter Extraction

- Assume linear sensitivity of each variability source.

\[
F = F_0 + \sum_i \left( K_{V_{thp}} \Delta V_{thp}^i + K_{V_{thn}} \Delta V_{thn}^i + K_L \Delta L_i \right).
\]

\[
\left( \frac{\sigma_F}{\mu_F} \right)^2 = \sum_i \left( k_{V_{thp}}^2 \sigma_{V_{thp}}^2 + k_{V_{thn}}^2 \sigma_{V_{thn}}^2 + k_{L_i}^2 \sigma_L^2 \right).
\]

- 3 equations from 3 ROs.
- Solve the equations and derive $\sigma_{V_{thp}}, \sigma_{V_{thn}},$ and $\sigma_L$.\(^a\)

\(^a\)Fujimoto, et al., ICMTS 2012
Measurements from Corner Chips

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1. Introduction
2. Proposed Monitor Circuits
3. Measurements from Corner Chips
   - Test Chip Design
   - Measurement Results
4. Parameter Extraction Results
5. Conclusion
65 nm triple well process.
Array based structure to capture local variation.
$14 \times 21 = 294$ instances of the same RO type.
TT, SS, FF, FS, SF corner chips.
Mismatch between corner model and measurement.

Amount of process shift?
- Amounts of shifts in key process parameters?

Amount of spread?
### Measurements from Corner Chips

#### Measurement Results

**WID Variation**

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**% Variation**

- **nMOSFET monitor**
- **pMOSFET monitor**
- **Standard inverter monitor**

- nMOSFET variability is larger than pMOSFET variability

⇒ Important for statistical design.
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Amount of shifts are extracted.
- Prediction of performances.
- Feedback to model.
Table: Extracted standard deviation of MOSFET threshold voltages and gate length from RO frequency measurements.

<table>
<thead>
<tr>
<th>Corner</th>
<th>$\sigma_{V_{thn}}$ [mV]</th>
<th>$\sigma_{V_{thp}}$ [mV]</th>
<th>$\sigma_{L}$ [nm]</th>
</tr>
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<tbody>
<tr>
<td>TT</td>
<td>16.6</td>
<td>11.9</td>
<td>0.89</td>
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<td>SS</td>
<td>18.3</td>
<td>14.5</td>
<td>0.53</td>
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<td>FF</td>
<td>20.9</td>
<td>16.6</td>
<td>1.14</td>
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<td>FS</td>
<td>18.2</td>
<td>13.3</td>
<td>0.99</td>
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<tr>
<td>SF</td>
<td>18.2</td>
<td>13.6</td>
<td>0.99</td>
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- FF corner has larger variation.
- SS corner has smaller $\Delta L$ variation.
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Conclusion

Summary

- Use of monitor circuits for detection of process corner and process spread.
- Product-representative monitor circuits suitable for detection is proposed.
- Model-to-hardware correlation methodology is proposed.
- Test chip has been fabricated in a 65 nm process.
- Experimental results from corner chips show the validity of the proposed circuits.