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Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing

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Dielectric properties of ultrathin hafnium oxide reoxidized with rapid thermal annealing (RTA) have been investigated. Capacitance equivalent oxide thickness (CET) of 45 Å hafnium oxide was scaled down to ~10 Å with a leakage current less than 3×10^{-2} A/cm^2 at −1.5 V (i.e., ~2 V below V_{FB}). Leakage current increase due to crystallization was not observed even after 900 °C rapid thermal annealing (RTA), but CET did increase after high temperature RTA due to the interfacial layer growth and possible silicate formation in the HfO_2 film. © *2000 American Institute of Physics.* [S0003-6951(00)04414-4]

High-*k* gate dielectric materials, such as CeO_2, Y_2O_3, Al_2O_3, Ta_2O_5, ZrO_2, HfO_2, TiO_2, $SrTiO_3$(STO), and $BaSrTiO_3$ (BST) have been studied as alternatives for SiO_2. The basic idea for using high-*k* materials is increasing the film thickness to reduce the tunneling leakage current and improve the reliability while scaling the capacitance equivalent oxide thickness (CET) below the direct tunneling limit of SiO_2.

However, CeO_2, Y_2O_3, and Al_2O_3 do not provide significant advantages over SiO_2 or Si_3N_4 because of the relatively low dielectric constants and ultrahigh-*k* materials such as STO and BST have been predicted to cause poor short channel effects due to the fringing field induced barrier lowering effect.[1] In addition, most of the high-*k* materials (e.g., Ta_2O_5 and TiO_2) are thermally unstable and may form silicides or low-*k* interfacial layers when directly contacted with silicon.[2]

Thus, HfO_2 and ZrO_2 are attractive since they are thermodynamically stable in contact with Si. HfO_2, especially, has many desirable properties such as high dielectric constant (~30), high heat of formation (271 kcal/mol),[3] and relatively large band gap (5.68 eV).[4] In addition, HfO_2 is compatible with n^+ polysilicon without any barrier layer and ultrathin HfO_2 with a CET ~11.5 Å has been demonstrated using reactive dc magnetron sputtering.[5] In this letter, we present the electrical and thermal stability characteristics of HfO_2 reoxidized using the rapid thermal annealing (RTA) process. This process turns out to have several advantages over reactive dc sputtering such as excellent CET scalability, lower leakage current, and good interface properties.

Metal–oxide–semiconductor (MOS) capacitor devices with thin HfO_2 gate dielectrics have been fabricated using the following process. First, field oxide was grown on a *p*-type (100) silicon substrate and patterned with an active area mask. A thin hafnium layer was then deposited using dc magnetron sputtering in Ar ambient at a pressure of 40 mTorr. Sputtering power density for hafnium was 2.47 W/cm^2. The base pressure of the vacuum chamber was 4×10^{-7} Torr. These samples were transferred to the RTA chamber and annealed under various conditions (e.g., varying temperature, time, ambients, and chamber purging time). After RTA annealing, a Pt electrode was sputter deposited, patterned, and etched using aqua regia solution ($1HNO_3:7HCl:5H_2O$) at 80 °C. Sputtering power density for Pt was 2.47 W/cm^2 and process pressure was 20 mT. The active area for the MOS ($Pt/HfO_2/Si$) capacitor is 5×10^{-5} cm^2. The effects of postmetal RTA have also been studied. After gate patterning, the backside of the wafer was etched to expose silicon substrate and metallized with aluminum to reduce the series resistance.

X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) were used to study the behavior of Hf–O bonds during the postdeposition annealing. Electrical properties of the MOS capacitor were measured using a HP4194 impedance/gain-phase analyzer and a HP4156A semiconductor parameter analyzer. CET was extracted from an accumulation capacitance measured at 1 MHz, without deducting for the quantum mechanical effect. Since the leakage current under positive bias can be limited by the minority carrier generation, the leakage current was measured at both +1 V and −1.5 V.

As expected, the oxygen ambient yielded a thicker CET than the nitrogen ambient (Fig. 1). RTA time does not seem to have a strong effect on the CET and the leakage current in a N_2 ambient. Most of the changes in CET and leakage cur-

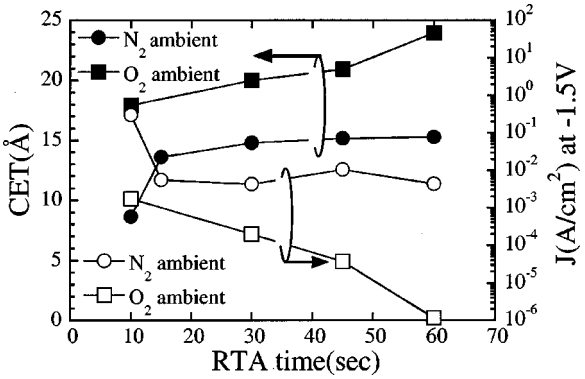

FIG. 1. Effect of RTA time at 700 °C on CET and *J* for various annealing ambients. Physical thickness of HfO_2 film was ~45 Å.

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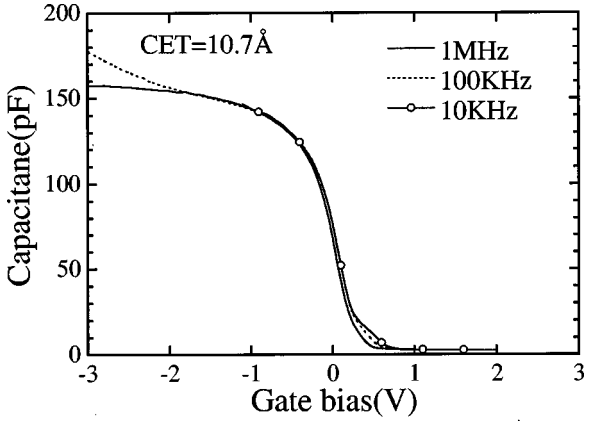

FIG. 2. Typical C–V curve of HfO_2 reoxidized at 600 °C RTA in an N_2 ambient for 15 s. Film thickness was ~45 Å and capacitor area was 5×10^{-5} cm^2. Slight capacitance increase at −2.5 V for 100 kHz is due to the leakage current, not frequency dispersion.

rent occur during the first 15 s. In the case of O_2 ambient, the CET increased slightly by extended RTA and the leakage current decreased accordingly.

Well-behaved capacitance–voltage ($C-V$) characteristics were obtained even after annealing the hafnium layer in the nitrogen ambient (Fig. 2). XPS analysis showed that the hafnium layer deposited in an Ar ambient contained enough oxygen to form HfO_2. Oxygen might be incorporated into the film during the hafnium deposition or transportation to the RTA chamber. The CET of HfO_2 film shown in Fig. 2 is 10.7 Å and the effective dielectric constant is ~16.4. A slight increase of capacitance at −2.5 V for 100 kHz is due to the leakage current rather than frequency dispersion. Frequency dispersion of accumulation capacitance measured at −1 V (to avoid the error due to the leakage current) was less than 2%/dec in the 10 kHz–1 MHz range. Midgap interface state densities extracted from the high frequency $C-V$ curve using the Terman method were around $7\times10^{10}\,eV^{-1}\,cm^{-2}$.

Unlike other metal oxides such as Ta_2O_5, the leakage current of HfO_2 films did not increase after high-temperature RTA (Fig. 3). CET increased as the RTA temperature was increased. The longer N_2 purging time before ramping up the temperature does not have much effect on the CET, but it does reduce the leakage current slightly. The increase of CET is very sensitive to the RTA temperature, which suggests a thermally activated reaction.

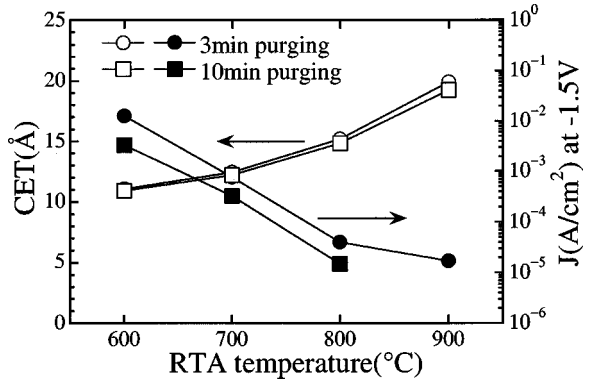

FIG. 3. Effects of pre-Pt RTA temperature on the leakage current and CET for various N_2 purging time. RTA time was 15 s.

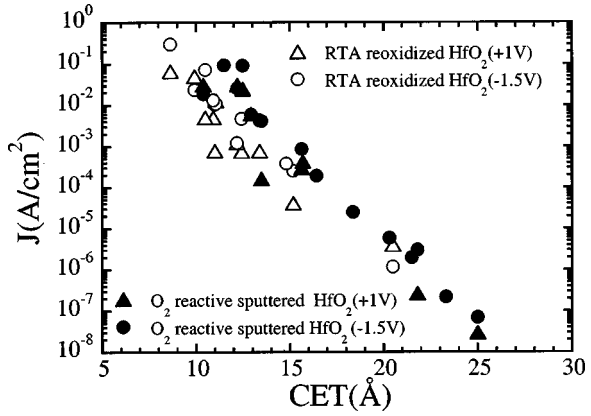

FIG. 4. *J*-CET distribution for the sputter deposited HfO_2 and RTA reoxidized HFO_2 films.

Although the slope of *J* vs CET plot shows a similar trend for both sputter deposited HfO_2 and RTA reoxidized HfO_2 (Fig. 4), the CET of reoxidized HfO_2 could be scaled down below 10 Å, which was not easy for reactive-sputtered HfO_2 (i.e., sputtered in O_2 ambient). Note that the leakage current of HfO_2 with a CET of ~10 Å is still less than 3×10^{-2} A/cm² at −1.5 V and 5×10^{-2} A/cm² at +1 V, which satisfies the <4 A/cm² requirement for 100 nm MOS field effect transistors.[6]

Hysteresis of $C-V$ curves is common for high-*k* materials and needs to be minimized. The cause of hysteresis for HfO_2 is believed to be due to charge trapping under negative gate bias. Hysteresis of as-deposited HfO_2 was quite large, but could be reduced to a negligible level using post-Pt annealing without any increase in the CET value (Fig. 5). The difference of hysteresis between pre-Pt RTA and post-Pt RTA indicates that about 200 mV of hysteresis is attributable to the damage during Pt deposition.

XPS analysis on 40 Å RTA reoxidized HfO_2 films shows an interesting snap back of the Hf–O peak toward the elemental hafnium peak after 900 °C RTA in nitrogen (Fig. 6). It is not clear whether the peak shift is due to the dissociation of Hf–O bonds or the formation of Hf–Si–O bonds. Such snap back was not observed in an O_2 ambient. Also, the significant increase of Si–O bonds after 900 °C RTA in an O_2 ambient (data not shown) suggests the growth of the interfacial layer.

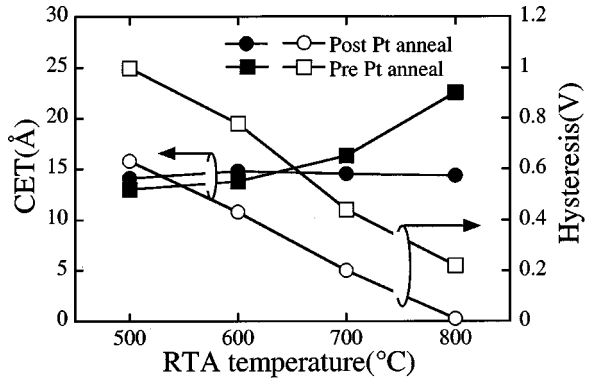

FIG. 5. Hysteresis decreased as RTA temperature increased. The effects of post-Pt RTA and pre-Pt RTA in N_2 ambient were compared. RTA time was 15 s for pre-Pt RTA and 5 s for post-Pt RTA. The annealing ambient was N_2.

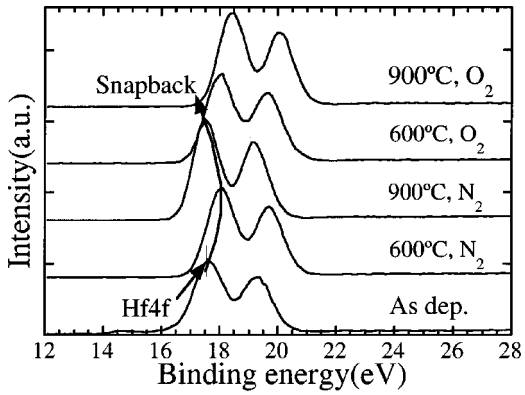

FIG. 6. Hafnium peak shift of 40 Å RTA reoxidized HfO_2 annealed at various temperatures.

TEM analysis (data not shown) on sputter deposited HfO_2 film showed that the thickness of the interfacial layer was increased to 15 Å after 700 °C, 5 min furnace anneal in N_2 ambient from 7 Å after 500 °C. Thus, most of the CET increase is due to the growth of the interfacial layer. The composition of the interfacial layer is believed to be hafnium silicate because the estimated dielectric constant of the interfacial layer is higher than that of SiO_2. In fact, this interfacial layer is beneficial in that it reduces the interface state density and improves the reliability.[5] The formation of this hafnium silicate interfacial layer is not due to the reaction between hafnium and silicon, but rather due to the oxygen diffused into the HfO_2 film during RTA. HfO_2 seems to be very transparent for oxygen diffusion.

In summary, HfO_2 with CET$\sim$10 Å with leakage current $<3\times10^{-2}$ A/cm^2 at -1.5 V was obtained using a simple RTA reoxidation process. Excellent dielectric properties such as high dielectric constant, low leakage current, low interface state density, and good thermal stability indicates that HfO_2 is a promising material as an alternative gate dielectric.

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