A HIGH-SPEED LOW-POWER RAIL-TO-RAIL BUFFER AMPLIFIER FOR LCD APPLICATION

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Abstract

A high-speed low-power rail-to-rail class-B buffer amplifier, which is suitable for liquid crystal display applications, is proposed. The summing circuit is biased by the constant current sources to applicable different supply voltages. The buffer draws little current while static but has a large driving capability while transient. The circuit achieves the large driving capability by employing simple comparators to sense the transients of the input to turn on the output stages, which are statically off in the stable state. This increases the speed of the circuit without increasing static power consumption too much. An experimental prototype output buffer implemented in a 0.35-\(\mu\)m CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent currents of 5.4 \(\mu\)A and 7.4 \(\mu\)A are measured for power supplies of 3.3 V and 8 V, respectively. The buffer exhibits the settling time of 1.5 \(\mu\)s for a voltage swing of 0.1 ~ (VDD – 0.1) V under a 600 pF capacitance load. The area of this buffer is \(29.3 \times 86.3 \mu\text{m}^2\).

Keywords: Buffer Amplifier, LCD, Column Driver.

1. Introduction

As Liquid-crystal displays (LCDs) are recently installed in notebook type personal computers and compact desktop personal computers and monitors are becoming larger and higher definition, there is a big demand of developing low-power dissipation, high resolution, small settling time and high-speed LCD driver [1-6]. An LCD driver is generally composed of column drivers, gate drivers, a timing controller, and a reference source. The column drivers are especially important to achieving high-speed driving, high resolution and low-power dissipation [1-3]. A column driver generally includes registers, data latches, digital-to-analog converters (DAC’s) and output buffers. Among those, the output buffers determine the speed, resolution, voltage swing and power dissipation of the column drivers [2, 5]. Due to the thousands of output buffer amplifiers built into a single chip, the buffer should occupy a small die area, and its static power consumption should be small. The output buffer should offer an almost rail-to-rail voltage driving which can accommodate higher gray levels. Also, the settling time should be smaller than the horizontal scanning time.

Some output buffers were proposed and demonstrated to reduce the power consumption in recent years. For examples, Yu et al [4] proposed a class-B output buffer for flat-panel display column driver, for which a comparator was used in the negative feedback path to eliminate the quiescent current in the output stage. Weng et al. [5] proposed a compact, low-power, and rail-to-rail class-B output buffer for driving the large column line capacitance of LCDs, where a nonlinear element in feedback path is modified from the current-mirror amplifier to obtain the area and power advantages. Lu [2] proposed a high-speed driving scheme and a compact high-speed low-power rail-to-rail class-B buffer amplifier, which are suitable for both of the small- and large-size liquid crystal display applications. This buffer amplifier employs a double cascode current mirror as the load of the rail-to-rail differential pairs. Since the cascode current mirror is a self-bias configuration, it cannot be operated under a wide range of power supply. An LCD driver should applicable to different power supplies [7]. In this work, a buffer amplifier, which can be operated under a wide range of power supply, is proposed.

2. Proposed Buffer Amplifier

Fig. 1 shows the configuration of the proposed rail-to-rail buffer amplifier. The connected points are labeled with the alphabets A ~ H. As a buffer, “output” is connected to the inverting input (in-) and the input signal is applied to the non-inverting terminal (in+). The capacitive load is connected to the output. This buffer consists of a bias stage (Mb1~Mb8 and Rb), a rail-to-rail differential amplifier (M1~M8), a current summer (M9~M12), comparators (M21~M24), and the output transistors (M25 and M26). The rail-to-rail differential pairs M3~M4 and M7~M8, which are biased by the constant current sources M1~M2 and M5~M6, are actively loaded by the current summer. The current summer, which is biased by the constant current sources (M9~M12) to applicable different supply voltages, is used to add the currents of the rail-to-rail differential amplifiers and then transfer the current to voltages for the comparators. The comparators are used to amplify the voltage difference of two inputs. Then the outputs of the comparators turn on/off the transistors of the output stages.
ratios of the buffer are designed as:

\[
\begin{align*}
\frac{W}{L_J} &= \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = 2 \\
\frac{W}{L_J} &= \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = 2 \\
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\frac{W}{L_J} &= \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = \frac{W}{L_J} = 2 \\
\frac{W}{L_J} &< \frac{W}{L_J} \quad \text{and} \quad \frac{W}{L_J} > \frac{W}{L_J} \\
\frac{W}{L_J} &> \frac{W}{L_J} \quad \text{and} \quad \frac{W}{L_J} < \frac{W}{L_J}
\end{align*}
\]

In the stable state, the output voltage is equal to the input voltage. The currents flowing in all transistors of the differential pairs are \( I \) where \( I \) is the current flowing in the bias stage. The currents flowing in the constant current sources of M9–M12 are also \( I \). Then the currents flowing in M13–M14 and M19–M20 have twice the current in the bias stage, i.e., 2\( I \). Since M13–M20 are two cascade current mirrors, the drain voltage of M14 is equal to that of M13 and the drain voltage of M20 is equal to that of M19. The currents flowing in the current mirrors are mirrored to the comparators. The aspect ratio of M21 is designed to be smaller than half that of M14 and the W/L of M22 is larger than half that of M20, this causes M21 to be in the saturation region but M22 to go out of the saturation region and be in the triode region. Then the drain voltage of M22 is pulled down to a very low level. Similarly, due to the mismatch design, M23 stays in the triode region and M24 goes to the saturation region. The drain voltage of M23 is close to VDD. This makes the output transistors M25 and M26 cut off from the output node and consume no power in the stable state.

When the input voltage, \( \text{in}+ \), is reduced, the currents in M3 and M8 will be increased, but the currents in M4 and M7 will be decreased. The gate voltages of M14 and M20 will be increased and the gate voltages of M21–M24 will be decreased. As a result, M21 will go into the triode region and M22 will go into the saturation region. The drain voltage of M22 will increase to turn on M26. Then M26 starts to discharge the output node. However, M25 is still in the cut off region. When the output voltage reaches the level that the voltage difference between the input and output is almost zero, M26 stops discharging the output node. Since the gate voltages of M26 can reach a value of VDD, M26 can be turned to fully “on” to discharge the output at a maximal speed. Similarly, when the input voltage, \( \text{in}+ \), is increased, M26 is still cut off from the output, but the gate voltage of M25 is reduced and M25 starts to charge the output load until the output voltage almost equal to the input voltage. The gate voltage of M25 can be pulled down to a very low level, so M25 can charge the output load at a maximal speed.

3. Experimental Results

The proposed output buffer amplifier was fabricated using a 0.35-μm CMOS technology. The die photograph is shown in Fig. 2. The area of the buffer is only 29.3×86.3 μm². Quiescent currents of 5.4 μA and 7.4 μA are measured for power supplies of 3.3 V and 8 V, respectively. Fig. 3 (a) and (b) show the measured results of the output with the input of a large dynamic range of a 20 KHz triangular wave of the proposed buffer amplifier loaded with a large size capacitor of 600 pF for power supplies of 3.3 V and 8 V, respectively. The upper traces are the input waveforms and the lower ones are the measured output waveforms. They can be seen that the outputs basically follow the inputs. Fig. 4 (a) and (b) show the step responses of the same buffer loaded with a capacitance of 600 pF with the voltage swings of 3.1 V and 7.8 V for power supplies of 3.3 V and 8 V, respectively. The upper traces are the input waveform and the lower ones are the measured output waveforms. The settling times for the output to settle to within ±5 mV of the final voltage are only 1.5 μs for both the supply voltages of 3.3 V and 8 V. The performance of the proposed buffer is summarized in Table 1. Compared with the previous buffers, the proposed circuit is superior in supply voltage range, input/output voltage range, area, quiescent power consumption and settling time.

4. Conclusions

In this work, a high-speed low-power rail-to-rail class-B buffer amplifier, which is suitable for LCD applications, is
proposed. An experimental prototype output buffer implemented in a 0.35-µm CMOS technology demonstrates that the circuit can operate under a wide power supply range. Quiescent currents of 5.4 µA and 7.4 µA are measured for power supplies of 3.3 V and 8 V, respectively. The buffer exhibits the settling time of 1.5 µs for a voltage swing of 0.1 ~ (VDD – 0.1) V under a 600 pF capacitance load. The area of this buffer is 29.3×86.3 µm². Compared with the previous buffers, the performance of the proposed circuit is superior in supply voltage range, input/output voltage range, area, quiescent power consumption and settling time. The measured data do show that the proposed output buffer circuit is very suitable for LCD applications.

Fig. 2 Die photograph of the proposed buffer amplifier.

Fig. 3 The measured results of the output with the input of a large dynamic range of a 20 KHz triangular wave of the proposed buffer amplifier loaded with a large size capacitor of 600 pF for power supplies of (a) 3.3 V and (b) 8 V, respectively.
Fig. 4 The step responses of the proposed buffer loaded with a capacitance of 600 pF with the voltage swings of 3.1 V and 7.8 V for power supplies of (a) 3.3 V and (b) 8 V, respectively.

Table 1 Performance Summary.

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Process technology</td>
<td>0.35 µm CMOS</td>
<td>0.35 µm CMOS</td>
<td>0.8 µm CMOS</td>
<td>0.35 µm CMOS</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>3.3 ~ 8</td>
<td>3.3</td>
<td>5</td>
<td>3.3</td>
</tr>
<tr>
<td>Input/output range (V)</td>
<td>0.1 ~ (VDD − 0.1) (100% of VDD)</td>
<td>0.05 ~ 3.25 (97% of VDD)</td>
<td>1 ~ 5 (80% of VDD)</td>
<td>0 ~ 3.3 (100% of VDD)</td>
</tr>
<tr>
<td>Quiescent current (µA)</td>
<td>5.4 (VDD = 3.3 V)</td>
<td>7.4 (VDD = 8 V)</td>
<td>24</td>
<td>7</td>
</tr>
<tr>
<td>Settling time (µs)</td>
<td>1.5 for C_L = 600 pF</td>
<td>8 for C_L = 600 pF</td>
<td>8 for C_L = 600 pF</td>
<td>2.4 (rise) 2.3 (fall) for C_L = 600 pF</td>
</tr>
<tr>
<td>Active area (µm²)</td>
<td>29.3×86.3</td>
<td>86×73.5</td>
<td>230×140</td>
<td>46.5×57</td>
</tr>
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References