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Twin Channel of Speed Control System Based on DSP

Bin Li[1, a], Zhengfeng Cao [2,b], Jinping Hong[3,c]

[1, 2,3]Traffic & Mechanical Engineering School Shenyang Jianzhu University

[a]binli2010@sina.com, [b]miao_rf@sina.com, [c]hong-1111@163.com

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Abstract. A microprocessor as the core of the digital controller has become one of the major features AC speed regulation system in modern. Based on DSP as the core of the speed control system，it can realize complex algorithm. At the same time, it can achieve the diagnosis of system's fault, and the self-setting of parameters controlled, etc. Thus it can make the motor speed control system have higher performance. This paper introduces the motor speed control system which consists of three DSP. This system is able to adjust two Frequency conversion motor. Division of work to the DSP is according to the function of DSP. Inter-DSP makes use of dual-port RAM to exchange data and communicate. They work together to achieve and improve the performance of the control system.

Introduction

With the development of power electronics technology, kinds of new controller and advanced control method is applied by motor speed control system. The accuracy of AC motor control technology has been greatly improved. Introducing digital speed regulation system in the field of motor control can design a high-performance control system. The computing speed of control system is faster than μs. And it obtains efficient and reliable performance. Furthermore, the system doesn't require a large number of peripheral circuits.

The study is designing twin channel of speed control system composition of three DSP. Two chips of LF2407A are specially used to control two motor. Two pieces of LF2407A work independently. And a VC33 realize control algorithm. Inter-DSP makes use of dual-port RAM to exchange data and communicate. It ensures the real-time control.

The Hardware Structure of Speed Control System

TMS320LF2407A produced by TI is 16-bit fixed-point digital signal processor, and it is dedicate to motor control. The TMS320LF2407A is rich in Peripheral Resources. It is designed by low-power (3.3V), and its computational speed is 40MIPS. The advantage of the DSP is that each DSP has two event manager modules (EVA and EVB) to motion and motor controlling. Each event manager module has two general purpose timer which is 16-bit, and eight output channel of 16-bit pulse width modulation (PWM).The circuit of PWM has a programmable dead-zone and output polarity controlled. Dead-zone controlled can avoid short circuit when the upper and lower bridge is breakover at the same time. The PDPINT pin of EV module is able to provide voltage, over current and other anomalies to the motor's monitor, resulting in the protection interrupt of power drive. Those can offer to security guarantees for system operation such as power transform and motor drive.

TMS320VC33 is a 32-bit high-performance processor. It is lower consumption and higher the speed of processing data（150MFOLPS）. Its internal memory is up to 34K× 32 bit. VC33 adopts floating-point calculation which improves the precision of calculation. VC33 uses assembly line operation that is not only to improve the operation and processing speed, but also to reduce the phenomenon of the bus congestion. Because VC33 supports the C programming language very well, it makes the complicated control algorithm achieve better.

The system applies dual-port RAM (the model is CY7C025) to communicate between the DSP. Dual-port RAM is a special data storage chips(Shown in Figure 1)，Using dual-port RAM can implement sharing data between the DSP. Dual-port RAM has two independent ports. Each port has its own control bus, address bus and I / O port. Two CPU can read and write dual-port RAM arbitrary units separately. With the dual-port RAM share information rapidly between the CPU, and the mode of access is simple. It takes the same time to access data and share information as the general external RAM. Dual-port RAM has two sets of interrupt logic to achieve handshake signal between two CPU. Arbitration logic within the dual-port RAM has the following features: To control the accessing timing of the same address; To allocate the accessing permissions at the storage unit; To exchange the logic of signal flag (such as interrupted signal), etc.

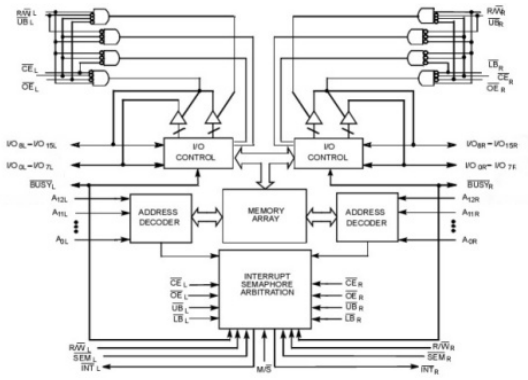

Fig. 1. Dual-port RAM of the electrical structure (CY7C025)

The contention may be occurred when two CPU both read the same unit of dual-port RAM at the same time. It happens data chaos and that the writing and reading data is not what we expect when the contention appeared. In order to prevent the occurrence of the phenomenon, it takes BUSY logic controlled (it is also called by the arbitration logic of hardware address). When the contention happened, the arbitral circuit is able to determine a priority of port to continue to read and write data. The arbitral circuit sets the BUSY pin of another delayed access port to effective (it is low level voltage). External accessing to the port is invalid when the BUSY pin is effective. When the port that has priority completed operation to the controversial unit, the arbitral circuit sets the BUSY pin of the delayed access port to high level voltage. At this time, the delayed port can continue to access data.

In addition, each piece of LF2407A makes use of IS61LV6416 which is 64K ×16bit to constitute 64K external static RAM.VC33 expands a piece of Flash memory which is 128K×16bit at external. And control system employs the CPLD.CPLD can realize the following functions: Chip Enable, Read and Write Enable, I / O configured, etc.

The Principle of Speed Control System

Speed control system can regulate and control two motors at parallel. The schematic diagram of system is shown in figure 2.

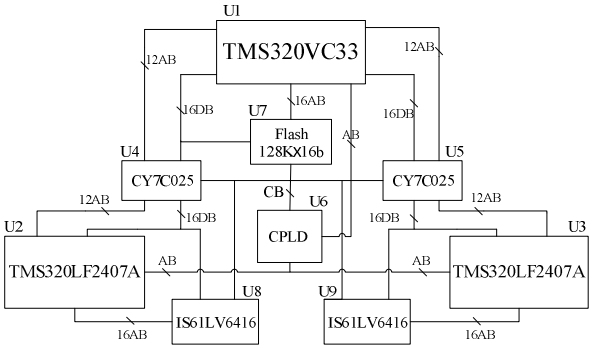

Fig. 2. The schematic diagram of speed control system for controlling two motor

In the speed control system, two pieces of LF2407A mainly control motor and the related peripherals. Each of LF2407A controls a way of motor (as shown in figure 3). In the process of motor speed control system, EV model which is a model of Internal LF2407A outputs 6-channel PWM according to control requirements. This 6-channel PWM can drive the inverter modules by circuit driver. Making the inverter modules exports the asynchronous motor required of voltage and current waveform. LF2407A also acquires analog data such as voltage and current of the control circuit. And the LF2407A passes the data to the dual-port RAM after A/D converter converted. Then the VC33 is triggered by dual-port RAM.VC33 reads data from the dual-port RAM when it received the trigger signal.VC33 calculates the corresponding results according to the control algorithm. And then VC33 transfers the resulting data into the dual-port RAM. After that, dual-port RAM triggers LF2407A.Then LF2407A reads data from the dual-port RAM when it received the trigger signal. LF2407A adjusts the output of the PWM waveform to regulate motor, which is basis of calculation. So it makes the speed control system be able to control the motor accurately and in real time by the kind of collaborative work among those DSP.

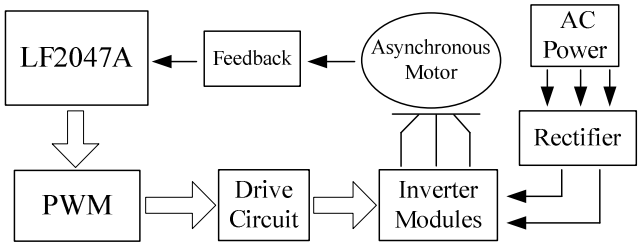

Fig. 3. Block diagram of single motor speed control system

How to make exchange data and communicate smoothly among three DSP is one of key point in this system. And how to solve that it does not conflict when two LF2407A transfer and accept data to VC33.So it needs certain setting for two pieces of dual-port RAM CY7C025. Interrupt scheme which takes advantage of arbitral circuit in CY7C025 and bonds the software of arbitrated program can resolve to this problem very well.

The specific program is: One end of the two BUSY pins of CY7C025 connects to the two READY pins of LF2407A. The other end of BUSY pins connects to the READY pin of VC33. The interrupt pin (INTL, INTR) of CY7C025 are connected to the external interrupt pins of LF2407A and VC33,as shown in figure 4.And CY7C025 reserves two areas which usually are the highest and the second high bit to as the interrupt source of LF2407A and VC33.

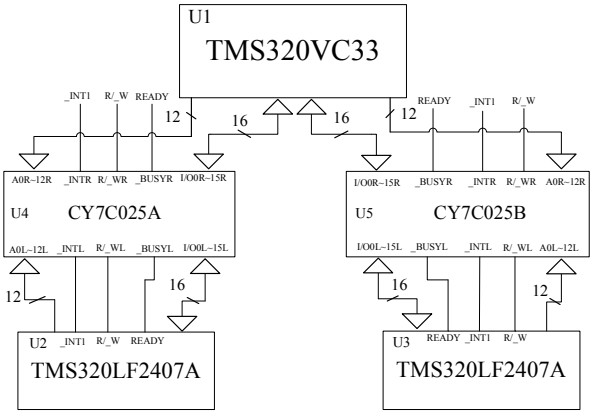

Fig. 4. The interface diagram of between dual-port RAM and DSP

The mechanism of inter-DSP data transferred is: the interrupt source in dual-port RAM triggers the external interrupt of U1 after U2 or U3 transferred the data to the dual-port RAM. U1 read data from the dual-port RAM when U1 received the interrupt signal. But U2 or U3 can't carry out any operation to the same unit at a time. U1 send data to the dual-port RAM after treatment. Then the interrupt source in dual-port RAM triggered the external interrupt of U2 or U3. U2 or U3 read data from the dual-port RAM after receiving the interrupt signal. Likewise, U1 can't carry out any operation to the same unit at a time. Thus it prevents from occurring the conflicts when the ends of DSP exchange data. We can set preferential interrupt to avoid collisions which U2 and U3 transfer data to U1 simultaneously. When U2 and U3 pass data to U1 at the same time, the sequence of data exchanged among U1 with U2 and U3 is decided by the priority of the preferential interrupt.

Another key point of the control system is how to design software. According to the work principle and hardware system, we design corresponding software programs to realize the function. It ensures the system efficient and stable operation. Specific software flow chart is figure 5.

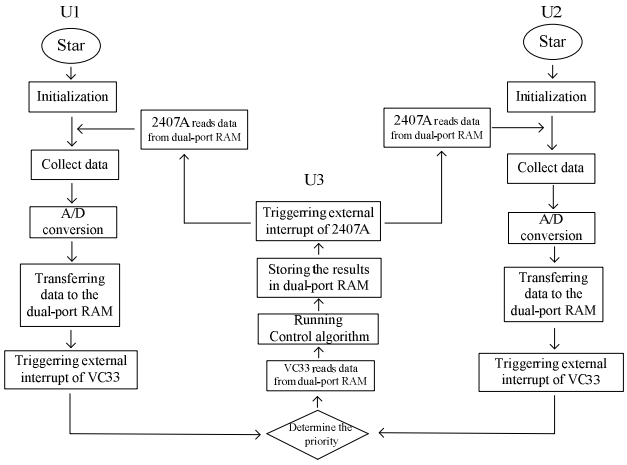

Fig. 5. The software flow chart of the control system

Conclusions

The speed control system based on DSP take advantage of the preponderance of different DSP. The LF2407A and VC33 do clear division of labor. And the DSP are collaborative work. It achieves high performance on multi-motor control. The application of dual-port RAM coordinates communications and data exchange between the DSP well. So that multiple parallel control can be realized.

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References

[1] Zhang Weixiong etc. Principles and Applications of DSP .China Machine Press.(2005)

[2] Wang Xiaoming etc. The Motor Control Base on DSP--TI Introduces the Application of Digital Signal Processor (DSP). Beijing Aeronautics and Astronautics Press.(2005)94-167.

[3] Qiushi technology. A Typical Design Example of the Module of Microcontroller. Posts& Telecom Press.(2004)406-413.

[4] Zhang Yanbin. SPWM Frequency Control Application. China Machine Press.(2006)

[5] Yao Xilu. The Application of Inverter Technology. Electronic Industry Press.(2009)

[6] Li Yongdong. AC Motor Digital Control System. China Machine Press.(2002)

[7] Power Electronic and Electric Drive Automation-Compilation of Important Papers of Prof. Chen Boshi. (2008)144-149.

[8] Liu Deming. Using Dual-Port RAM Achieve High-Speed Data Communication Between the DSP. National Defense University.

[9] Lin Lihua. Motor Control System Controlled by Double-DSP. Nanjing University of Aeronautics and Astronautics