Efficient Neural-Based Large-Signal and Isothermal Models for the Dual Gate MESFET

M. Abdeen and M.C.E. Yagoub

School of Information Technology and Engineering, University of Ottawa, 800 King Edward, Ottawa, Ontario, Canada K1N 6N5
mabdeen@alumni.uottawa.ca, myagoub@site.uottawa.ca

Abstract: This paper presents neural-based large-signal and isothermal models for the dual gate MESFET as efficient alternatives to existing nonlinear models for such a complex device. The developed neural model is a combination of two sub-models; a static model represented by DC current-voltage characteristics and a dynamic model represented by pulsed current-voltage characteristics. The isothermal model is based on pulsed current-voltage measurements to better represent the RF device behavior and to neutralize the effect of channel self-heating on model accuracy. Insights on the discrepancy between model parameter values extracted from pulse and from DC current-voltage measurements are also discussed. The measurement and model data are in very good agreement with global model errors of less than 1%.

Key words: Modeling, dual-gate transistors, MESFET, isothermal model, neural networks, nonlinear circuits.

INTRODUCTION

The evolution of today’s RF/microwave communication systems is due in great part to the development of more advanced and efficient active devices. Transistors such as BJTs, FETs, and HEMTs are fundamental components in today’s personal, corporate and global communication systems.

The single gate Metal-Semiconductor Field Effect Transistor (MESFET) is one of the most popular active devices with wide areas of RF/Microwave applications. The dual-gate MESFET (DGFET) is a variation of the single gate with a second gate between the first gate and the drain. Its advantages over the single gate of comparable size include higher gain, better input gate-to-drain isolation, and higher output impedance. That made it attractive for various nonlinear applications such as mixers, frequency multipliers, and power combiners and splitters. Despite the existence of some modeling work for the dual-gate MESFET, there is a need to develop more efficient, accurate, and faster nonlinear modeling methodologies.

Most existing MESFET large-signal models use DC current-voltage measurements. Device parameters such as the transconductance and the output conductance are then extracted from that model. However, the values obtained from DC current-voltage based models were not with a good agreement with their counterparts obtained from RF S-parameter measurements.

This is due to low frequency dispersion, self-heating, and trap effects. Many MESFET researches [PAG 88] [FIE 95] [KOH 02] have shown that pulsed current-voltage characterization renders better device parameters than the ones produced by DC current-voltage ones.

Paggi et. al. [PAG 88], for example, showed that the values of the output resistance, R_o, extracted directly from pulsed current-voltage curves are much closer to the actual microwave values than the value taken from DC current-voltage curves. Pulsed measurements are, therefore, preferred if more accurate large-signal device characterization is desired.

The drain current is the most important non-linear component in the dual-gate FET model. Existing dual-gate FET drain current models, with the exception of [JEN 99] and [IBR 03], are based on considering the device as two single-gate FETs connected in cascode. This approximation did not result in a good agreement between the simulation and the measurement data.

In the model developed by Jenner [JEN 99] the nonlinear drain current is represented by a three-dimensional power series. However, obtaining good accuracy can require as many as 165 parameters. Moreover, the model is generated from DC measurements and does not take into account the frequency dispersion of the transconductance and the output conductance.

On the other hand, although the model developed by Ibrahim et. al. [IBR 03] required only 49
parameters, it still present a significant amount of model extraction efforts. Moreover, modeling the RF current component required the extraction of the transconductance from three-port S-parameter measurements. This experimental process presents a fairly complex and costly process.

Neural modeling of devices and circuits is one of the most recent trends in microwave CAD. Fast, accurate and reliable neural network models can be trained from measured or simulated data. Once developed, these neural models can be used in place of CPU-intensive physics/EM models of active/passive devices to speed up microwave design. Neural network (NN) techniques have been used to model a wide variety of microwave devices and circuits [HAY 99] [ZHA 00] [DEV 02] [XU 02] [ABD 03] with significant successes.

To address these issues, we present in this paper two efficient neural-based models of the dual gate transistor. The nonlinear model is a combination of a static model generated from DC current-voltage characteristics and a dynamic model represented by pulsed current-voltage characteristics. The isothermal model is based on pulsed current-voltage measurements to better represent the RF device behavior and to neutralize the effect of channel self-heating on model accuracy.

We also present insights on the discrepancy between model parameter values extracted from pulse and from DC I-V measurements to complete our modelling approach.

1. The nonlinear model

The dual-gate MESFET drain current model developed in this work has two components, a DC and an RF component.

Static current component is modeled using the DC current-voltage characterization. For the RF component, however, dynamic characterization is required. Most published work on the single and dual-gate FET approximates the dynamic behavior of the device with the static current-voltage curves. This results in significant errors in calculating the trans- and output conductances of the device. Pulsed measurements, on the other hand, provide a better representation of the RF large-signal behavior of the transistor [FER 96]. The total drain current is given by [IBR 03]

\[
I_{ds} = I_{ds}^{DC} h(f) + I_{ds}^{RF} (1 - h(f))
\]  

(1)

where \(I_{ds}^{DC}\) is the DC component of the drain current, \(I_{ds}^{RF}\) is the RF component, and \(h(f)\) is a function that ensures a smooth transmission from DC to RF characteristics. For the model developed here, and for simplicity, \(h(f)\) is chosen to be the unit-step function, i.e., the model represents either the DC or the RF current model

\[
h(f) = \begin{cases} 
0 & f = 0 \\
1 & f > 0
\end{cases}
\]  

(2)

where \(f\) is the frequency. The DC current is a function of the static potential of the two gates and the drain, \(V_{gs1}, V_{gs2},\) and \(V_{ds}\) respectively. On the other hand, pulsed current-voltage characteristics depend on the bias point as well as the pulse amplitudes applied [LAZ 01]. Therefore, the RF drain current is a function of the bias point \((V_{gs1}, V_{gs2}, V_{ds})\) as well as the pulsed voltages \((V_{pg1}, V_{pg2}, V_{pd})\) applied over the bias point. In other words:

\[
I_{ds}^{DC} = I_{ds}^{DC} (V_{gs1}, V_{gs2}, V_{ds})
\]  

(3)

\[
I_{ds}^{RF} = I_{ds}^{RF} (V_{gs1}, V_{gs2}, V_{ds}, V_{pg1}, V_{pg2}, V_{pd})
\]  

(4)

The NN model generation process starts by assuming an initial model configuration. The “universal approximation theorem” states that a multilayer preceptron network (MLP) can approximate any arbitrary multidimensional function [HOR 89]. We started with a three layer neural network. The number of layers and neurons per layer are then changed until a satisfactory model training error is reached. Measurement of data points are performed such that they cover the desired parameter range. The obtained data is divided into two sets, training and testing/verification set. The testing/verification data set is independent from the training set (never used in training).

2. Results for the nonlinear model

We have modeled a 1x1.5x400μm GaAs dual-gate MESFET. Pulsed and DC measurements are performed by a programmable DC/pulse measurement setup depicted in Fig. 1. This pulse arrangement is suitable for GaAs device measurements to avoid channel self-heating effects. Each measurement set is performed in a separate session. For the DC measurements, the bias range for the two gate voltages is \(-1.0 \sim 0.25V\) (steps of 0.25V) while that of the drain voltage is \(0 \sim 8V\) (in steps of 0.25V). For the pulsed measurements, the DC bias point is scanned from

\[(V_{gs1} = -1.0V, V_{gs2} = -1.0V, V_{ds} = 0.0V)\]

to

\[(V_{gs1} = 0.2V, V_{gs2} = 0.2V, V_{ds} = 5.0V)\]
in steps of

\( \Delta V_{gs1} = 0.3V, \Delta V_{gs2} = 0.3V, \Delta V_{ds} = 1.0V \).

The drain and the gates are pulsed simultaneously. The pulsed gate voltage levels are varied from -1.0 to 0.2V (in steps of 0.3V), while the drain pulsed voltage levels are varied from 0 to 8V (in steps of 0.4V). The drain current was averaged over many reading points under the same measurement conditions. This is all software programmed from a software user interface. The width of pulse is 1μs with pulse separation of 1 ms (a duty cycle of 0.1 %).

2.1. The DC neural model

The neural model generation process starts by assuming an initial configuration of the multilayer perceptron network [ZHA 00]. Using NeuroModeler [NEU 01], we started with a three-layer neural network. We then changed the number of layers and neurons per layer until an optimal model is reached. The DC neural model developed here is a three layer. We found no significant improvement of the model accuracy if more layers are used since the model is relatively simple. Ten hidden neurons were sufficient to obtain a very good accuracy of less than 1%. The input layer has 3 input parameters, the static voltages, \( (V_{gs1}, V_{gs2}, V_{ds}) \). The output layer has one output, the DC drain current, \( I_{ds}^{DC} \). Fig. 2 shows the measured and modeled data at \( V_{gs2} = 0.0V \) for different gate voltage \( V_{gs1} \).

2.2. The RF neural model

The RF current model developed in this work consists of four layers; one input layer, one output layer, and two hidden layers. The input layer has 6 input parameters, the static voltages, \( (V_{gs1}, V_{gs2}, V_{ds}) \), and the dynamic voltages \( (v_{gs1}, v_{gs2}, v_{ds}) \). The output layer has one output, the RF drain current, \( I_{ds}^{RF} \). The total number of hidden neurons is 15, i.e. 9 and 6 neurons for the first and second layer respectively. An illustration of the neural model structure is shown in Fig. 3. Figs. 4, 5, and 6 show the measured and modeled pulsed data for the dual-gate FET for various DC and pulsed voltages. The model shows very good fitting of the data. The model error is less than 1%.
2.3. The large-signal drain current neural model

The large-signal drain current neural model is a combination of the two individual neural submodels developed in the previous two sections, i.e., the DC and RF neural models (Fig. 7).

Before training, the measurement data is first randomized. It is then split into training and testing/verification parts. This step is important to ensure the model training and testing/verification data are well spread in the data range of interest. About 70% of the measurement data points are used to train the model. The remaining 30% data points are used in model testing/verification. Back-propagation with quasi-Newton algorithm is used for model training. The final model showed a very good agreement between the simulations and the measurement data. The average model error was less than 1%. The overall model generation takes only a few minutes on a typical computer.

It is to be noted that the pulsed current-voltage characteristics do not show a negative output resistance effect. This effect is mainly due to the channel self-heating variation with the DC bias. The pulsed characteristics are iso-thermal (have a fixed DC bias current) and hence the channel temperature is constant for one given set of bias points. In addition, the pulsed current-voltage characteristics change appreciably with the DC drain bias. As the DC drain bias increases, the drain saturation current decreases and the knee of the curve moves closer to the zero drain voltage. Similar effects have been noticed for the single gate FETs.

3. The isothermal model

3.1. The pulsed DC model

To develop an isothermal model, we used an on-wafer 6 gate 1x1x600 μm dual-gate MESFET
manufactured by Nortel Networks, with the same experimental setup shown in Fig. 1. The pulsed voltage of the lower gate \((G_1)\) is varied from -1.0 to 0.5 V (step of 0.3V), while the drain voltage levels are varied from 0.0 to 6.0 V (step of 0.2V). The upper gate \((G_2)\) is DC biased from -0.7V to 0.5V in steps of 0.3V. The width of pulse is 1μs with pulse separation of 1ms (a duty cycle of 0.1 %).

This pulse arrangement is suitable for GaAs device measurements to avoid channel self-heating effects. The pulse measurements are performed at a DC bias point of \((V_{gs1}, V_{ds}) = (-1.0V, 0.0V)\), i.e. under zero DC power dissipation. About 75% of the pulsed measurement data is used in model training while the remaining 25% is used for model testing.

A similar neural model is also generated using DC measurement data. Fig. 8 shows measured and modeled values of both pulsed and DC current-voltage curves for the dual-gate MESFET for different values of \(V_{gs1}\) while the second gate voltage \(V_{gs2}\) is fixed at a value of 0.5 V.

### 3.2. discrepancies between DC models

It is to be noted that DC and pulse neural network models produce a very good fit with measurements. Also, there is a significant difference between the pulsed and the DC drain current although under the same numerical value of the gate voltages. DC drain current can cause channel self-heating which causes early mobility saturation and therefore lesser DC current. This effect is significantly minimized in models based on pulsed measurements since the pulse width is chosen small enough to avoid overheating the channel. Under pulse measurements, the device operates at a constant (or zero) DC drain current and therefore a constant power dissipation. Under such conditions the device temperature is constant and the model is therefore isothermal. The dual gate MESFET transconductances \(g_{m1}\) and \(g_{m2}\), and the output conductance \(g_{ds}\) are defined as

\[
\begin{align*}
g_{m1} &= \frac{\partial I_{ds}}{\partial V_{gs1}} \bigg|_{V_{gs2}, V_{ds}}, \\
g_{m2} &= \frac{\partial I_{ds}}{\partial V_{gs2}} \bigg|_{V_{gs1}, V_{ds}}, \\
g_{ds} &= \frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{V_{gs1}, V_{gs2}}.
\end{align*}
\]

Published works on the single-gate FET showed discrepancies between the values conductances obtained from DC and those obtained from pulsed measurement. To investigate this effect for the dual-gate FET, differentiation of the neural analytical expression for both the pulsed and DC drain current is performed as per (5). Mathematical manipulation is done symbolically using Maple [MAP 01].

Fig. 9 and Fig. 10 show the difference between the pulsed and DC values of \(g_{m1} (\Delta g_{m1}/g_{m1, DC})\) and \(g_{ds} (\Delta g_{ds}/g_{ds, DC})\), respectively.

![Fig. 8. Pulsed current-voltage curves (•: measurement, –: modeled) and DC current-voltage curves (A: measurements, ---: modeled) for the Nortel dual-gate FET \((V_{gs2} = 0.5\text{ V})\).](image)

![Fig. 9. Variation of the transconductance \(g_{m1}\) (in %) with the gate voltage \(V_{gs1}\) and the drain voltage \(V_{ds}\).](image)

From these Figures we note that the reliance on DC current-voltage measurements to produce small-signal parameter values can result in an error of up to 40% in the case of transconductance and an error over 100% for the case of the output conductance. This demonstrates the significant advantage presented by pulsed measurements.
Fig. 10. Variation of the output conductance $g_{ds}$ (in %) with the gate voltage $V_{gs1}$ and the drain voltage $V_{ds}$.

4. Conclusions

In a first step, we have presented a large-signal drain current neural model for the dual-gate MESFET along with a pulsed isothermal model. The static behavior of the device is represented by the DC current-voltage characteristics while the RF behavior is modeled using pulsed current-voltage measurements at different bias points. The model generation is relatively fast (a few minutes on a typical computer). This model paves the way to including the device model, and for the first time, in commercial circuit simulators (e.g. ADS [ADS 03]) with the help of user defined model capability. This is a topic of future research. In a second step, we have developed an isothermal neural network approach for large-signal modeling of the drain current for the DG MESFET based on pulsed current-voltage measurements.

Neural nonlinear approach presents an efficient alternative for modeling devices as complex as the dual-gate MESFET. The use of pulsed current-voltage measurement rather than the DC ones allowed for the minimization of dual-gate channel self-heating effects. Percentile differences of small signal parameter values obtained from the pulsed and the DC current-voltage measurements (such as $g_m$ and $g_{ds}$) were shown to be as much as 100%.

ACKNOWLEDGMENT

The authors would like to thank Dr Jeff Bennett with Nortel Networks for his advices and technical support. This work is supported in part by the Natural Science and Engineering Research Council of Canada.

REFERENCES


[MAP 01] Maple 8.01, Maple Inc., Waterloo, ON, Canada.

[NEU 01] NeuroModeler 1.2, Q.J. Zhang, Department of Electronics, Carleton University, Ottawa, ON, Canada.

