Simulation and Analysis of Dual Gate Organic Thin Film Transistor and its inverter circuit using SILVACO

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Abstract:-This research paper represents the simulation and analysis of Dual Gate Organic Thin Film Transistor (DG-OTFT). All the simulations have been carried out using SILVACO TCAD tool. Its performance have analysed on the basis of parameters, which were extracted from its transfer characteristics. DG-OTFT has shown improved electrical performance as compared to single gate OTFT. Furthermore, DGOTFT based organic inverter circuit has been simulated in its zero –Vgs-load logic (ZVLL) configuration. It has been observed that DGOTFT results in improved noise margin in its ZVLL configuration.

Keywords: ATLAS simulator, dual gate OTFTs, organic inverters, organic thin film transistors, SILVACO, ZVLL.

I. INTRODUCTION:-
THIN-FILM TRANSISTORS (TFT’s) using organic semiconductors as the active material have made an impressive progress in terms of light weight, flexibility, and low cost as compared to other semiconductors. Due to above reasons the imposition of organic thin film transistors (OTFT) are increasingly likely. OTFT will find application, not only in displays, but also to integrate logic circuitry and memory arrays into low cost electronic products such as smart cards, smart price and inventory tags, and large-area sensor arrays.[1,2] This paper deals with analysis of dual gate OTFT’s structures using 2-D ATLAS simulator. A simulation is done on electrical characteristics and performance of dual gate OTFTs. Thereafter dual gate OTFT structure is used to design a circuit of inverter. Most of the organic inverter circuits make use of p-type designs only, due to lower mobility and instability of their n-type counterpart. The n-type transistors are more sensitive to oxygen, air and moisture than p-types. The static and dynamic behaviours of organic inverters in zero-Vgs-load logic (ZVLL) configurations are analyzed using dual gate (DG) organic transistors. It is observed that DG based inverters under different configurations outperforms the SG ones. The organisation of paper is as follows. The present section introduces the content of paper. Thereafter, section II analyzes pentacene based DG-OTFT device design. Device Simulation and performance parameters extraction are explained in section III while in section IV, behavior of p-type organic inverter circuits in ZVLL configurations are dealt in and finally result and discussion is drawn in section V and conclusion is drawn in section VI.

II. DUAL GATE OTFT DEVICE DESIGN.
An organic field-effect transistor (OTFT) is a Field-effect transistor using an organic semiconductor in its channel. Like MOSFETS, OTFT have symmetrical structures that are source and drains are interchangeable. In Dual gate organic thin film transistors (DGOTFT) the active semiconducting layer is sandwiched between two gate electrodes from which it is electrically isolated by two gate insulators. The fundamental principles of the operation of the dual gate organic thin film transistors (DGOTFT) do not differ from that of a common OTFT. In a single gate OTFT the charges are induced by the gate potential at the semiconductor/insulator interface forming a conducting channel. The formation of the channel creates a conducting path between the source and drain electrodes. It also screens the gate potential similar to the operation of a plate capacitor. The dual-gate OTFTs were characterized in double gate mode by sweeping the bottom gate bias voltages from positive to negative while fixing the top gate potentials, and vice versa.

![OTFT Schematics with two gated structure(DG-OTFT).](image-url)
The change in the threshold voltage of the bottom gate depends on the top gate bias. There are two working regions of DG-OTFTs. When one of the gate is made positive, the respective channel is in depletion and no gate screening will occur, while the other gate will be in accumulation regime, the field of the positive gate will penetrate to such a large extend that the channel in accumulation will be affected by both gates. When both channels are in accumulation, the charges present in the channels will screen the respective gate potentials, hence both channels will operate individually and no mutual influences are observed.

For a dual-gate OTFT with its top channel in accumulation, a drop in the transconductance was demonstrated when the bottom gate potential becomes negative. The transition regime between both linear regimes is marked by a drop in the transconductance, where the bottom channel depends on the bottom gate only and the top channel will depend on both gates. The transition regime results from the fact that the charges accumulated in the bottom channel will start to screen the influence of the bottom gate potential on the top channel. The change in drain current will depend only on the change of the current of the bottom channel [3-7].

III. DEVICE SIMULATION & PARAMETERS EXTRACTION.

A 2-D ATLAS simulator of Silvaco Company is used as a semiconductor simulator. We have used an active layer of pentacene which is a p-type organic material 150-nm thickness in DGOTFT respectively. We assumed an active layer of pentacene with 150-nm thickness. We assumed that \( \mu_0 \), activation energy (\( \Delta E_a \)), and \( \beta \) are 0.62 cm\(^2\)V\(^{-1}\)s\(^{-1}\), 0.018 eV, and \( 7.7 \times 10^{-5} \) eV (V/cm)\(^{1/2}\), respectively. The calculation was done with a one-carrier model of the hole. The gate insulator was assumed to be SiO\(_2\) with a dielectric constant of 3.9 and a thickness of 100 nm. The channel length was set to 100 \( \mu \)m, which is long enough to avoid short-channel effects, and the channel width was assumed to be 800 \( \mu \)m. Source and drain length were taken of gold of 52.5nm thickness.

![Fig. 2. Output characteristics of DG-OTFT](image1)

![Fig.3. Transfer characteristics of DG-OTFT](image2)
Table-I. Extracted Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>DGOTFT</th>
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<tbody>
<tr>
<td>$V_{th1}$ (V)</td>
<td>-15.97832</td>
</tr>
<tr>
<td>$V_{th2}$ (V)</td>
<td>-15.97832</td>
</tr>
<tr>
<td>$I_{on}/I_{off}$</td>
<td>2.23179e+13</td>
</tr>
<tr>
<td>$g_m$ (A/V)</td>
<td>7.0598e-007</td>
</tr>
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</table>

Figure-2 gives output characteristics of DG-OTFT at different gate voltages. Figure-3 gives transfer characteristics of DG-OTFT which shows dual gate draws current at zero gate voltage ($V_{gs} = 0$V). Performance parameters such as threshold voltage ($V_{th}$), transconductance ($g_m$), current on-off ratio ($I_{on}/I_{off}$), are extracted from transfer characteristics which is given in table I. The extraction shows higher transconductance ($g_m$) and $I_{on}/I_{off}$ ratio of dual gate structure which proves to be better devices for switching applications.

IV. ORGANIC INVERTER CIRCUIT.

This section investigates the performance of organic p-type inverter circuit in ZVLL configurations, using dual gate organic thin film transistors as shown in Figure.4. These configurations are simulated under mix-mode, wherein, each input file is split into two parts; one describes the circuit net-list, and the other explains device simulation and model parameters [8].

Fig. 4. Schematics of organic inverter circuits with dual gate OTFTs in ZVLL configuration.

In ZVLL configuration, source and gate terminals of the load are connected such that, it behaves as a constant current source that produces higher gain and noise margins as compared to other inverters configuration. In this logic, enhancement and depletion mode operations are required for driver and load transistors, respectively. A biasing voltage, $V_{dd}$ of 10 V is applied and output voltage, $V_{out}$ is obtained at the drain terminal of the driver for an input supply, $V_{in}$ swept from 0 to 10 V. In this configuration, driver width ($W_D$) is kept at 2000 μm, whereas, a width ($W_L$) of 400 μm is considered for load. In order to analyze the dynamic behavior, a pulse of 0–10 V at a frequency of 1KHz is applied at the input terminal, as shown in figure below[9-11].
Fig. 5. Transient response of dual gate organic inverters in ZVLL configurations at 1 KHz input. The figure 5 shows inverted characteristics obtained at the output with given input pulse at 1 KHz frequency.

Fig. 6. Voltage Transfer Characteristics of dual gate organic inverter

Voltage transfer characteristics (VTCs) of dual gate inverters are depicted in Figure 6. The output high voltage, $V_{OH}$ should be high enough to achieve the higher noise margins. However, it attains lower magnitude due to threshold voltage drop in the load transistor[12].

Here $V_{OH} = V_{dd} - V_{tL}$

Where, $V_{tL}$ is the threshold voltage of load transistor.

Table-II: Extracted Parameters In Inverters

<table>
<thead>
<tr>
<th>$V_{OH}$(V)</th>
<th>$V_{OL}$(V)</th>
<th>OUTPUT SWING (V)</th>
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</thead>
<tbody>
<tr>
<td>9.2</td>
<td>1.6</td>
<td>7.6</td>
</tr>
</tbody>
</table>
V. RESULTS & DISCUSSION
Dual gate organic transistor exhibited superior performance in terms of $I_{ds}$, $I_{on}/I_{off}$ and $g_m$ as seen in table I. Also, table II depicts that dual gate based organic inverter shows increased noise margin. Based on the observation carried out among different types of inverter circuits, it can be concluded that for better performance and circuit designing onto flexible substrates, it is advisable to integrate fully organic complementary inverter. But then, it is essential to optimize the devices with higher and comparable mobility to obtain lower propagation delay and good balance between pull up and down operations at lower W/L ratios.

VI. CONCLUSION
In this paper performance of DG-OTFT and DG-OTFT based organic inverter has been analysed. It can be concluded that dual gate OTFT has shown superior performance in terms of saturation current due to formation of two conducting channels and also dual gate based organic inverter has shown improved voltage swing. Therefore, it can be concluded that dual gate is more suitable for applications in large area of electronics.

REFERENCES


