Realizing the Benefits of Structural Test for Intel Microprocessors

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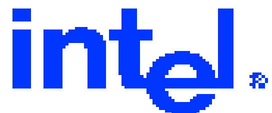


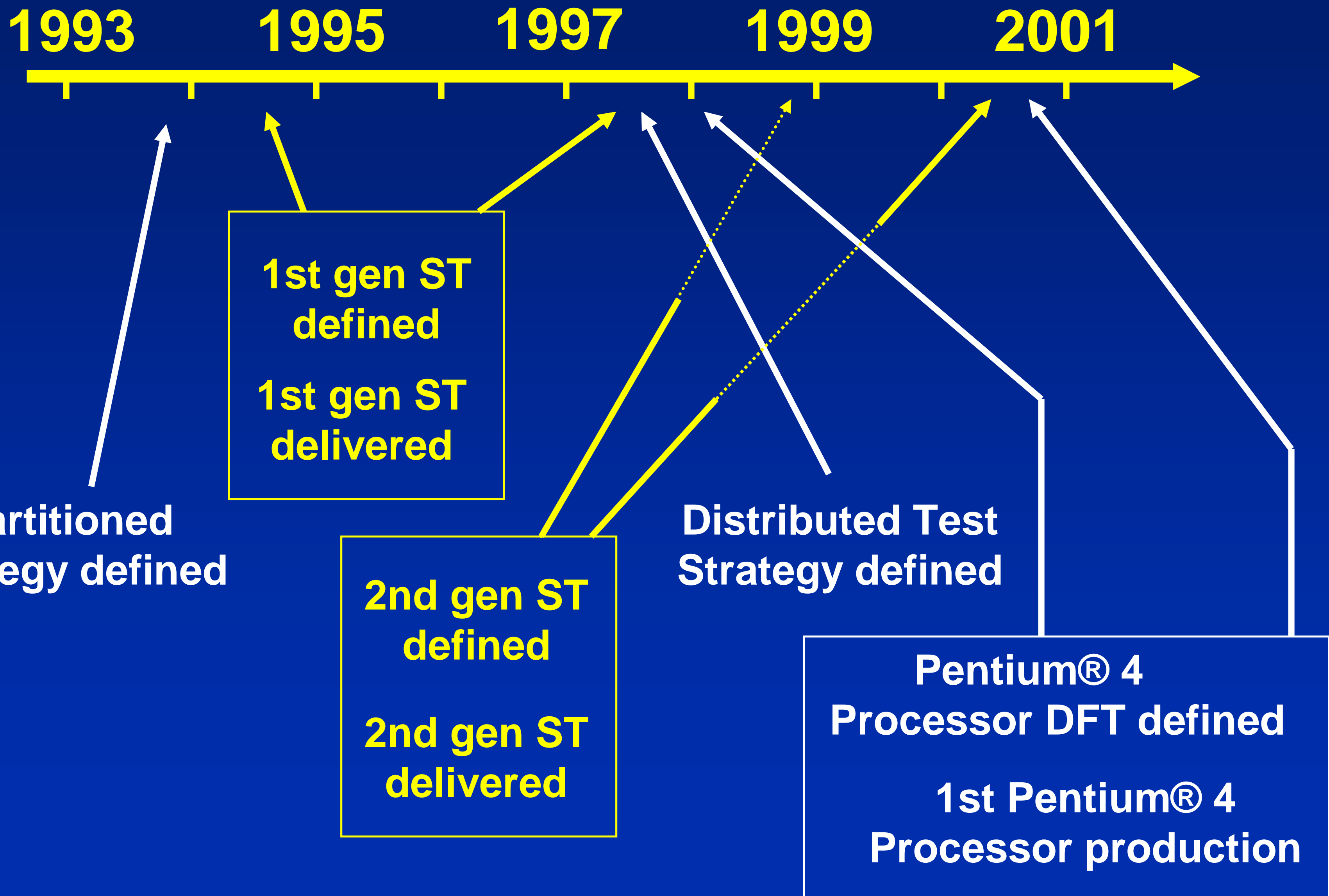
Purpose of Work

- Get off CPU functional testing / tester treadmill
- Optimize product - content - testers for cost
- Risk manage test quality during migration

Outline

- Timeline Overview
- 1st and 2nd Generation Structural Testers
  - Architectural Choices
  - Expected Test Content and Flow
- Data from Pentium® 4 Processor
- Future Trends

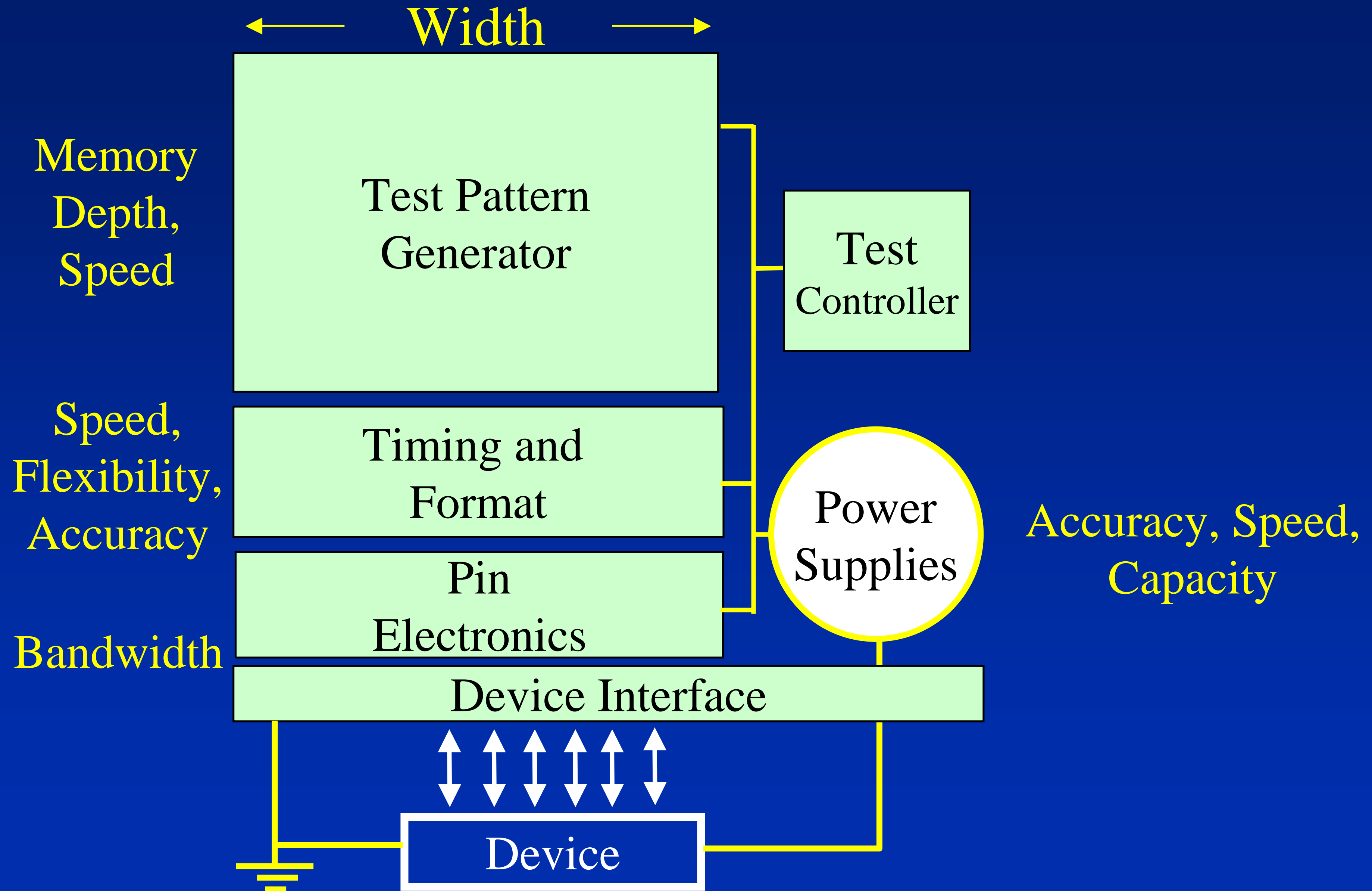
Migration is a Process, not an event



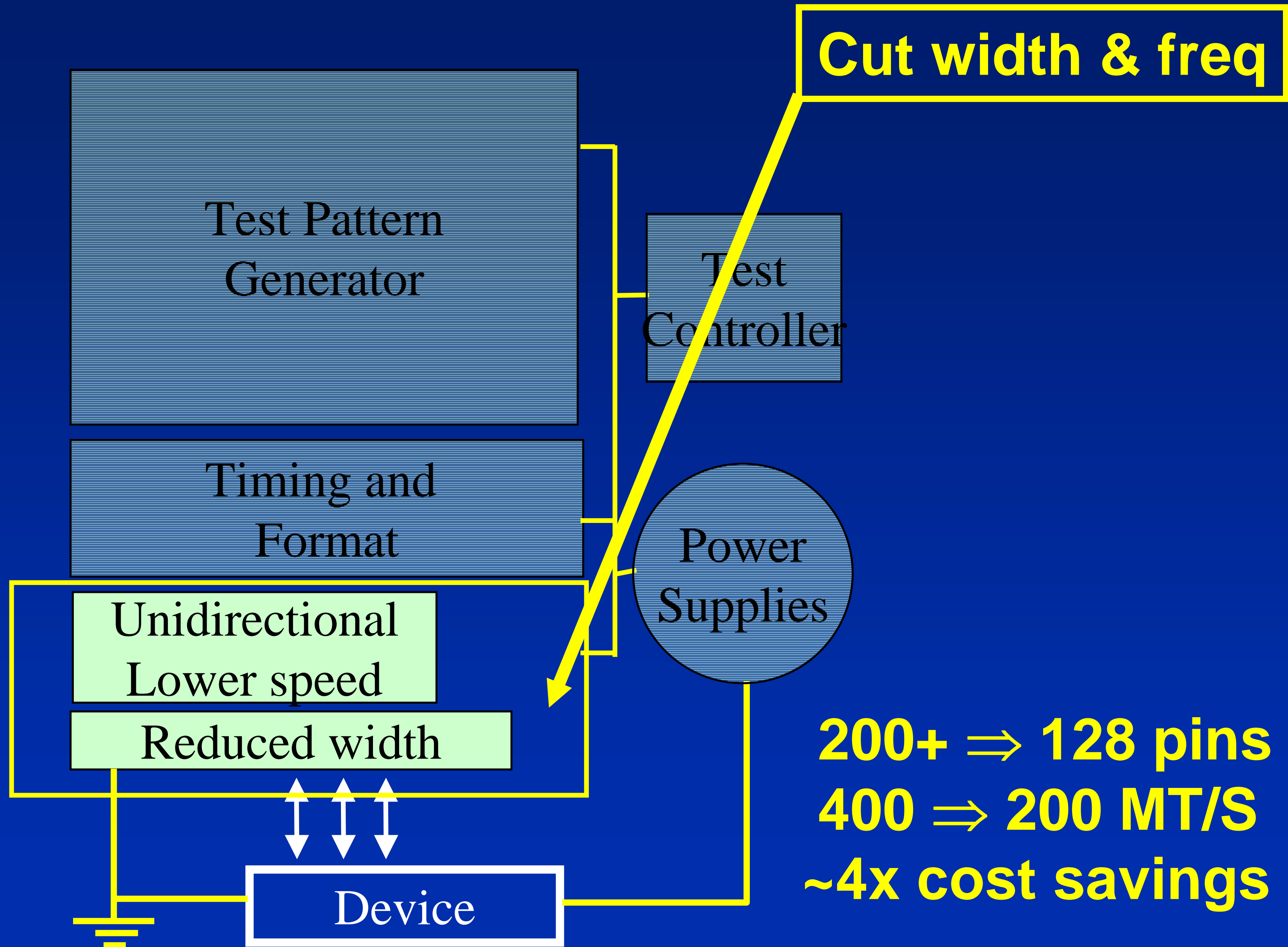
Definition of 1st Gen Struc Tester

- Key Goals
  - Get off treadmill for higher speed testers
  - Achieve lower cost by reduced capability
    - Plan for ST to run only scan + memory tests
  - Enable parallel testing
- Consider but rejected
  - Adding scan to FT — still on treadmill
  - Eliminate FT entirely — test quality risk

Architectural Choices for ST



Architectural Choices

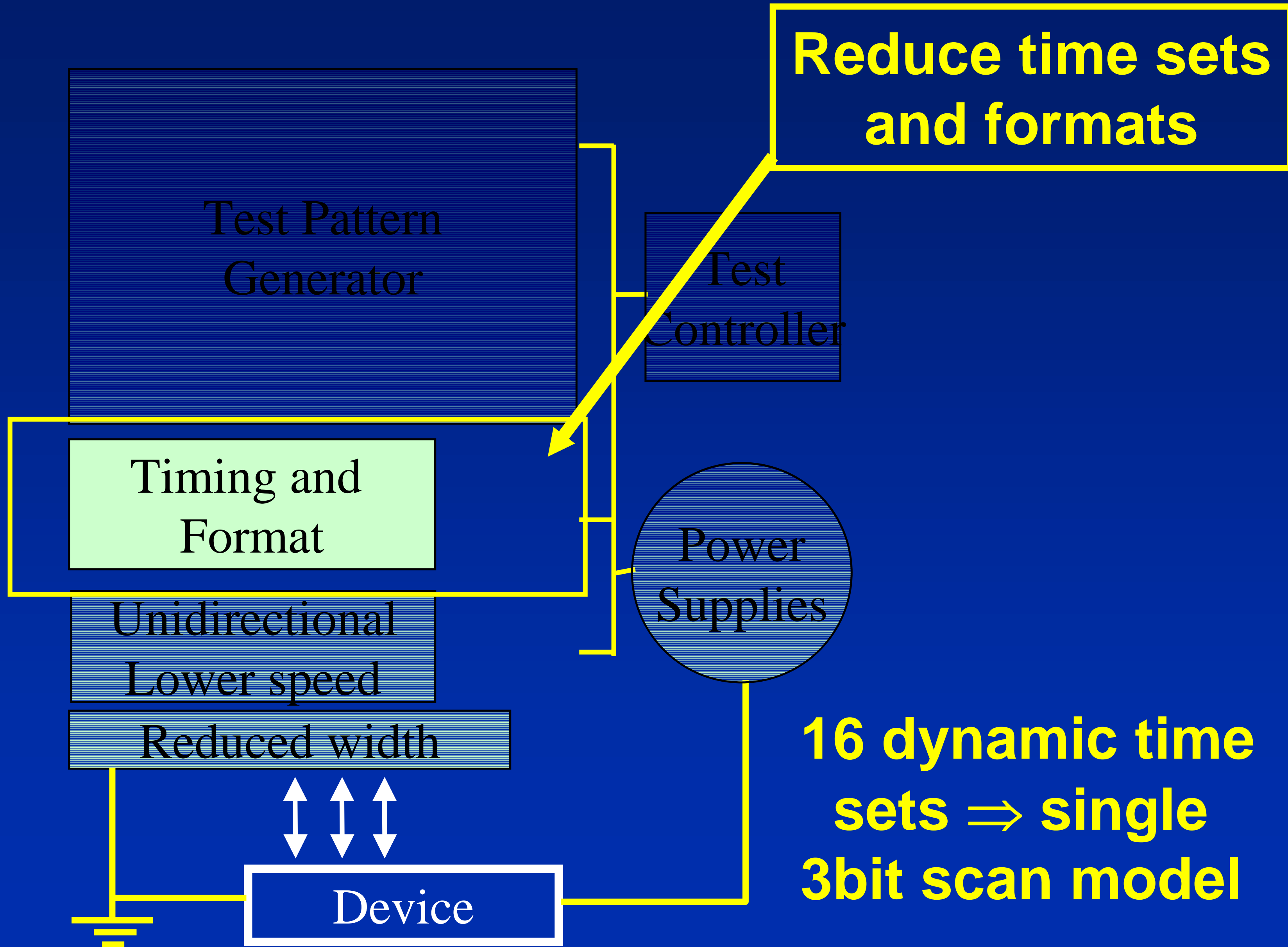


Testability Port

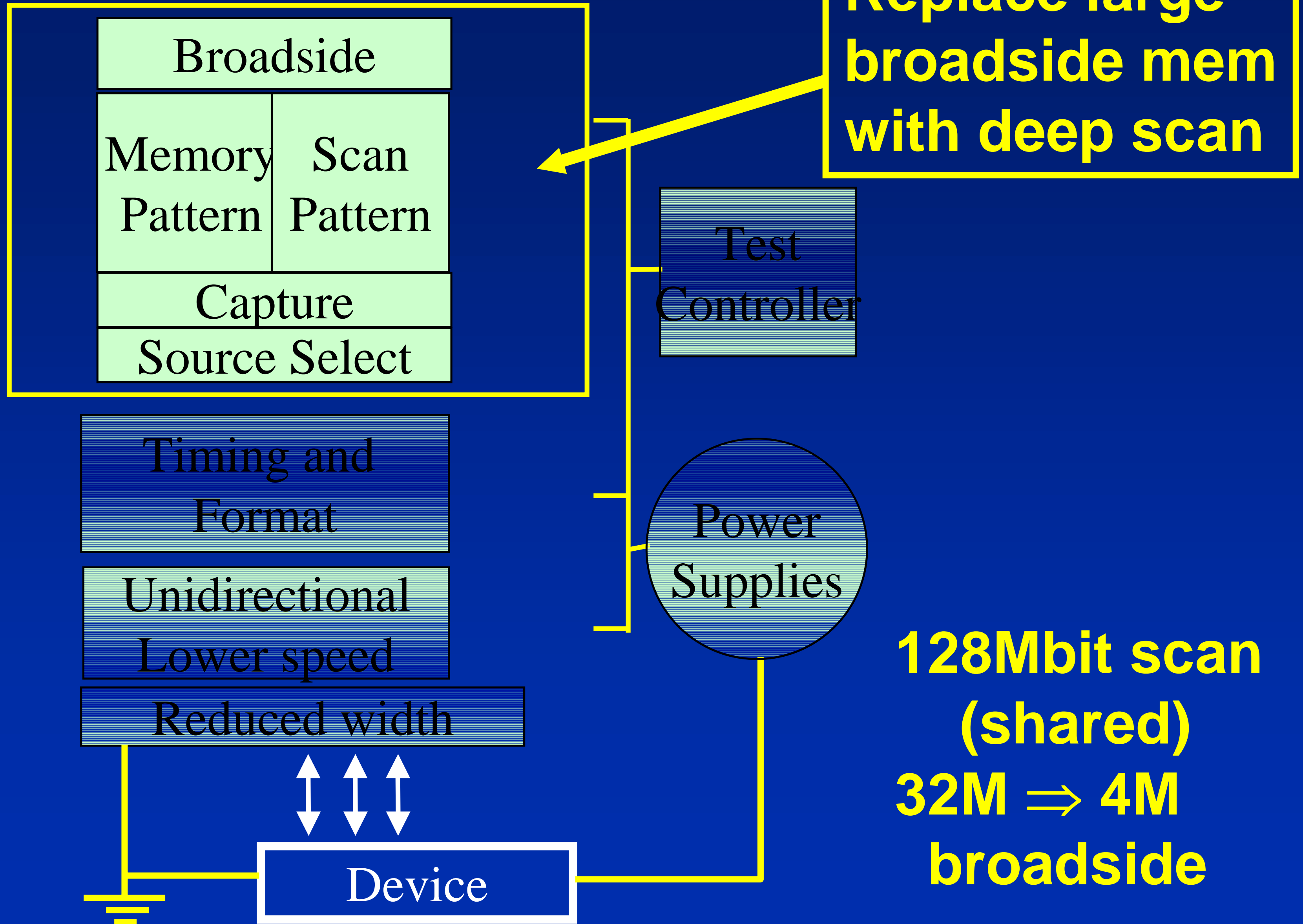
Function	Capability	Pin Count
Scan inputs	200 MT/S, 1nS	36-48
DUT outputs	200MT/S, "	36-48
Array address	200MT/S, "	Up to 36
Array data inputs	200MT/S, "	Up to 36
Control & JTAG	200MT/S, "	24
Clocks	200MHz, 300pS	Up to 4
Total		128-152

Compatibility Enforced at Product Design

Architectural Choices



Architectural Choices



Definition of 1st Gen Struc Tester

- Key Goals
  - Get off treadmill for higher speed testers
  - Achieve lower cost by reduced capability

    Plan for ST to run only scan + memory tests
  - Enable parallel testing
- Key Definition Features
  - 128 pin testability port
  - N-1 generation tester interface speed
  - Deep and shared scan memory
  - APG running at full interface speed **(see paper)**

Evolving Outlook for Content

OLD VIEW   Partitioned testing (Early 90's)

- Scan + memory testing on structural tester
- Full chip vectors on functional tester

NEW VIEW   Distributed Test (1997+)

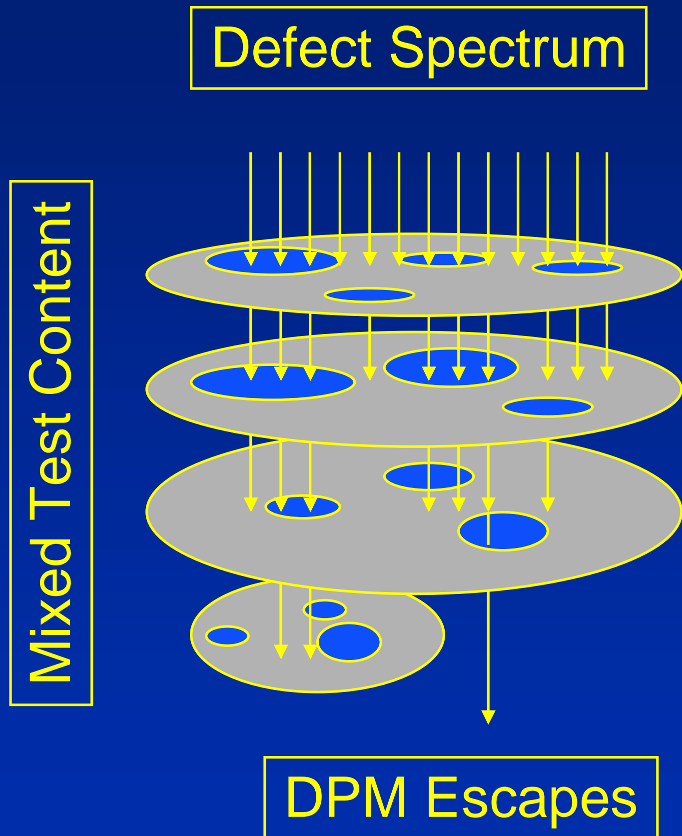
- More and varied defect types to detect
- Multiple content types on multiple platforms

  Functional on Func, Structural on Struc

  + Func content on structural tester

  + Struc content on functional tester

Segmented Test Content



- Defect Based Self-Test on Structural Tester
- Defect Based Off-chip on Structural Tester
- Functional Self-Test on either ST or FT
- Full chip vectors on Functional Tester

Distributed Test Platforms

Wafer Test **Package Test**

Structural Sort	Burn-In	Struc Class	Func Class

Structural Sort:
128pin, 200MT/s
Tight T/V/F control
Cover hard defects

Burn-In:
4pin, 75 MT/s
Loose T/V/F control
Time intensive tests

Struc Class:
128pin, 200MT/s
Tight T/V/F control
Hard + Soft defects
Some speed tests

Func Class:
Full pin, full spd
Tight T/V/F control
Soft defects + speed
Minimize test time

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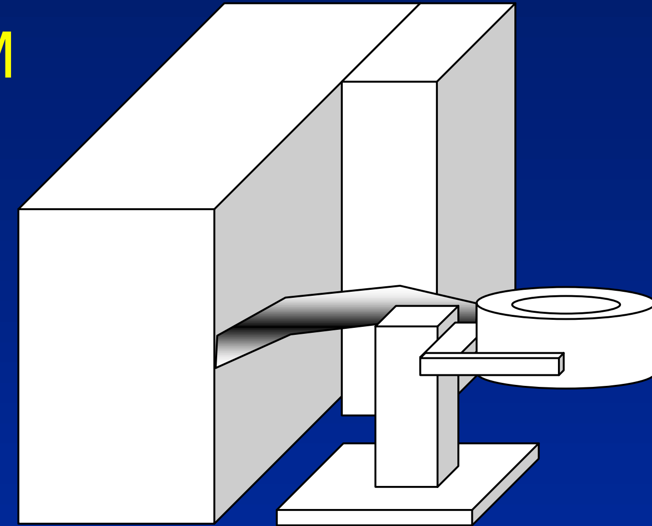
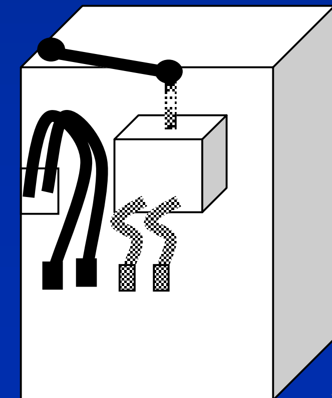
Define partioning based on economics, not capability
Segmentation enables FT reuse

New Architectural Choices for ST2

- Increase flexibility for mixed content
  - Large Vector Mem increase to 16M
  - Parameter passing to SVM
  - Bidirectional pins
  - 1GBit scan memory depth
- Move pin drivers to mainframe
  - Not needed for interface speed
  - Higher level of board integration
  - Test head contains only power supplies
- Outcome
  - 2x reduction in space
  - >2x improved MTBF
  - Further 2x cost reduction

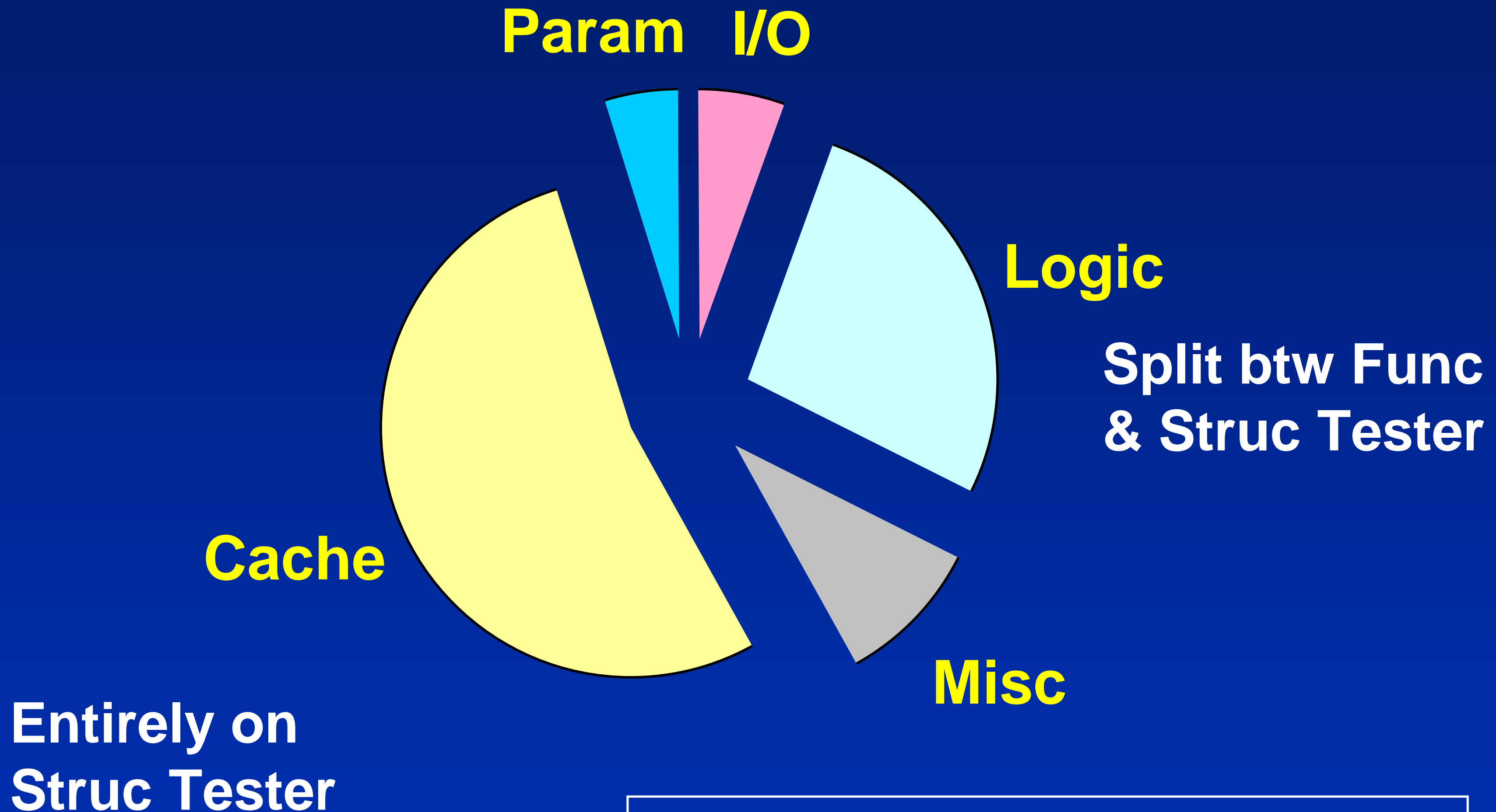




Pentium® 4 Processor Production Data

- Multiple content types on multiple platforms
  - Legacy full chip functional vectors on FT
  - New internal functional tests on ST
  - Scan tests on ST
  - Array testing, APG and BIST, on ST
  - Defect based I/O tests on ST or FT
  - Special purpose tests on ST or FT
  - Both ST1 and ST2 are in production

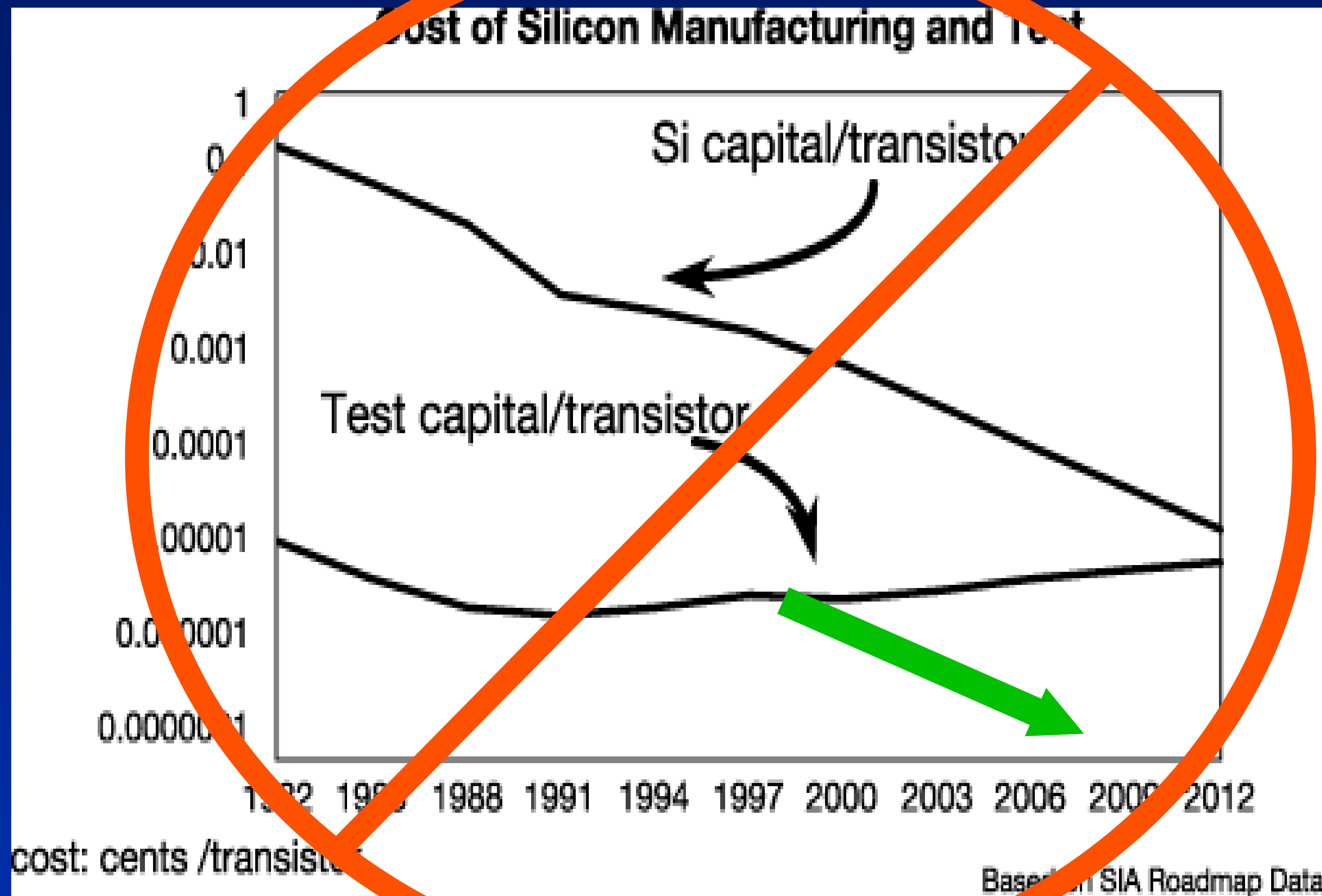
Partitioning by Test Type by Time



Wafer test – 100% on ST
Package test – 77% on ST

Key Achievements

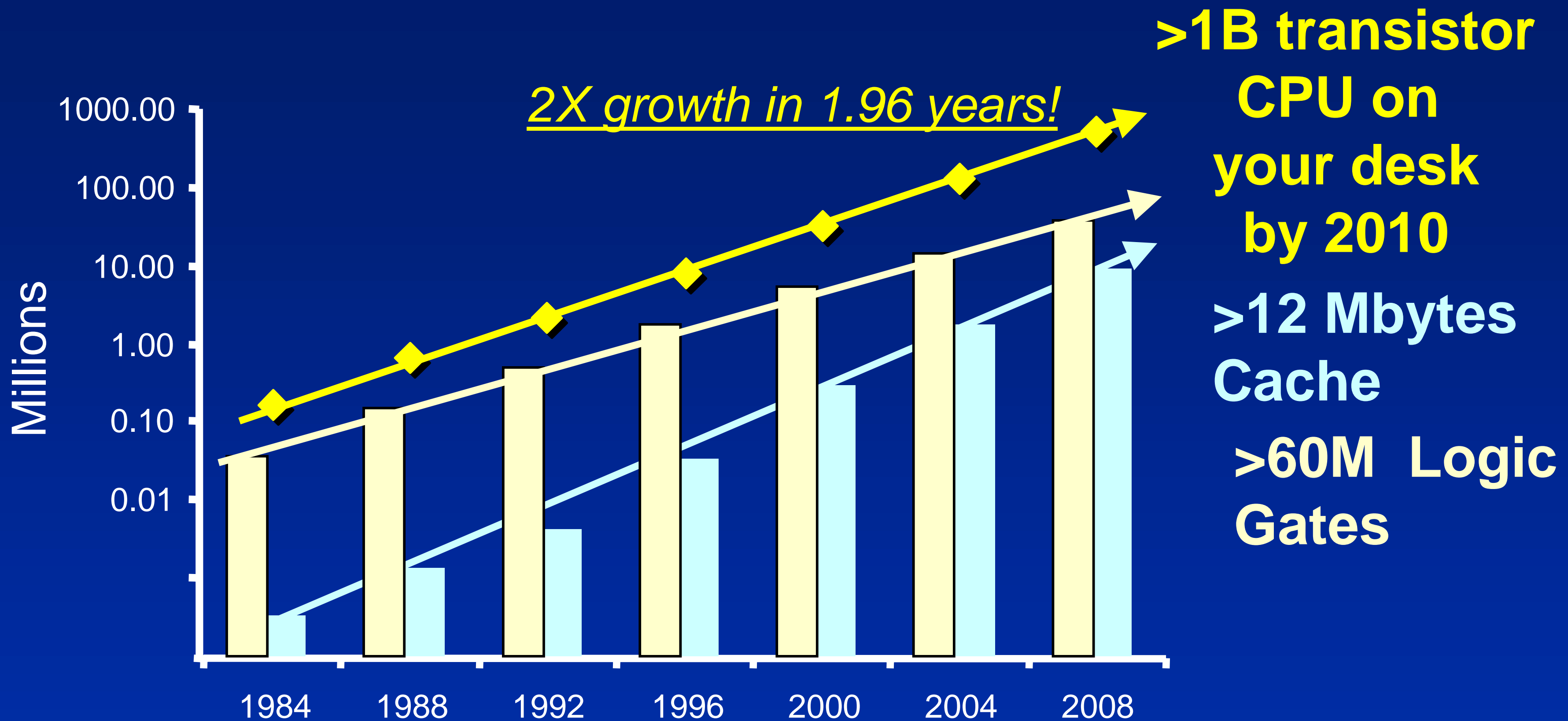
- Achieved ST migration including speed tests
  - Fallout tracks content, not platform
  - Logic-cache internal speed paths on ST
  - Other full chip speed paths on FT
  - Parallel test enabled
- Achieved key cost goals
  - 2002 CPU has 18x more xtors than 1995
  - Test cost per unit is lower than 1995
  - Intel tester capital greatly reduced
  - Per site tester cost 1/10 of functional tester



Prior to 1997, Intel test capital followed ISTR Trend

Today our test capital is scaling with Si trends

Moore's Law to Continue

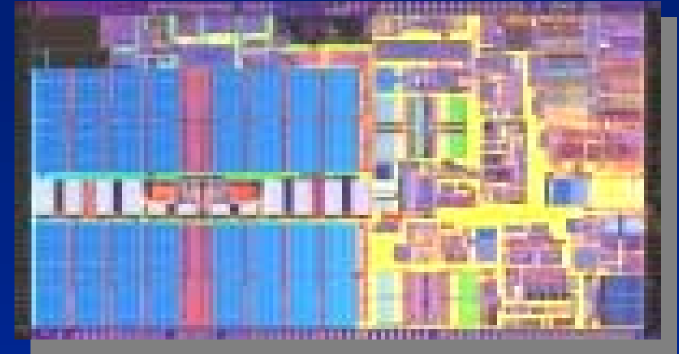


Transistor counts increasing to meet demand for performance and functionality

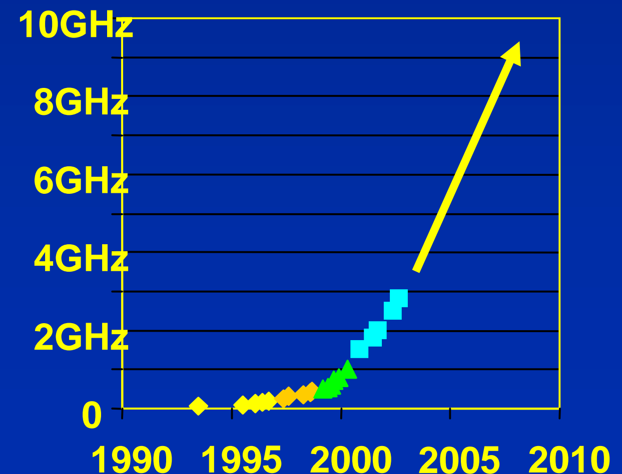
Test must keep up the pace !

Future Trends
(or how to test a billion transistors)

- Cache content growing
  - Test time
  - Yield / redundancy
  - Stability tests
  - New memory types
- Logic complexity
  - High GHz
  - Shallow logic
  - Soft Errors
  - New transistors and matls

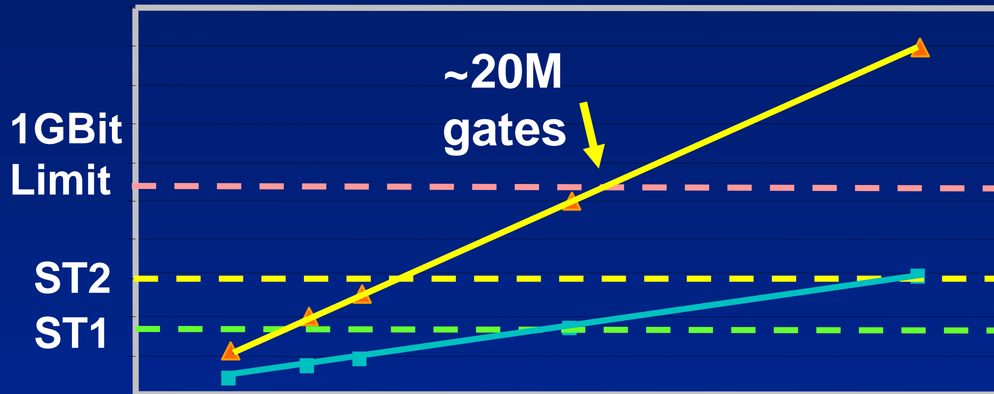


Mobile Pentium® III Processor

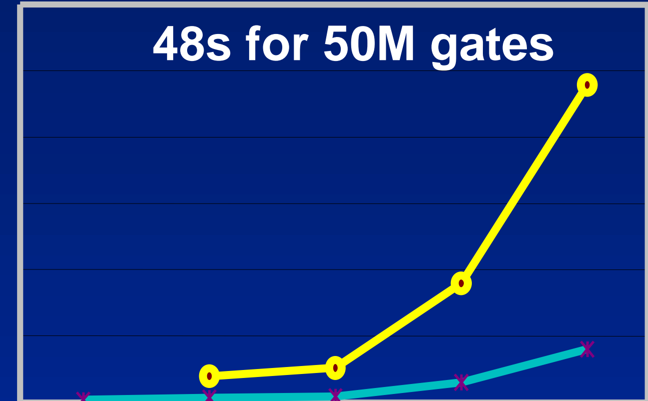


Test Times Endanger Product Cost

Data Volume vs Logic Gates



Scan Test Time vs CPU Gen



- Data Volume increasing beyond tester limits with addition of multiple fault models
- Real problem is test time and affordability
  - Need improved bandwidth, data density, or much cheaper platforms

Possible Tester Directions

Wafer Test **Package Test**

Structural Sort	Burn-In	Struc Class	Func Class

Alternative A

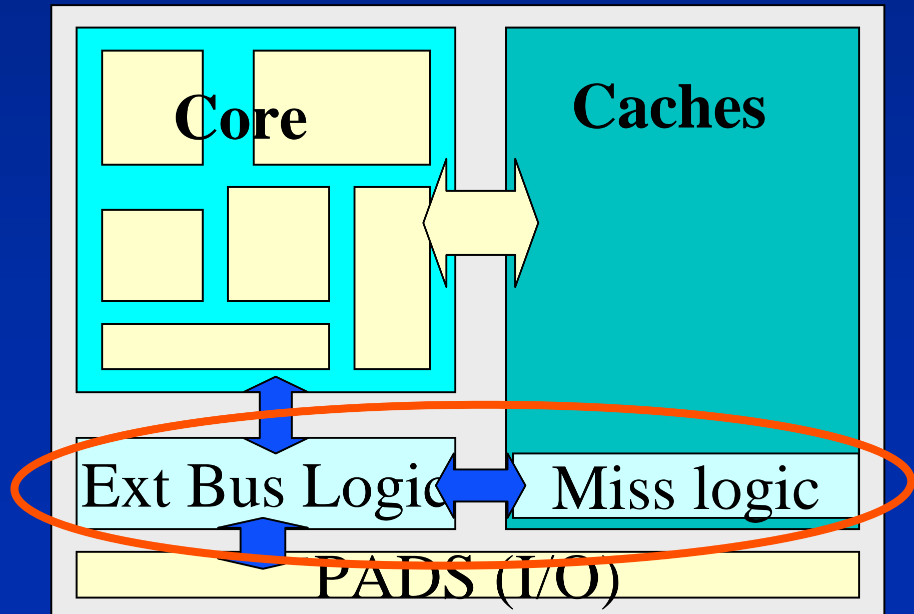
- Develop ST3
  - Site cost 2-4x less
  - More parallel sites
  - Or cheaper platform

Alternative B

- Enhance ST platform
  - More capable
  - Same price
- Eliminate FT step

Functional Tester Elimination

- Currently 77% converted to ST platform
- Of remaining 23%
  - 1/2 of failing patterns have low bus activity
  - 3/4 of down bin patterns have low bus act.
  - Potential moveable
- ST enhancement
  - Generate subset of full chip patterns
  - Swappable bus specific interface



Conclusions

- Optimize product - content - testers together
- Choose right content to test the defects
- Be flexible to allow for changing test needs

Acknowledgements
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