DESIGN OF LOW POWER OPERATIONAL AMPLIFIER USING CMOS TECHNOLOGIES

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Abstract: Nowadays use of most of the electric components have been increased due to that power dissipation and the use of the power given to the electric & electronic circuits are not fully utilized. So to avoid this problem the concept of Low Power system arises. As part of the construction of microelectronics, it has been proposed to make the choice a little circuit with attraction with the use of MOS cells. Since we often use operational amplifiers (OA) in our specialty, we chose to recreate an AO from templates provided in the book Basics of CMOS Cell Design. Now day’s differential amplifiers are widely employed in many circuits. If we minimized the power consumption of the differential amplifier the power consumption of the whole circuit will be considerably minimized. So in this paper we designed a new differential amplifier circuit using CMOS technology with lesser power consumption & high Gain.

Index Words: Low power OPAMP, CMOS,

I. INTRODUCTION

In recent years, there is an increased tendency of the embedded memories utilized in the SOC system, whose performance is greatly limited by the peripheral memory circuits, such as the decoders, level shifters, sense amplifiers, charge pumps, and so on. For embedded SONOS or flash memory systems, the performances of the sub circuits in the read path, which includes input buffer, row/column decoder, sense amplifier (SA) and output buffer, determine the access speed of the overall system. The sense amplifier lies in the bottleneck of the access path under low power supply with its delay taking up about forty percents of the whole access time, and the pre charge speed, sensing speed and noise immunity are the main challenges faced in the SA design with the reduction of power supply (VDD), especially to values as low as 1.5V [1]-[3]. Several solutions are proposed in literature to allow the normal functions under low power supply at the cost of reducing performance or noise immunity [2]-[4].

Operational Amplifiers (Op amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being...
scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon. The classic Widlar op amp architecture, originally developed for bipolar devices, has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower trans conductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes.

Analog circuit design requires a good understanding of how the system and circuit work. Unlike digital circuitry which works with two distinct states, many parameters are under consideration for analog circuits which work with continuous values. Digital circuit design may be quickly validated on a computer with the help of well-developed CAD tools. Due to the multi-dimensional variables of an analog circuit, any slight change in the analog configuration like current, voltage, a transistor parameter, a device model, a manufacturing process, or a modified layout may cause significantly different performance. In general, this low level device modeling makes analog design more complicated and challenging than digital design. For analog design engineers, a good design methodology including intuition, mathematical methods, and system level simulation combined with device level simulation is essential for creative analog designs. The proposed mixed mode design methodology, which is comprised of mathematical derivation, system level simulation, and device level simulation, will be demonstrated in this thesis.

Silicon technology continues to scale to ever smaller transistor sizes to reach the market need to include more and more transistors in DRAM and faster processing of microprocessor. While such scaling is of great benefit to digital CMOS circuit behavior, analog devices are sometimes hampered by smaller device sizes and lowered supply voltage. As the transistor lengths decrease in size, the channel modulation has a greater effect and drain current increases more with a larger VDS. To develop efficient portable electronic equipment the semiconductor industry has pushed the circuit designers towards low voltage power supply and low power consumption of circuits [4]. Though new smaller size process technologies offer opportunities to operate a tighter frequencies consuming less power, for analog circuits, this fact partially applies since it is often the case that additional current is needed to keep the same performance when the power supply voltage is decreased. Power dissipation in a circuit can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage head room available [5]. Another concern that draws from supply voltage scaling is the threshold of the transistor. A decrease in supply voltage scaling is the threshold of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues. Thus, typical analog design techniques are needed in order to face the above issues.

One important design aspect to challenge the low voltage operation is operating the analog devices in sub threshold region. In this paper a CMOS operational amplifier is presented which operates at 2V power supply and 1uA input bias current at 0.8 um technology using non-conventional mode of operation of MOS transistors and whose input is depended on bias current. The unique behavior of the MOS transistors in sub threshold region not only allows a designer to work at low input bias current but also at low voltage. For CMOS analog circuits, when the transistors operate in weak inversion region, gm/ID reaches the maximum [6]; hence the minimum power consumption can be achieved due to the
small quiescent current at the expense of large silicon area and slow speed. When MOS transistors operate in strong inversion, however, although good frequency response and small area are obtained, non-optimum larger power is consumed, and VDS (sat) is high. So, it seems a painful tradeoff question between high and low power [7]. The best tradeoff among area, power and speed is achieved when the transistors work in moderate inversion region [8, 9, and 10]. To reduce the current in the circuit the input is made bias dependent using feedback loops in the input transistors of the differential pair with two current substractors. The reported low power low voltage amplifiers using classical schemes [11, 12, and 13] have good small signal characteristics but their slew rate is small. By using the above techniques slew rate is improved, as well as lower power dissipation is achieved. Also as the transistors are operate data weak and moderate inversion of MOS transistor, the op-amp operates at low power as well as low voltage.

II. DESIGN TECHNIQUES

A. One-Stage Op Amps

Simple op amp topologies Differential input & single-ended output Differential input & differential output.

- The bandwidth is usually determined by the load capacitance, CL.
- The circuits suffer from noise contributions of M1-M4. In all op amp topologies, at least four devices contribute to the input noise: two input transistors and two “load” transistors.

B. Folded Cascode Op Amps

In the design of analog/mixed-signal IP many factors contribute to the overall consumption of power. The common methods include:

- Simplifying the complexity of the circuit and using folded designs exploiting the complementary properties of NMOS and PMOS devices.
- Taking conventional architectures and converting them into designs that consume less power with adaptive biasing.
- Gearing the integrated circuit technology towards low power performance by using high Vt processes for example 65 nm LP or 40 nm LP. Although this may not necessarily reduce power in the active mode as more current is needed to drive the high speed transmitter in the slower, low power technologies. Decreasing transistor’s dimensions together with lowering the supply voltage. Before delving into power reduction techniques for high speed serial interfaces, consider the case of an operational amplifier as the techniques applied here are pertinent to many other circuit examples.

1. The power consumption of the operational amplifier can be reduced by use of architecture with only a single (differential) stage. This will reduce the current consumption of the device. However, a method of maximizing the gain, whilst preserving an acceptable bandwidth and slew rate are now required in the single gain stage.

2. The output stage could be designed to provide sufficient output drive while quiescently consuming as little power as possible.
3. Optimizing the biasing circuit will reduce the power consumption in the op-amp. This is achieved by reducing the internal stage currents by programming an external current in the form of a resistor outside the integrated circuit. Speed, voltage noise and junction leakage will now become major considerations for the designer as these parameters are affected by the value of the bias current programmed.

4. Two important factors that determine the maximum power dissipation in an integrated circuit are the technology used for the design and the type of application. A particular application for CMOS op-amps could be low power switched capacitor filters. If a lower power/low leakage CMOS technology such as 65LP or 40LP is used, then there are two important requirements in the op-amp design. First there must be enough current to charge the compensation capacitor and load capacitor in the required time. Second there must be enough current in the second gain stage transistor to maintain a phase margin of 45 to avoid ringing and degradation of the settling time. If the output current of this circuit is less than the quiescent bias current then this is known as a Class A circuit.

5. Quiescent power dissipation can be reduced by replacing Class A op-amps with Class AB and dynamic op-amps. The Class AB output stage is designed to be biased at small currents so quiescent power dissipation is correspondingly lower.

6. The basic two-stage differential input op-amp can be designed in the sub-threshold current region to minimize the current consumption.

C. Scaling Issues “Is Analog Anti-Moore?”

Whereas scaling of digital circuits is has been investigated in detail, the application of scaling analog circuits is still not that common. For example typical transistor dimensions in an analog circuit are a few multiples larger than 40 nm minimum channels.

The sub-threshold characteristics of devices with channel lengths below 2 μm are very different to devices with larger dimensions. It has been observed that the current becomes exponentially dependent on drain voltage independent of \( V_{DS} \). This effect is sometimes referred to as “drain induced barrier lowering” (DIBL). If this effect can be avoided then \( I_D \) decreases exponentially as \( V_{GS} \) is reduced below \( V_T \).

Scaling devices and reducing the supply voltage accordingly, will not degrade open circuit voltage gain. Scaling dimensions but keeping supply voltage constant will, however, decrease the gain. The dynamic range of circuits such as op-amps fall because the analog signal range becomes limited due to the reduction in the power supply voltage. The problems of scaling down include fabrication challenges, limitations in the design of devices and circuits and the efficiency and distribution of power supplies.

Thermal noise will remain constant because the device Transconductance remains constant under constant field scaling. The 1/f noise intensifies, but the effect of this can be reduced by translating the signal to a higher portion of the frequency spectrum, using chopper stabilization.

D. Low Power Design Guidelines

A set of guide-lines can be developed for low power analog design, considering the op-amp as an example: the biasing circuitry, input, output and compensation stages can be examined. The DC biasing circuitry for the op-amp must provide accurately determined and suitably regulated quiescent biasing currents at very low current levels. The current must be insensitive to changes in temperature, supply voltage and process tolerances. The configuration of the input stage will dictate whether the
op-amp can be used in a single low voltage (1.2 V, or lower) supply application. Therefore the following properties are desirable (but not always possible) on a particular low power analog design:

- Very low power supply operation using core devices
- Class B or AB output stage "this reduces the quiescent power dissipation particularly in a leaky process"
- A rail to rail common mode input range
- A load-capacitance aware compensation scheme
- Capability to drive a small output load
- Bandwidth and slew rate commensurate with supply current
- Getting high precision by keeping offsets low, high input impedance, high CMRR and high PSRR.

III. EXISTING WORK

Complete Design of Low Voltage Low Power Operational Amplifier Using (Folded Cascade Topology)

The complete schematic of Folded Cascode Operational amplifier is shown in fig1.2. This Op amp uses cascading in the output stage combined with unusual implementation of differential amplifier to achieve good input common mode range. Folded cascode Op Amp offers good input common mode range, self-compensation, and the gain of two stages Op Amp. This architecture does not required perfect balance of current in differential amplifier because excess dc current can flow into or out of the current mirror, because the drains of M1 and M2 are connected to drains of M4 and M5. The bias current I(M5), I(M3) and I(M4) are designed so that the dc current through current mirror never be zero.

If this current goes to zero then, this requires a delay in turning the mirror back on because of the parasitic capacitances that must be charged. For example if V\text{id} the differential voltage is large enough to turn M1 on and M2 off. Then all of the I(M5) flows through the M1 and none through M2, resulting in I(M5)=I(M1) and I(M2)=0. If I(M3) and (M4) are not greater than I(M5) then the current through M8 will be zero. To avoid this we have to take I(M3) and I(M4) normally between I(M5) and 2I(M5). In the current design this is I(M3)=I(M4)=1.5 times the I(M5).

Fig.3. Low Voltage Low Power OPAMP

Fig. 4. Bias Circuit for OPAMP

Shows the circuit of a general MOS differential amplifier. The blocks labeled active load can consist of any of the circuits previously discussed that will replace resistances the key aspect of the differential amplifier is the input source coupled pair, M1 and M2. We will first examine the large signal characteristics of the circuit of figure assume that M1 and M2 are in saturation .neglecting channel modulation and assuming VT1 andvT2 ,it follow that the pertinent relationship describing the large signal behavior.
IV. PROPOSED DESIGN

The new approach developing analog circuit techniques that are compatible with future CMOS technologies. There are several important advantages of this approach. First, the need to develop expensive CMOS technologies with lower threshold voltages is avoided. Secondly, high efficiency dc-dc converters are not required. Thirdly, circuit techniques that permit low voltage operation with large thresholds offer the potential for more fully utilizing the technology at higher voltages and at lower voltages if, in fact, low threshold technologies do become standard technologies.

**Low voltage circuits are needed because**

1. As the device channel length is scaled down into submicrons and the gate oxide thickness becomes only several nanometer thick, the supply voltage has to be reduced in order to ensure device reliability. With deep submicron processes now available, the maximum allowable supply voltage is decreasing from 5V to 3V and even to 2V.

2. The increasing density of the components on chip dictates low power. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating.

3. Portable, battery-powered equipment needs low power to ensure an acceptable operation period from a battery, and the supply voltage must be as low as possible to reduce the number of batteries used.

The main purpose of the input stage in OpAmp is to amplify differential signals and reject common-mode input voltages. An important specification of an input stage is the common-mode input range. If the common-mode voltage is kept within this range, the input stage will properly respond to small differential signals. Hence an application has to be designed such that the common-mode input voltage stays within the common-mode input range. Other important specifications of the input stage are the input referred noise, offset, and the common-mode rejection ratio.

**Fig.5: Proposed Operational Amplifier Circuit**

**Fig.6: Proposed Operational Amplifier Results**

The Proposed Design uses a less no of transistor than most of the Existing techniques. At the same time we are designing the particular circuit using CMOS Technologies hence lower power and area will be achieved automatically. The Proposed circuit is designed and verified using DSCH.
V. CONCLUSION

A method is presented to efficiently compensate buffered Op-Amps. In this approach, the OTA is compensated by connecting a capacitance between the input and output of the buffer. This configuration results in a significant improvement both in the unity gain frequency and phase margin, providing higher speed and improved stability. A fully-differential Op-Amp is designed in a CMOS 0.12 \( \mu \)m standard digital CMOS process using the proposed compensation scheme. The total power consumption of the Op-Amp is reduced when compared to the existing techniques with a single power supply.

REFERENCE

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