**DARTS Literature:**

1. DARTS homepage: http://www.ecs.tuwien.ac.at/projects/DARTS

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**Distributed Algorithms for Robust Tick Synchronization**

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**Advantages:**
- Fault-Tolerance: Tolerate F out of n > 3f+1 faulty nodes
- Synchrony: Global notion of time
- Graceful Degradation: Clocks adapt to environment conditions
- Reduced EM Radiation & Ground Bouncing: Individual clocks do not switch simultaneously

**GALS Design:**
- Globally Asynchronous Locally Synchronous
- Synchroynous islands communicate over handshake
- No global notion of time
- Application level synchronization
- Design of FUs synchronous
- Asynchronous communication between FUs
- Metastability at clock boundaries

**DARTS Approach:**
- Aims:
  - Attain fault tolerance
  - Make clock routing unITICAL
  - Maintain reasonable synchronous view
- Approach:
  - Partition chip into n functional units Fu
  - Attach one TS-Alg unit to every Fu
  - TS-Algs communicate via on-chip TS-Net
  - TS-Algs provide Fu with local clocks
  - No crystal oscillator needed

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**Experimental Results:**
- Self-oscillating as expected
- Reasonable skew between clocks
- 22MHz on FPGA, more than 220MHz on ASIC expected

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**Threshold Modules:**
- Evaluation of algorithm’s rules
- Count number of active inputs
- Generate clock transition if threshold is reached
- Constant propagation delay
- Hazard-free

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