Analysis and Design of Fully Differential Gain-Boosted Op-amp for 14bit 100MS/s Pipelined Analog-to-Digital Converter

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Abstract—This paper presents the analysis and design of high speed, high gain fully differential operational amplifier (op-amp). The op-amp is designed for sample and hold circuit of 14 bit 100MS/s pipelined analog-to-digital converter (ADC). Both the main op-amp and the boosting op-amp are fully differential folded-cascode. The main op-amp has a switched capacitance common mode feedback circuit. The boosting op-amp is connected as a follower. The op-amp is designed in 0.18μm CMOS process with 3.0V power supply. Spectre simulation shows that the op-amp has the DC gain of 112dB and the unity gain bandwidth of 1.15GHz.

Keywords- fully differential op-amp; folded cascode; boosting amplifier; pipelined ADC

With the development of the wireless communication, high speed and high resolution ADCs are essential and the design of a high performance op-amp is the most important part.

Analog and digital circuit integrates onto a single die to reduce system costs, but noisy digital circuit degrades analog performance due to noise injection through power distribution network or the substrate. Fully differential analog signal processing is one of the most important techniques that reduce the problems associated with noise coupling. The fully differential technique doubles the maximum signal swing in the circuit effectively. The op-amp as the most important analog system building block has had to adopt the fully differential design technique.

Optimizing circuit for both speed and accuracy leads to contradictory demands [1][2]. High accuracy depends on high dc gain and fast settling requires a high unity-gain frequency. It is difficult to combine high dc gain with high unity-gain frequency in a CMOS op-amp. The structure of a single-stage op-amp is always used to designing high speed op-amps. It mainly has folded-cascode and telescopic topology. Compare to telescopic topology, the folded-cascode topology requires more power, but it offers large output swing and has good performance on common-mode input range[3][4]. For high gain, the architecture of a single stage amplifier with gain-boosted amplifier is a nice choice. So it is good to use a folded-cascode structure with gain-boosted amplifier in the sample and hold stage.

II. THE MODEL OF THE GAIN-BOOSTED AMPLIFIER

![Figure 1: The model of the gain-boosted amplifier](image)

This paper describes the analysis and the design of fully differential gain-boosted op-amp for 14bit 100MS/s pipelined ADC. The organization of this paper is as follows: the model of the gain-boosted amplifier is explained in section II and the circuit implementation with 0.18μm CMOS process is presented in section III. In section IV, the simulation results are given and discussed. The conclusions are presented in section V.
Figure 2. Fully differential folded cascode op-amp with fully differential gain-boosted amplifiers

According to $R_{\text{out}}$, the DC gain is

$$A_{\text{tot}} = g_{m2}r_{a2}(A+1) + r_{a1}.$$  \hfill (1)

And the DC gain of the amplifier without gain boosting is

$$A_{\text{tot}} = g_{m1}r_{a1}(g_{m2}r_{a2} + 1).$$  \hfill (2)

The gain boosting technology makes the DC gain of the circuit increasing several orders of magnitude.

III. CIRCUIT IMPLEMENTATION

A. The Op-amp Circuit

In Fig.2, a fully differential folded cascode that has two fully differential folded cascode gain-boosted amplifiers has been chosen. Actually, any amplifier can be used as the gain-boosted amplifier. A single transistor is the simplest amplifier. It consumes less power. But for high gain, the
folded cascode amplifiers are usually used for the gain-boosted amplifiers. For the input transistors, NMOS means large unity gain bandwidth but low non-dominant pole, while PMOS means small unity gain bandwidth but high non-dominant pole. So for high phase margin, the main amplifier is with PMOS input transistor. Using a PMOS input also has the shortcomings. PMOS-input requires larger input transistors and higher current to achieve high speed. Boosting stage BP is with PMOS input transistors (Fig.3). Boosting stage BN is the same as the BP type except that it is with a NMOS input transistor to realize high output impedance.

Considering about the stability, the unity-gain frequency (\( \omega_1 \)) of the boosting amplifier should not be above the second-pole frequency (\( \omega_2 \)) of the main amplifier [6]. Where \( \beta \) is the feedback factor and \( \omega_1 \) is the unity-gain frequency of the main amplifier, because \( \omega_1 \) of the boosting amplifier is smaller than the main amplifier, it is easy to satisfy (4)

\[
\beta \omega_1 < \omega_1 < \omega_2
\]  

B. The Design of the CMFB Circuit

Fully differential amplifier provides much better rejection of common-mode noise and high-frequency power-supply variations compared to their single-ended counterparts [7]. When the fully differential op-amp is in a feedback configuration like sample and hold circuits, the high differential gain of a fully differential amplifier stabilizes the differential-mode signals within the amplifier, but the common-mode signals can float. It needs an additional component (common-mode feedback (CMFB) circuit) to control the common-mode (CM) voltages. A CMFB circuit averages both differential output voltages to produce a common-mode voltage \( V_{cm} \). \( V_{cm} \) is then compared to a desired reference common-mode voltage \( V_{CM} \). The difference between \( V_{cm} \) and \( V_{CM} \) is amplified and this error voltage is used to change the common-mode feedback voltage of the op-amp to force \( V_{cm} \) and \( V_{CM} \) to be equal.

CMFB circuits can be divided into two general categories: switched-capacitor CMFB (SC-CMFB) circuits and continuous-time CMFB circuits. Compared to continuous-time CMFB, SC-CMFB consumes less power. Because the op-amp is used in sample and hold circuit, nonoverlapping phase clocks are available. The SC-CMFB is adopted which is shown in Fig.4. It consists of four capacitors and six switches. The size of the capacitors should be chosen carefully so that they will not over-load the main op-amp. The nonoverlapping phase clocks (Fig.5) control the switches on and off. When CLK1 is high, \( C_1 \) is charged to \( V_{CM} - V_{BIAS} \) [8]. \( V_{CM} \) is 1.5V. When CLK2 is high, \( C_1 \) and \( C_2 \) are connected parallel. The DC voltage of \( C_2 \) is decided by \( C_1 \) and refreshed every CLK2 period. The gain-boosted op-amp is switched on or off.

IV. SIMULATION RESULTS

According to the above analysis and design, a fully differential amplifier is designed in a 0.18\( \mu \)m CMOS process and simulated with Spectre, with a CM voltage of 1.5V and...
3pF load capacitor. Fig.6 shows the AC simulation of the main amplifier. The DC gain is 112 dB and the phase margin is 69°.

The setting behavior of the op-amp is simulated in a closed-loop configuration of sample and hold amplifier (Fig.7). The sample and hold circuit adopts the flip-around structure. The feedback factor β is nearly 1. This structure consumes low power and has low noise. The whole performances of the op-amp are shown in Table 1. Previous designs are also included [2][9]. From Table 1, we can see that the op-amp proposed in this paper has a higher DC gain, a larger unity GBW and a faster settling time than the other designs.

### Table 1. Performance Parameters

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<tr>
<td>DC Gain,(dB)</td>
<td>112</td>
<td>90</td>
<td>95</td>
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<tr>
<td>Unity GBW,(GHz)</td>
<td>1.15</td>
<td>0.116</td>
<td>0.412</td>
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<tr>
<td>Phase Margin,(deg)</td>
<td>69</td>
<td>64</td>
<td>75</td>
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<td>Supply Voltage,(V)</td>
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<td>5.0</td>
<td>3.0</td>
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<tr>
<td>Load Capacitor,(pF)</td>
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<td>1.9</td>
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<tr>
<td>Settling Time,(ns)</td>
<td>2.44</td>
<td>61.5</td>
<td>7.5</td>
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<tr>
<td>Power,(mW)</td>
<td>19.48</td>
<td>52</td>
<td>12.8</td>
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V. CONCLUSIONS

This paper presents the analysis and design of fully differential amplifier with gain boosting technology. The gain-boosted amplifier is achieved by using the folded cascode amplifier. Based on 0.18μm CMOS process, it has good performance, with a DC gain of 112dB and a unity gain bandwidth of 1.15GHz. The designed op-amp fulfills the stringent specifications of 14bit 100MS/s sample and hold circuit of pipelined ADC.

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