

# A Fully-Differential 2 GHz Tunable Recursive Bandpass Filter on Silicon

Sébastien Darfeuille<sup>1</sup>, Zoheir Sassi<sup>1</sup>, Bruno Barelaud<sup>1</sup>, Laurent Billonnet<sup>1</sup>, Bernard Jarry<sup>1</sup>,  
Hervé Marie<sup>2</sup>, Nguyen Tran Luan Le<sup>2</sup>, Patrice Gamand<sup>2</sup>

<sup>1</sup>IRCOM, UMR CNRS 6615, University of Limoges, 123 Avenue Albert Thomas, 87060 Limoges cedex, France

<sup>2</sup>Innovation Centre RF, Philips Semiconductors, 2 Rue de la girafe, 14079 Caen cedex, France

Email : sebastien.darfeuille@ircom.unilim.fr

**Abstract** — In this paper, we present a novel fully-differential active integrated bandpass filter employing recursive principles. This circuit, based upon the cascade of two elementary recursive stages, can be tuned independently in terms of centre frequency, selectivity and gain. The chip surface is less than 1.4 mm<sup>2</sup>. Centre frequency can be tuned in the 1.7 to 2.4 GHz range, bandwidth can be set to less than 60 MHz and gain can be up to 20 dB. This chip has been implemented using Philips QUBIC4 Si BiCMOS technology [1].

## I. INTRODUCTION

Off-chip passive filters are nowadays the most frequently implemented solution in RF receivers front-ends. However, the main drawback with that kind of filters is that they are often expensive and occupy an important surface.

An interesting alternative could be the use of active filters associating in a single circuit a bandpass filter and a low-noise amplifier, thus leading to more compact and lower cost circuits. Another advantage is that, as they are realised with the same technology, these filters can be easily integrated with the other functions of the transceivers (mixer, ...). Moreover, they often exhibit a frequency tunability that could help to reduce the number of required elements in multi-standard equipments that are being generalised more and more each day. This aspect is also interesting to realise automatically tuned structures [2]. In this article, we propose an original tunable recursive filter integrated using a silicon MMIC process and based on the cascade of two elementary recursive stages.

## II. THEORETICAL BACKGROUND

The concept of recursive filters has been mainly developed at low frequencies for digital applications. However, as demonstrated in [3], it can also be applied to microwave analogue filters.

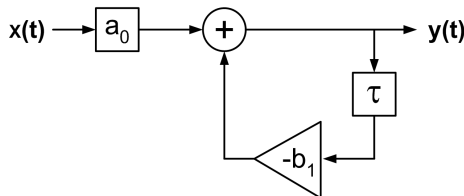


Fig. 1. Block diagram of a first-order recursive filter

Fig. 1 presents the flow graph of a first-order recursive filter, driven by the following time-domain equation :

$$y(t) = a_0 x(t) - b_1 y(t - \tau) \quad (1)$$

which leads to the corresponding transfer function :

$$H(f) = \frac{a_0}{1 + b_1 e^{-j2\pi f\tau}} \quad (2)$$

The topology proposed here relies on the cascade of two first-order recursive cells, as can be seen in Fig. 2.

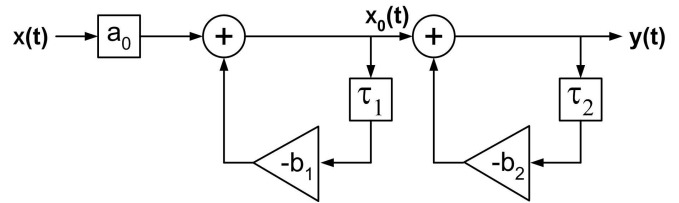


Fig. 2. Block diagram of the cascaded recursive filter

The main advantage of this kind of structure is that it permits to realise, with only two branches, a recursive filter that would require three branches with a more classical ladder implementation, as can be seen in Fig. 3.

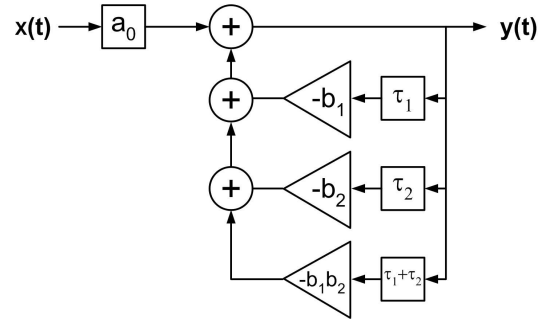


Fig. 3. Block diagram of the equivalent ladder configuration

The obtained transfer function is depicted by [4] :

$$H(f) = \frac{a_0}{1 + b_1 e^{-j2\pi f\tau_1} + b_2 e^{-j2\pi f\tau_2} + b_1 b_2 e^{-j2\pi f(\tau_1 + \tau_2)}} \quad (3)$$

Then, if the delay times are chosen identical ( $\tau_1 = \tau_2 = \tau$ ), it is possible to achieve a typical second-order recursive filter response with amplifiers of respective gains  $b_1 + b_2$  and  $b_1 b_2$ .

$$H(f) = \frac{a_0}{1 + (b_1 + b_2) e^{-j2\pi f\tau} + b_1 b_2 e^{-j4\pi f\tau}} \quad (4)$$

### III. IMPLEMENTATION

The chosen topology for the differential first-order cells is derived from [5], with the delay cell inserted within the feedback branch.

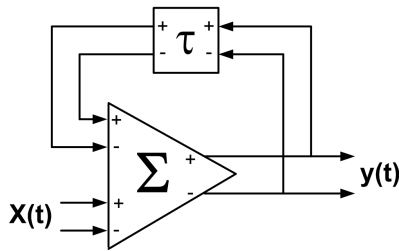


Fig. 4. Principle scheme of an elementary stage

The use of a passive delay section achieving a  $180^\circ$  phase shift has been preferred to an active solution - even considering the important size of the inductors - as it allows to reduce the global power consumption which is a critical point in our application where two of these delays are required. Varactor diodes controlled by two independent voltages allow to control the objective delay in each cell.

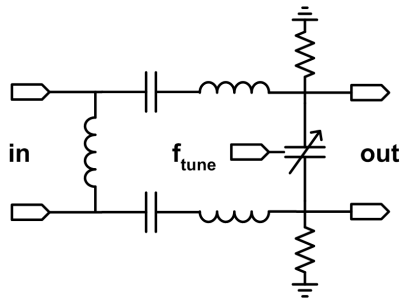


Fig. 5. Tunable passive delay electrical scheme

The circuit used for amplification and summation is derived from the adders presented in [5] and [6] and is presented in Fig. 6. The use of a cascode topology for the direct input ( $in_1$  in Fig. 6) exhibits better noise performances than a common-base one, whereas for feedback input ( $in_2$  in Fig. 6) a classical differential amplifier topology including a gain control with a current-mirror is used.

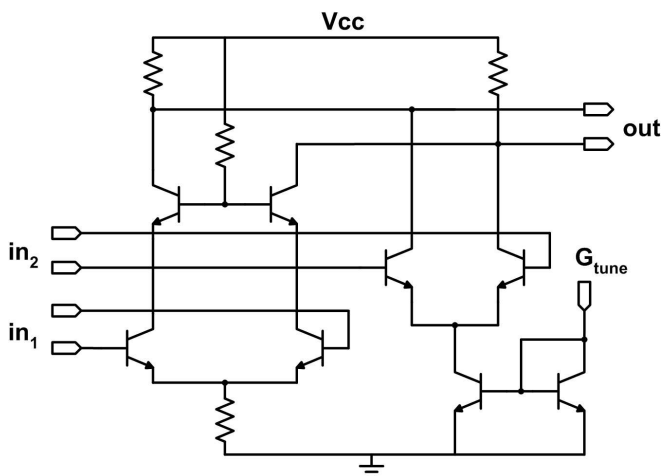


Fig. 6. Simplified electrical scheme of the amplifier/adder

Finally, a buffer stage (see Fig. 7) derived from the cascode amplifier of the adder is cascaded at the output. It permits to set the global gain of the structure. Indeed, the base resistance of the cascode transistors of the adder has here been replaced with a PMOS transistor. Thus, by controlling the gate voltage, it is possible to set the gain of this stage and, as a consequence, of the whole filter.

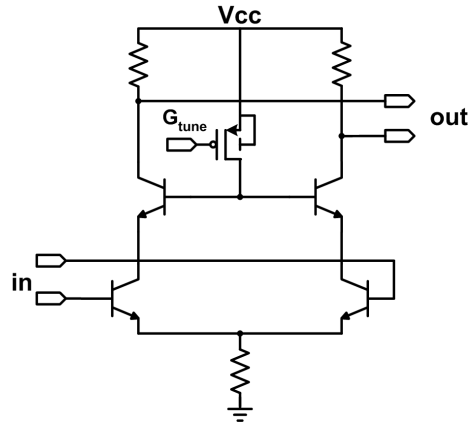


Fig. 7. Simplified electrical scheme of the output buffer

The use of tunable structures for all the elements in the circuit gives more flexibility in the response shape. Indeed, it is possible to control independently the centre frequency (by acting on the delay elements), the bandwidth (by acting on the gain of the feedback input of the adders), and finally the global gain (with the output buffer).

The chip surface is  $1.05 \times 1.3 \text{ mm}^2$ . On the layout presented in Fig. 8, the two passive delays can be easily identified at the top-left and bottom-right as they are the most space consuming components due to the use of inductors (each delay occupies a surface of about  $600 \times 550 \mu\text{m}^2$ ). In general, chip dimensions is a highly critical point due to the price of the substrate. Here, to keep an acceptable surface for the global circuit, the other parts (adder and buffer) are inductorless.

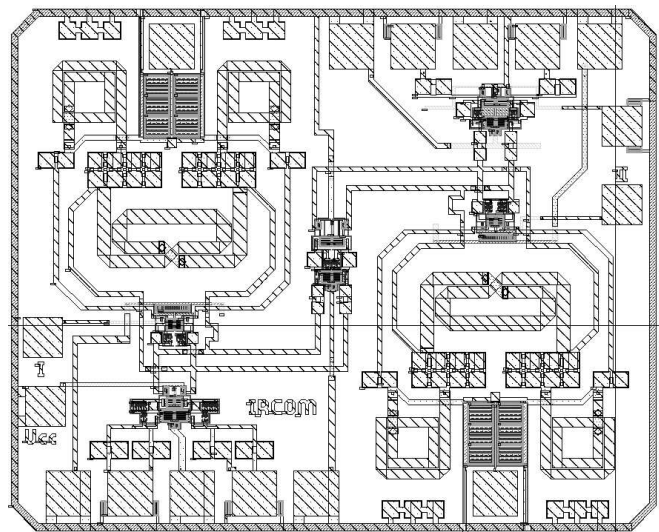


Fig. 8. Layout of the circuit

#### IV. SIMULATION RESULTS

The circuit is being processed at the foundry. Measurements will be available at the conference.

As can be seen in Fig. 9, this filter can be tuned in the 1.7 to 2.4 GHz range.

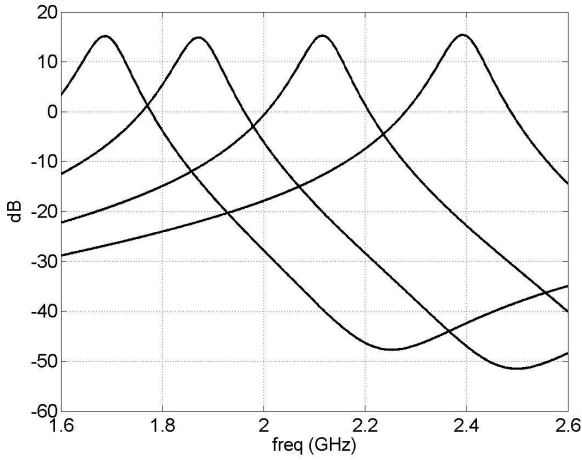


Fig. 9. Simulated gain

For all the centre-frequencies, it is possible to obtain a gain of 15 dB and a 60 MHz bandwidth. These values of gain and selectivity are not the best achievable and can still be decreased or increased to fit specific performances. Moreover, as illustrated in Fig. 10, it is possible, by setting different delays for the two subcircuits ( $\tau_1 \neq \tau_2$ ), to obtain a different response shape (for example if a flatter response is desired in the bandwidth). However, in this case, selectivity is generally worse than when the delays are chosen identical ( $\tau_1 = \tau_2$ ).

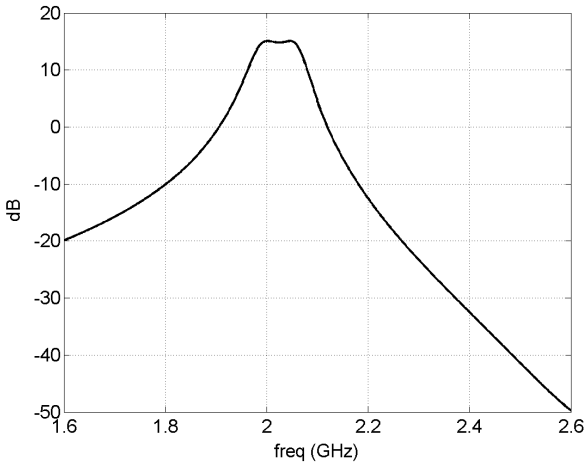


Fig. 10. Simulated gain with a quasi-flat response shape

Depending on the centre frequency, and for a typical 15 dB gain and 60 MHz bandwidth, noise figure varies between 3.6 and 5.5 dB, and output-referred -1 dB compression point between -36 and -26 dBm. This last parameter is the main drawback of this circuit and is due to the important number of active cascaded sub-cells.

For a nominal 2.7 V biasing and in the same conditions as previously, power consumption varies between 35 and 50 mW.

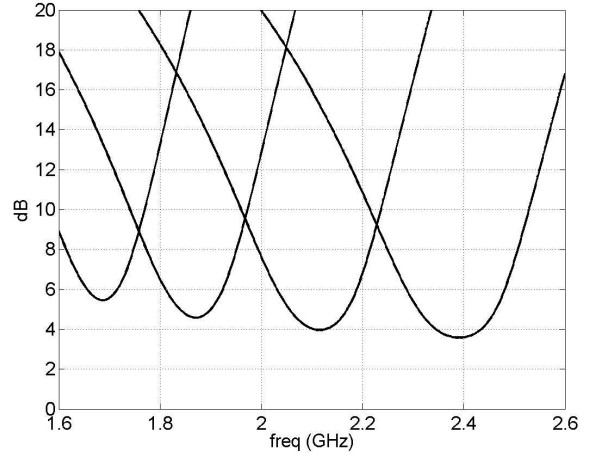


Fig. 11. Simulated noise figure for various centre frequencies

Thanks to the presence of the amplifier at the input and of the buffer at the output of the circuit,  $S_{11}$  and  $S_{22}$  responses are quasi-independent of the different tuning parameters. In any case, in the 1.7 - 2.4 GHz range, they are less than -9.5 dB for  $S_{11}$  and -14.5 dB for  $S_{22}$ . This value of  $S_{11}$  can be explained by the fact that, for the chosen inductorless adder topology, it is impossible to obtain simultaneously noise and power matching over a wide frequency band [7]. A compromise has thus been made between these two parameters. Concerning  $S_{22}$ , the value is directly driven by the value of the resistances placed between the collectors of the output buffer cascode transistors and the global bias  $V_{cc}$  (see Fig. 7).

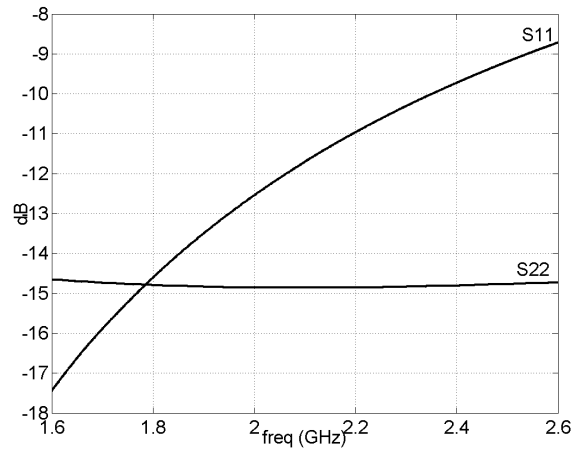


Fig. 12. Simulated matching parameters

All the  $S$ -parameters presented here are fully-differential mode  $S$ -parameters obtained using mixed-mode analysis method [8]. They correspond to the results that would be obtained if 50  $\Omega$ -baluns were used at the input and output of the circuit.

As can be seen in Fig. 13, common-mode gain is always lower than -20 dB, which leads to a more than 35 dB common-mode rejection ratio at the centre frequency. All

## V. CONCLUSION

In this article, we have presented an original differential tunable recursive filter. This circuit performs a simulated gain of 15 dB with a 60 MHz bandwidth at centre frequencies ranging between 1.7 and 2.4 GHz. In these conditions and depending on the centre frequency chosen, power consumption ranges between 35 and 50 mW for a supply voltage of 2.7 V. Simulated noise figure is about 3.6 to 5.5 dB at the centre frequency.  $P_{-1dB}$  is reached for an output power of -36 to -26 dBm. Chip dimensions are  $1.05 \times 1.30 \text{ mm}^2$ .

## ACKNOWLEDGEMENT

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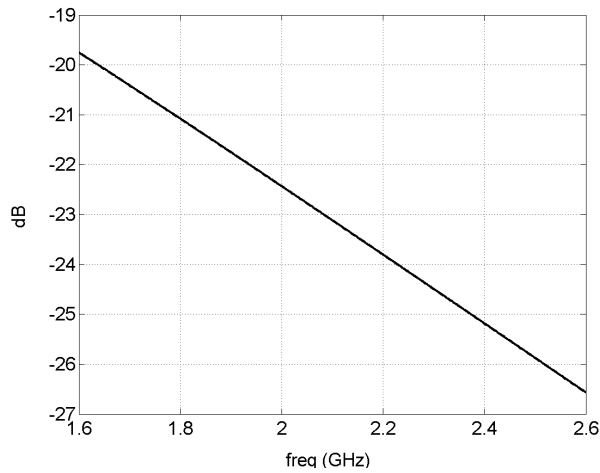


Fig. 13. Simulated common-mode gain

Conversion modes (i.e. differential-to-common and common-to-differential modes)  $S$ -parameters were found to be lower than -40 dB at any frequency, meaning that the topology is quite insensitive to electromagnetic interferences (which are typically of the common-mode type).

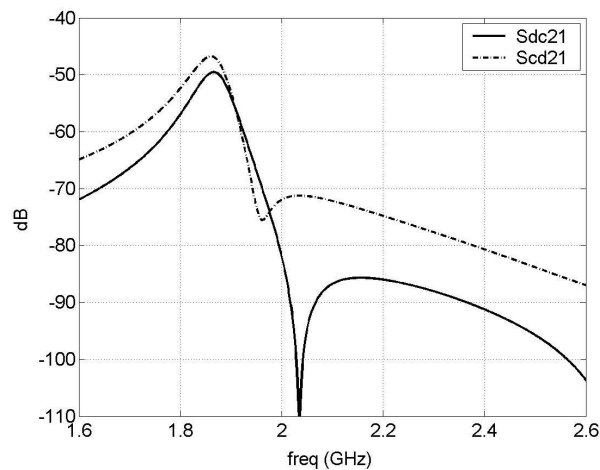


Fig. 14. Simulated common-to-differential and differential-to-common gains