studied, and a number of efficient techniques exist for their computation. Pennebaker et al focus on one of the main obstacles in performing accurate DCT computations is the implementation of the irrational coefficient multiplications needed to calculate the transform. Traditional DCT implementations adopt a compromise solution to this problem, employing truncation or rounding off to approximate these quantities. As a consequence, computational errors are systematically introduced into the computation, leading to the degradation of the signal-to-noise ratio (SNR).To partially address this issue, algebraic integer (AI) encoding has been employed. The main idea in this approach is to map required irrational numbers into an array of integers, which can be arithmetically manipulated in an error free manner. At the end of the computation, AI based algorithms require a final reconstruction step (FRS) in order to map the resulting encoded integer arrays back into the usual fixed-point representation. FRS can be implemented by means of individualized circuits, at, in principle, any given precision. Cintra et al [8] mainly focus on reducing the complexity of DCT computations. An orthogonal approximation is followed in this method where zeros and ones are presented in place of multiplication and add shift bits.

From all the above we see the research is focused either on the complexity of DCT or coefficients modulation of DCT. But the simulation time taken by DCT is still not efficient one and suffering from critical sampling. The matrix data (pixel data) can be approximated on less human vision focus areas in an image which lead to reduce the simulation time. So image can be still validate. Work is completely at the algorithm level where focusing on the reducing the complexity and reducing the number of operations.

At the algorithm level where focusing on the reducing the complexity and reducing the number of operations. DCT at hardware level has been also employed. Low Power DCT structure are very popular nowadays, & can be realize with MAC (Multiply Accumulate) unit and computation sharing multiplication CSHM[10] which reduces the computation susceptible to small or no quality degradation. This seems to have an energy aware design in nano-meter regime and raise the structure as Process- variation aware because parametric variation below 90nm raise the question of redesigning of the structure of DCT, with more/less significantly contributing coefficients, with data path redesigning. The design discussed reduces the pre-computers & Select/Shift and Add units and obtain the skew in different path-length. This guarantees the DCT architecture to be one of the fruitful under the process variation effect and can provide the best result in every circumstance. Voltage Over Scaling is required for error resiliency subjected to process variation analysis. This raises the problem of over computation as VOS[11], for delay of some less significant part. Dynamic reconfigurable DCT provides the examination of input bit stream and then reconfigure the DCT to have optimal computation in result will have area over head which becomes the problem of this approach. The arithmetic involve is distributed arithmetic[16] which becomes very popular nowadays requires ROM based coefficient storage, while cordic based DCT are also available which produces coefficient accordingly. In context to approximation component development taking into account as various type of adder (as adder is prime component of DIP), like ETA (Error Tolerance Adder), Variable Latency Speed Adder.

The 1D-DCT transforms Image in one dimension. This can be extends to 2D-DCT in similar fashion and the analysis is carried out provides that, component are arranged in increasing order of frequency. To archive for error resiliency/tolerant, Speed, Power, Area and Accuracy will be a challenging part to achieve, many a time trade-off scenario is observed.

Parameters to Evaluate the Image

1) PSNR(Peak Signal to Noise Ratio)[17]
2) SSIM (Structural Similarity Based Image Quality Assessment)[14]
3) FSIM (Feature Similarity Index For Image Quality Assessment)[13]
4) GMSD(Gradient Magnitude Similarity Deviation)[11]
5) RFSIM (Riesz-transform based Feature Similarity metric)[12]

3. Research Gap

Error Resilient feature of Image Compression is not fully utilized in terms of

- Optimized hardware
- Power requirement
- Coefficient aware design
- Optimization in JPEG architecture

4. Conclusion

Present era has witnessed tremendous improvement in multimedia applications with growing data traffic in network, which results in improper energy utilization on portable devices. These data are compressed without compromise of quality and certainly up to 10% degradation in quality is tolerable/acceptable as per human perception. This well-known feature is utilized in Digital Image Processing (DIP) applications like JPEG, MPEGx, etc. The study of image/video encoder provides detail of prominent compressor unit i.e., Discrete Cosine Transform (DCT) block; which transforms the signal or data from spatial domain to frequency domain and arranges it from low to high frequency. As an outcome of literature review, we came to know based on pixel behavior that fewer coefficients are required to process from input end in comparison to conventional multiplier based DCT.

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