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Article

Analysis of Losses in Open Circuit Voltage for an 18-µm Silicon Solar Cell

Lu Wang [1,*], Jianshu Han [2], Anthony Lochtefeld [3], Andrew Gerger [4] and Allen Barnett [2,*]

1 Tongwei Group Co., Ltd., Chengdu 610041, China

2 School of Photovoltaic and Renewable Energy Engineering, University of New South Wales, Sydney 2052, Australia; E-Mail: j.han@student.unsw.edu.au

3 AmberWave Inc., Salem, NH 03079, USA; E-Mail: alochtefeld@amberwave.com

4 SolAero Technologies Corp., Albuquerque, NM 87123, USA; E-Mail: andrew_gerger@solaerotech.com

* Authors to whom correspondence should be addressed; E-Mails: wangl18@tongwei.com (L.W.) allen.barnett@unsw.edu.au (A.B.); Tel.: +86-184-8226-8838 (L.W.).

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Abstract: An 18 µm thin crystalline silicon solar cell was demonstrated, and its best open circuit voltage is 642.3 mV. However, this value is far from the cell's theoretical upper limit in an ideal case. This paper explores the open circuit voltage losses of the thin silicon solar cell, starting from the ideal case, through first principle calculation and experiments. The open circuit voltage losses come from the introduced recombination due to the non-ideal surface passivation and contacts integration on front and rear surfaces, and edge isolation. This paper presents a roadmap of the open circuit voltage reduction from an ideal case of 767.0 mV to the best measured value of 642.3 mV.

Keywords: V_{oc} losses analysis; 18 µm; silicon solar cell

1. Introduction

The theoretical upper limit performance of both thick silicon solar cells [1] and thin silicon solar cells [2,3] have been well studied. There is a significant performance gap between the ideal and the

practical cells, which is caused by optical losses, bulk recombination, surface recombination, contact recombination, and resistance losses in a manner similar to that observed by Swanson [4].

In a previous paper, an 18 μm thin crystalline silicon solar cell on steel has achieved a best efficiency of 16.8% and a best open circuit voltage (V_{oc}) of 642.3 mV [5]. The structure of the ultrathin silicon (UTSi) solar cell is shown in Figure 1. The ultrathin silicon is 20 μm thick, which is attached onto 125 μm steel substrate, and includes three layers: top front surface field (FSF) layer which is n^+ and 1 μm, middle base layer, which is n type and 18 μm, and bottom emitter which is p^+ 1 μm. Both surfaces of this thin silicon are well passivated and optically designed.

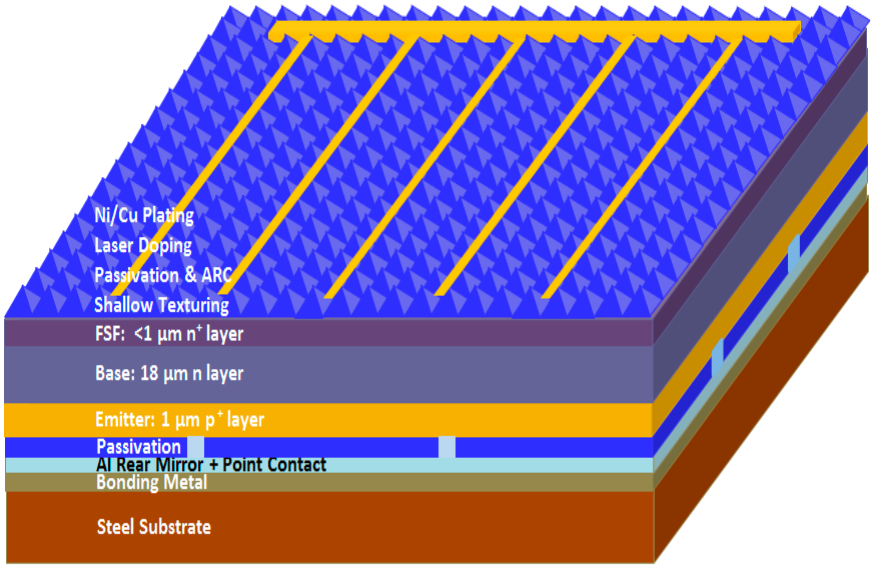

Figure 1. Diagram of the UTSi solar cell on steel substrate [5].

However, according to our analysis the theoretical maximum V_{oc} of this thin silicon solar cell can be as high as 767 mV [5]. The V_{oc} difference between an ideal case and a practical case is due to the introduced recombination. This paper discusses these recombination sources that include non-ideal passivated front and rear surfaces, laser-introduced damage on the front surface, contacted regions on both front and rear surfaces and edge recombination. Based on our previous analysis, bulk recombination is negligible for such thin crystalline silicon solar cells [5]; thus, it is not discussed in this paper.

This paper explores the V_{oc} losses through the first principle calculation and the measurement results on test samples and the UTSi solar cells. The V_{oc} loss at each step is figured out and a roadmap of V_{oc} reduction from the no loss (or modeled) case of 767 mV to the best measured value of 642.3 mV is established.

2. Fabrication

The detailed fabrication of this UTSi solar cell has been described [5,6]. All semiconductor layers including n^+ front surface field, n base and p^+ emitter are epitaxially grown on a porous silicon layer on a p^+ wafer. After the thin silicon is grown on its host p^+ wafer, the rear surface undergoes passivation and metallization. Then, the epitaxial thin silicon layer is exfoliated and transferred onto the steel substrate. After exfoliation, the porous silicon surface becomes the front side, and this surface is shallow textured in an alkaline solvent. This textured front surface is then passivated by PECVD deposited

SiO_xN_y (silicon oxynitride). Front contacts are formed by combining selective laser doping and self-aligned Ni/Cu light induced plating. Fabrication is completed by edge isolation, a combination of laser cut and chemical etching processes, because well isolated edges lead to reduced FF and V_{oc} losses.

3. V_{oc} Losses Analysis

3.1. V_{oc} in Ideal Case

In an ideal case, the UTSi solar cell has a high V_{oc} and efficiency potential. PC1D [7,8] is used to calculate the upper limit efficiency and V_{oc} of a 20 μm silicon solar cell. Lifetimes of the n^+ front surface field (FSF) layer, p^+ emitter and n base are assumed to be 10 μs, 10 μs and 1000 μs, respectively. The modeled upper values of V_{oc} and efficiency are 767 mV and 25.4%, respectively [5]. To separate the surface recombination from bulk recombination, we assume the surface recombination velocity (SRV) of both surfaces to be 0 cm/s, so that there is only bulk recombination. Table 1 shows the reverse saturation current densities and the corresponding V_{oc} values.

Table 1. J_0 components, values and their corresponding V_{oc} values when SRV is 0 cm/s. J_{0e} is the reverse saturation current density in the emitter, J_{0b} is the reverse saturation current density in the base and FSF layer.

Steps	J_0 Components	J_0 Value (A/cm^2)	V_{oc} (mV)
--	J_{0b}	4.73×10^{-15}	--
--	J_{0e}	3.03×10^{-17}	--
1	$J_{0b} + J_{0e}$	4.76×10^{-15}	767.0

In addition to the PC1D model, first principle calculations are used to calculate V_{oc}. We first separate the surface recombination from bulk recombination by assuming SRV(S_n, S_p) to be 0 cm/s so that there is only bulk recombination in the base (J_{0b}) and emitter (J_{0e}). The J_0 equation becomes $J_0 = J_{0b} + J_{0e} = \frac{qD_n n_1^2}{L_n N_A} \times \tanh(\frac{W_p}{L_n}) + \frac{qD_p n_1^2}{L_p N_D} \times \tanh(\frac{W_n}{L_p})$, where N_A and N_D are doping densities; L_n and L_p are minority carriers diffusion lengths; W_p and W_n are the thickness; S_n and S_p are minority carriers surface recombination velocities; D_n and D_p are minority carriers diffusivity at *p* and *n* silicon, respectively; and n_i is the intrinsic concentration. J_0 is determined by $\frac{W_p}{L_n}$ and $\frac{W_n}{L_p}$, the ratio of thickness over diffusion length. The maximum V_{oc} is 758 mV for a 20-μm cell, with an *n* base with a thickness of 18-μm, a doping density N_D of 5×10^{15} cm^{-3} and a lifetime of 1000 μs, a p^+ emitter 1 μm, 5×10^{17} cm^{-3} and lifetime of 10 μs. No n^+ FSF layer is considered in this calculation.

3.2. V_{oc} Loss Due to Surface Recombination

3.2.1 SRV on a Passivated n type Surface

There is a 1–2 μm 5×10^{17} cm^{-3} or 1×10^{18} cm^{-3} n type FSF layer in this UTSi solar cell, and this layer is mostly etched away during the shallow texturing process [5]. The front surface of the textured UTSi solar cell is mainly an n (5×10^{15} cm^{-3}) surface with a partially remaining n^+ (5×10^{17} cm^{-3} or

1×10^{18} cm^{-3}) surface. The front surface is passivated by silicon oxynitride (SiO_xN_y) [9]. This section tests the surface recombination in the SiO_xN_y passivated n type surfaces. Two groups of test samples were designed, as shown in Figure 2: group A1 with n (5×10^{15} cm^{-3}) epitaxial surfaces and group B1 with n^+ (5×10^{17} cm^{-3}) surfaces. Float-zone (FZ) substrates were chosen because they have negligible bulk recombination and provide an ideal substrate for epitaxial growth. In this way, their lifetime or implied V_{oc} values are not limited by bulk but by surfaces. These FZ substrates were from the same wafer and these samples were processed along with control samples to eliminate extraneous variables. After SiO_xN_y deposition, these samples were annealed at 400 °C for 10 min to activate surface passivation [9]. Their implied V_{oc} (iV_{oc}) and lifetime were measured by a Sinton lifetime tester [10]. An iV_{oc} of 718 mV and effective lifetime of 1085 μs were obtained in the sample with 18 μm 5×10^{15} cm^{-3} n type silicon epitaxial layers, while an iV_{oc} of 696 mV and lifetime of 556 μs were measured in the sample with 1 μm heavily doped 1×10^{18} cm^{-3} n^+ epitaxial layers. To calculate the SRV of both surfaces, the equation $\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2 \times S}{W}$ is used, where τ_{eff} is the effective lifetime measured, S is the SRV, W is the thickness of silicon, τ_{bulk} is the bulk lifetime of the FZ wafer. In this calculation, the intrinsic bulk lifetime of the FZ wafer, 1.8×10^4 μs, was estimated using an online program PV Lighthouse [11]. Intrinsic bulk lifetime eliminates the effect of Shockley-Read-Hall recombination and leads to conservative values for the SRV. SRV values for the 5×10^{15} cm^{-3} surface and 1×10^{18} cm^{-3} surface are 13 cm/s and 26 cm/s, respectively.

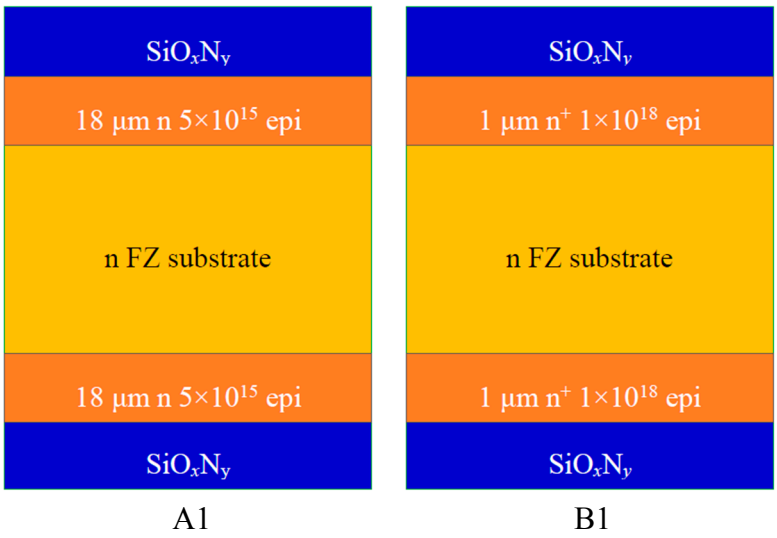

Figure 2. Control sample and two groups of test samples for n and n^+ epitaxial layers and their passivation.

Table 2. iV_{oc} and J_0 components for samples in Figure 2.

ID	iV_{oc} (mV)	Lifetime (μs)	SRV (cm/s)
Group A1	718	1085	13
Group B1	696	556	26

3.2.2. SRV on a Passivated p^+ Surface

SRV depends strongly on the processing methods, including oxidation conditions, annealing conditions, surface roughness and contamination. King reported a surface recombination velocity of 1640 cm/s on a SiO_2 passivated p^+ silicon surface, which is independent of injection level [12]. Thermal oxide is used to passivate the heavily doped p^+ epitaxial emitter of the UTSi solar cell. This section tests the SRV of the thermal oxide passivated heavily doped p^+ type surface. Control samples were used at each step to eliminate contamination and extraneous variables. A doping density of 5×10^{17} cm^{-3} for the rear emitter was selected in this experiment, and these test samples' structures are plotted in Figure 3. Group A2 has 1 μm, 5×10^{17} cm^{-3} epitaxial p^+ layers on both surfaces, which are passivated by SiO_xN_y [9]; Group B2 has 1 μm, 5×10^{17} cm^{-3} epitaxial p^+ silicon layers on both surfaces, which are passivated by SiO_2. These samples were from the same wafer and were processed along with the control ones.

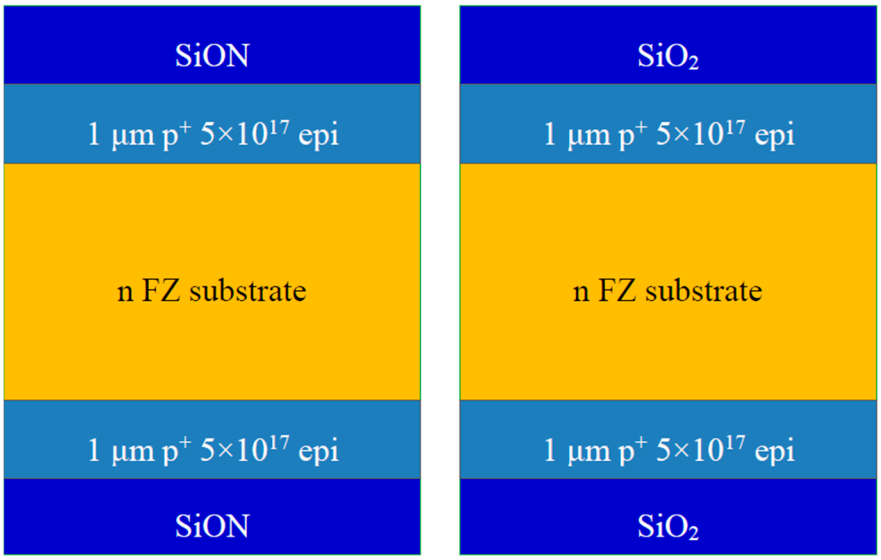

Figure 3. Test structures for p^+ epitaxial layers and their passivation.

SRV (S_p) values are extracted in Table 3, using the relation $J_0 = qsn_{ie}^2 / N_{A,surf}$ [12], where J_0 is extracted from the above lifetime measurements, which is determined by the surface when the bulk recombination is negligibleis; $N_{A,surf}$ is the doping density of surface; q is the electronic charge; n_{ie} is the intrinsic carrier concentration in the emitter, and equals to $n_{i0}^2 e^{\frac{\Delta E}{kT}}$, where n_{i0} is the intrinsic carrier concentration in the absence of bandgap narrowing and ΔE is the bandgap narrowing. $\Delta E = 0.03$ eV for 5×10^{17} cm^{-3} and $\Delta E = 0.01$ eV for 2×10^{17} cm^{-3} [12,13]. According to the calculated results, the SRV values of the SiO_2 passivated p^+ emitter surface are 1551–1677 cm/s, as shown in the table, which is consistent with the value of 1640 cm/s reported by King [12].

Table 3. Lifetime, iV_{oc}, J_{0e} and SRV of Group A2 and B2 test samples from Figure 3.

Group	Lifetime (μs)	iV_{oc} (mV)	J_{0e} (A/cm^2)	SRV (cm/s)
A2	161–221	644–658	--	--
B2	139–157	637–642	$1.85 \times 10^{-13} \sim 2.0 \times 10^{-13}$	1551–1677

3.3. V_{oc} Losses Calculation

The theoretical maximum open circuit voltage achievable in a 20 μm silicon solar cell is 767 mV, when both surface recombination velocities are 0 cm/s. However, the front n type surface and the rear p^+ emitter surface of the UTSi solar cell are passivated by SiO_xN_y and SiO_2 respectively, and neither SiO_xN_y nor SiO_2 are the perfect passivation layers; thus, there is surface recombination on each surface. This section calculates the J_0 of the UTSi solar cell after introducing the surface recombination. According to Table 2, the SRV value of the SiO_xN_y passivated n front surface is less than 13 cm/s; According to Table 3, the SRV value of the SiO_2 passivated p^+ rear surface is 1551–1677 cm/s, and 1640 cm/s is chosen to calculate the new J_0 for rear emitter (J_{0es}) because it is very close to the mean value and also consistent with the value reported by King. The rest parameters in this calculation are the same as those in the calculation of Table 1. The J_0 values for each layer and the corresponding V_{oc} are shown in Table 4. The V_{oc} decrease from 767.0 mV to 710.1 mV is caused by the recombination on the SiO_xN_y passivated surface. Since a maximum SRV is used in this calculation, 710.1 mV is a minimum value; in other words, a higher V_{oc} at this step is possible, such as when the front SRV is 5 cm/s, the corresponding V_{oc} is 725 mV. V_{oc} decrease from 710.1 mV to 687.0 mV is caused by recombination on the SiO_2 passivated p^+ surface.

Table 4. J_0 and iV_{oc} of the UTSi solar cell when passivated by SiO_xN_y and SiO_2. $J_{0b} + J_{0e}$ is from Table 1, and J_{0bs} is the reverse saturation current density of the base and J_{0es} is the reverse saturation current density of the emitter when taking SRV into consideration.

Steps	Component	J_0 (A/cm^2)	V_{oc} (mV)	Steps
1	$J_{0b} + J_{0e}$	4.76×10^{-15}	767.0	Maximum
2	J_{0bs}	4.23×10^{-14}	>710.1	Front SiO_xN_y
--	J_{0es}	6.12×10^{-14}	--	--
3	$J_{0bs} + J_{0es}$	1.04×10^{-13}	687.0	Front SiO_xN_y + Rear SiO_2

3.4. Measured V_{oc} on Test Samples

To verify the above calculated V_{oc}, test samples based on epi on FZ wafers were designed. These test samples had a similar structure to that of the UTSi solar cell, excluding the fact that the ultrathin silicon in the UTSi solar cell was supported by a steel substrate and the epitaxial layers in the test samples were grown directly on FZ thus no foreign support was needed. Figure 4 shows the structure of these test samples. Again, in the FZ substrate, bulk recombination is negligible and surface recombination dominates the final iV_{oc}. These test samples were processed together with the UTSi solar cells and control samples to eliminate extraneous variables during fabrication. Table 5 lists the lifetime and iV_{oc} values of the test samples measured using a Sinton lifetime tester. These measured iV_{oc} values are between 682–703 mV, and their mean value is 691.7 mV, consistent with the calculated value of 687.0 mV in Table 4.

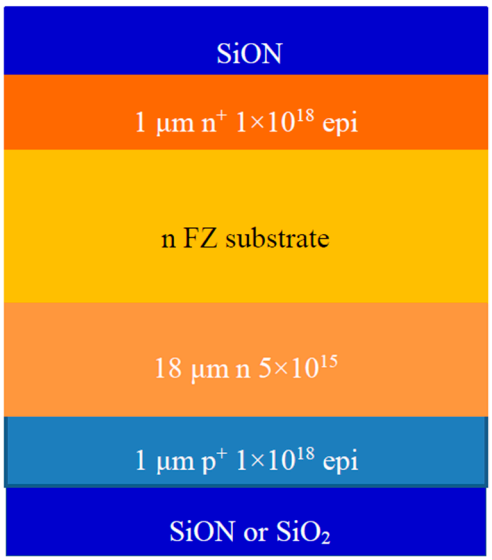

Figure 4. Structure of the test samples for the UTSi solar cells based on epi on FZ wafer.

Table 5. Lifetime and iV_{oc} of epi on FZ wafer test samples.

ID	Lifetime (μs)	iV_{oc} (mV)
Test samples	383–674	682–703

4. V_{oc} Loss Due to Rear Surface Metallization

4.1. V_{oc} Losses Calculation

The reverse saturation current density (J_{0e}) of the emitter is composed of recombination both at the passivated surface (J_{0es}) and at the point contact region ($J_{0e\text{-}pc}$). Therefore, $J_{0e} = J_{0es}(1-f) + J_{0e-pc}$ where $J_{0pc} = J_{100} f(1 + \frac{4\ln 2 \times W}{\pi r} + \frac{W^2}{8r^2})$ was introduced when the passivated emitter and rear cell (PERC) solar cell was invented [14], J_{100} is the saturation current density with 100% rear contact coverage, f is the contact ratio 0.56%, r is the radius of the contact points and W is the cell thickness. The SRV of the point contact region is 10^7 cm/s [15]. Table 6 summarizes the calculated J_0 and V_{oc} values.

Table 6. J_0 and V_{oc} values of the thin silicon solar cell after rear surface metallization. $J_{0e\text{-}pc}$ is the reverse saturation current density introduced by the point contact on the rear surface.

Steps	Component	J_0 (A/cm^2)	V_{oc} (mV)	Steps
3	$J_{0bs} + J_{0es}$	1.04×10^{-13}	687.0	Rear SiO_2
--	$J_{0e\text{-}pc}$	9.76×10^{-14}	--	--
4	$J_{0bs} + J_{0es} + J_{0e\text{-}pc}$	2.02×10^{-13}	670.0	Rear contact

4.2. Measured V_{oc} on Test Samples

To confirm the calculated results in Table 6 experimentally, test samples based on epitaxial on FZ wafers were made to examine the recombination introduced by the rear pattern and contacts. The test

structures are shown in Figure 5, where the left image is the structure after passivation, the right image is the structure after point contact patterning and metallization. The minority carrier lifetime, and iV_{oc} and V_{oc} of these samples were measured at each step as shown in Table 7. The rear point contact patterning and metallization led to a slight decrease in lifetime, iV_{oc} and V_{oc}. The best V_{oc} measured after aluminium metallization was as high as 673 mV. The final V_{oc} values were in the range of 665–673 mV, which are consistent with the calculated value of 670 mV in Table 5. This result demonstrates that the calculation is valid.

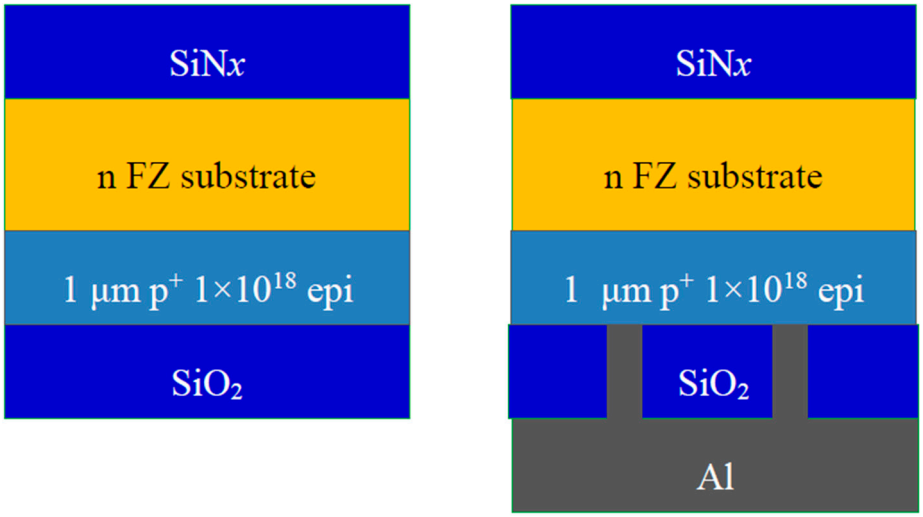

Figure 5. Test sample before rear contact patterning (**left**), PERC rear contact with Al metallization (**right**).

Table 7. Lifetime, iV_{oc} and V_{oc} change of test structures before and after rear surface metallization.

Steps	**Front SiO_xN_y/Rear SiO_2**		**Rear metallization**
Values	Lifetime (μs)	iV_{oc} (mV)	V_{oc} (mV)
	445.2	685.4	665–673

5. V_{oc} Loss Due to Front Surface Metallization

5.1. Laser Doping

The n type front surface is patterned by laser doping, which introduces locally heavy doping within openings. However, laser doping inevitably introduces damage to the surface and bulk of the silicon solar cell. Laser damage can be partially healed by subsequent annealing. The V_{oc} loss depends on the power, speed and wavelength of the laser, the structure of the solar cell and the subsequent annealing temperature. A minimum V_{oc} loss of 6.1 mV has been reported [16]. Figure 6 illustrates this laser doping process on a test sample made of epi on FZ wafer, whose front surface was shallowly textured and passivated by SiO_xN_y. Based on our experiments, the V_{oc} loss at this laser doping step can be 10–20 mV, and Figure 7 shows the iV_{oc} changes on a test sample in this process.

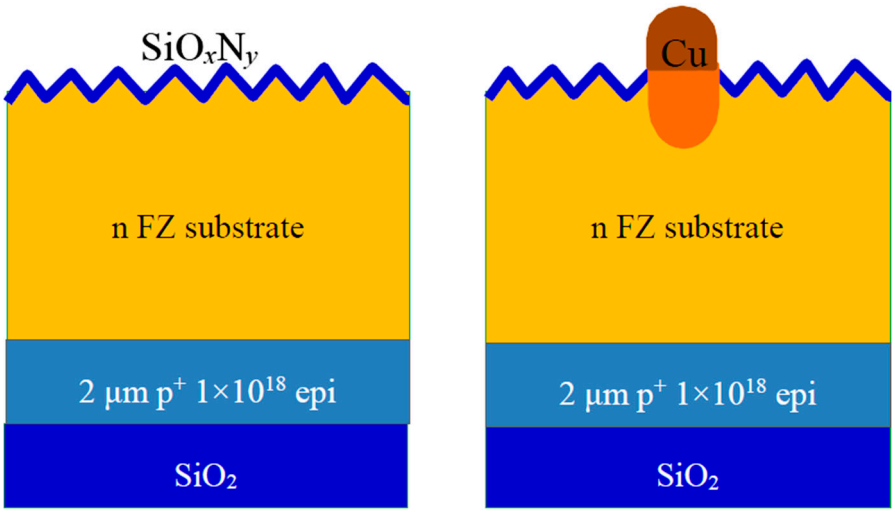

Figure 6. Laser doping on a textured surface, where the front surface is passivated by SiO_xN_y (**left**) and patterned by laser doping (**right**).

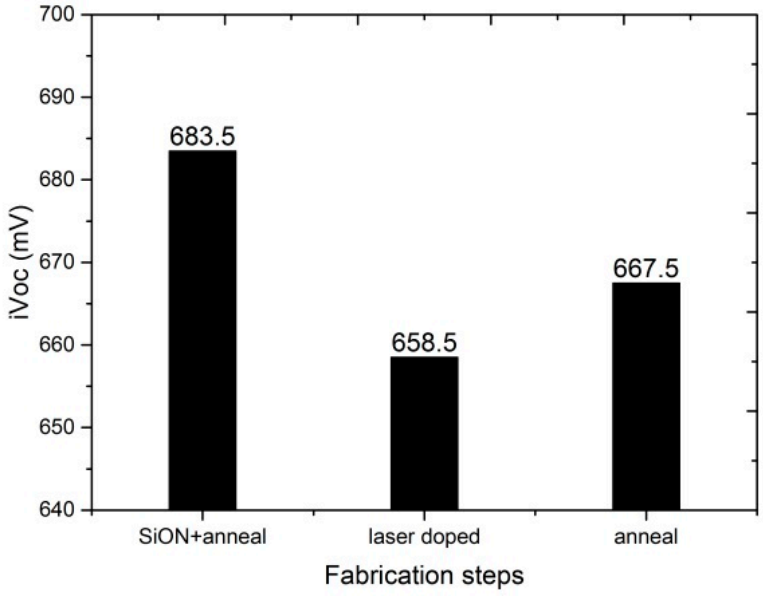

Figure 7. iV_{oc} changes in the laser doping process on a test sample epi layer on FZ wafer.

5.2. Metallization

Laser doping is followed by self-aligned metallization (Ni/Cu plating). According to the experimental results, the metallization caused V_{oc} losses are no more than 5 mV. V_{oc} increases after metallization were even observed. This is because the V_{oc} measured before metallization is a local value within the laser opening, while the measurement on the grid represents an average V_{oc} of the whole cell.

According to the measurements, the average V_{oc} loss due to laser doping and metallization is 20 mV. So, after these two steps, V_{oc} decreased from the previous 670.0 mV to 650.0 mV. 650.0 mV is a reasonable estimation, since a maximum V_{oc} of 653 mV was measured in the UTSi solar cells at this processing stage. Table 8 lists the V_{oc} and J_0 changes due to front surface processing.

Table 8. J_0 and V_{oc} of the thin silicon solar cell after the front surface laser doping and metallization. $J_{0b\text{-}ld}$ is the reverse saturation current density introduced by the laser doping and metallization on the front surface.

Steps	Component	J_0 (A/cm^2)	V_{oc} (mV)	Steps
4	$J_{0bs} + J_{0es} + J_{0e\text{-}pc}$	2.02×10^{-13}	670.0	Rear contact
--	$J_{0b\text{-}ld}$	2.14×10^{-13}	--	--
5	$J_{0bs} + J_{0es} + J_{0e\text{-}pc} + J_{0b\text{-}ld}$	4.16×10^{-13}	650.0	Laser doping/metallization

6. V_{oc} Loss Due to Edge Isolation

Edge isolation is an important step for either removing shunts on old edges or redefining active areas of a solar cell. Edge isolation approaches include laser grooving, sawing, grinding with sandpaper and plasma etching [17]. V_{oc} increases have been observed after removing shunts on old edges [18]. In our experiment, the major purpose of edge isolation is to redefine the active areas of a solar cell, and is achieved by a combined process of laser cutting and chemical edge cleaning. A 3 × 3 cm^2 raw sample was edge isolated into a 2 × 2 cm^2 cell. Based the measurements before and after isolation, a V_{oc} loss as low as 10 mV can be achieved on both the UTSi solar cells on steel and the epitaxial layer on FZ samples. Table 9 lists J_0 and V_{oc} values by assuming 10 mV loss during this step. The final V_{oc} is 640.0 mV, which is very close to the best V_{oc} of 642.3 mV measured in the finished UTSi cells on steel.

Table 9. J_0 and V_{oc} of the UTSi solar cell after edge isolation. $J_{0\text{-}edge}$ is the reverse saturation current density introduced by edge isolation.

Steps	Component	J_0 (mA/cm^2)	V_{oc} (mV)	Steps
5	$J_{0bs} + J_{0es} + J_{0e\text{-}pc} + J_{0b\text{-}ld}$	4.16×10^{-13}	650.0	Laser doping/metallization
--	$J_{0\text{-}edge}$	1.93×10^{-13}	--	--
6	$J_{0bs} + J_{0es} + J_{0e\text{-}pc} + J_{0b\text{-}ld} + J_{0\text{-}edge}$	6.09×10^{-13}	640.0	Edge isolation

7. Summary of V_{oc} Losses

Figure 8 summarizes the V_{oc} at each step. This solar cell has a very high V_{oc} potential when assuming an SRV of 0 cm/s. Each subsequent processing step, such as non-ideal passivation of the front and rear surfaces, laser doping on the front surface, metallization on both front and rear surfaces and edge isolation, introduces an increase of recombination, and thus an increase in J_0. Calculation results and measurement results on either FZ test structures or the UTSi solar cells on steel are coincident with each other. The best achieved V_{oc} was of 642.3 mV. The primary V_{oc} loss is due to the recombination at the SiO_2 passivated p^+ surface. Thus the greatest opportunity to improve V_{oc} lies in the improvement of the rear surface passivation. The second dominant V_{oc} loss that can be further reduced is the 10 mV loss due to edge isolation. Once the cell size increases from 2 × 2 cm^2 to 10 × 10 cm^2, edge recombination is less critical and zero V_{oc} loss is possible. The third largest V_{oc} loss is caused by the relatively high front SRV. If the SRV decreases from 13 to 5 cm/s, there will be another 15 mV increase. Improvements in these three aspects can lead to a V_{oc} increase of more than 40 mV, hence a V_{oc} of more than 680 mV can be achieved in the UTSi solar cells.

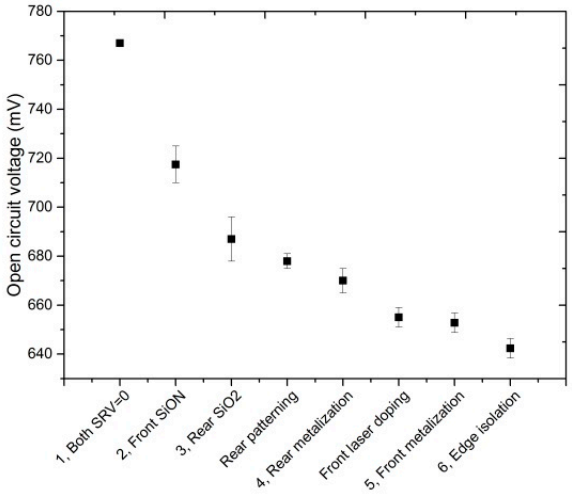

Figure 8. Summary of V_{oc} variation during the fabrication process. The first data point was from the calculation, while the remaining data points were based on the measured results, thus with error bars.

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Author Contributions

Lu Wang and Allen Barnett conceived and designed the experiments; Lu Wang, Jianshu Han, Anthony Lochtefeld and Andrew Gerger performed the experiments; Lu Wang analyzed the data and wrote the paper.

Conflicts of Interest

The authors declare no conflict of interest.

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