A novel ultra-high compliance, high output impedance low power very accurate high performance current mirror

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ABSTRACT

In this paper a novel ultra-high compliance, low power, very accurate and high output impedance current mirror/source is proposed. Deliberately composed elements and a good combination (for a mutual auto control action) of negative and positive feedbacks in the proposed circuit made it unique in gathering ultra-high compliances, high output impedance and high accuracy ever demanded merits. The principle of operation of this unique structure is discussed, its most important formulas are derived and its outstanding performance is verified by HSPICE simulation in TSMC 0.18 μm CMOS, BSIM3 and Level49 technology. Simulation results with 1 V power supply and 8 μA input current show an input and output minimum voltages of 0.058 and 0.055 V, respectively, which interestingly provide the highest yet reported compliances for current mirrors implemented by regular CMOS technology. Besides an input resistance of 13.3 kΩ, an extremely high output resistance of 34.3 GΩ and −3 dB cutoff frequency of 210 MHz are achieved for the proposed circuit while it consumes only 42.5 μW and its current transfer error (at bias point) is the excellent value of 0.02%.

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1. Introduction

Current mirrors are one of the essential widely used building blocks in analog integrated circuits. They are used to perform current amplification, biasing, active loading and level shifting. Hence, their efficient design improves the overall performance of the system. The most important parameters of current mirrors are accuracy, input/output compliances, input/output impedances, frequency bandwidth, linearity, noise and sensitivity to changes in load impedance. In many high performance applications, the performance of the simple current mirror is inadequate, especially due to low output resistance and high current transfer error. The traditional method to increase the output impedance and improve the accuracy is using cascode transistors to (equalize drain–source voltages of mirror transistors and) reduce channel length modulation effect. However cascoding the transistors increases the required supply voltage and decreases input/output compliances, which is not compatible with today’s technology trend. Due to technology down scaling and its intrinsic benefits, the trend in VLSI design is to reduce voltage supply. Hence, low voltage and low power circuit designs are in great demand. It can be found that there are many researches dealing with methods to improve the performance of low voltage current mirrors. Some of these methods are based on using level shifters [1,2], FGMOS transistors [3,4] and bulk driven schemes [5–7]. Although these methods operate with low power supplies and maintain high compliances, but unfortunately they suffer from some drawbacks. Two first solutions introduce extra offset to the output current. Offset can be canceled using adaptive biasing, but at the cost of increasing power consumption and extra circuit complexity. FGMOS transistors suffer from charge entrapment during fabrication process, large capacitance DC biasing and special technology that requires higher design cost comparing to traditional transistors [8–10]. Moreover, they are not suitable for DC processing. Bulk driven current mirrors also suffer from current offset problem, low bandwidth, high power consumption and limitations imposed by implementation process [6].

One of most widely used current mirrors is the low voltage cascode one. It has moderately low input and high output impedances, moderately low input and output voltages and high accuracy. To further decrease its input voltage and impedance, the input current can be applied to the drain of the transistor M 1 [11] (Fig. 1a). However this method introduces some offset to the output current. This offset current can be eliminated by subtracting it from the input or the output node. However it increases the circuit’s complexity and requires much more attention in the design of biasing network. The better solution is obtained using an amplifier to equalize the drain–source voltages of mirror transistors. The other advantage of this solution is that it also improves other specifications of current mirror such as input and output impedances. This method is implemented in [12–14]. In [12] in order to
The proposed current mirror, conceptual schematic shown in Fig. 2 consists of a high swing cascode current mirror (M1–M4, with M4 transistor connected as diode), M3 as output transistor and an amplifier with gain amplitude of \( "A" \). The high swing cascode is biased with \( I_{b1} = I_{b2} = I_b \) currents and its input impedance is reduced using an FVF block [18] at input node and is driven by the input current signal \( I_{in} \). Both cascode transistors M1 and M4 experience the same bias current; hence \( V_{ds1} \) is set equal to \( V_{ds2} \), prohibiting the channel length modulation effect and thus a very high accurate result is attained. M4, the diode connected cascode transistor, makes a separate biasing voltage source unnecessary. This transistor, on the other hand, provides the input and output nodes with an extra positive feedback loop, which increases the performance of the block without using extra circuitry. This structure includes two nested feedback loops in the input side. One of them is a negative shunt feedback implemented with an FVF while the other one is a positive series type consisting of transistors M1–M4. Both loops act simultaneously and are specially devised to reduce the minimum input voltage, \( v_{in,min} \), and the input impedance. Similarly, the output side includes two feedback loops, one of them is a negative series implemented by transistors M4–M5 and amplifier of \( "A" \) and the next one is a positive shunt feedback consisting of transistors M1–M4. These two loops act simultaneously and are specially arranged to reduce the minimum output voltage, \( v_{out,min} \), and increase the output impedance. In conventional method a negative series feedback is used to increase the output impedance. This reduces the output compliance by at least \( V_{dsat} \). In other word the feedback acts while the output voltage is greater than \( 2V_{dsat} \). By further decreasing the output voltage the feedback gain falls rapidly, causing the output impedance to be decreased rapidly due to the transistors entering the triode region.

Based on conventional definitions, MOS transistor linear region occurs when its output voltage becomes lower than \( V_{DS,off} = V_{GS} - V_{GS,off} \), which leads to sharp reduction in output current versus voltage reduction. In other words for a transistor with constant \( V_{GS} \) voltage, the channel length modulation causes significant reduction in transistor output resistance. This means that \( I_{DS} \) becomes very sensitive to variation in \( V_{DS} \) in this region.

According to \( I_{DS} = \beta (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \), the transistor current, \( I_{DS} \), can be varied by both \( V_{GS} \) and \( V_{DS} \). When transistor output voltage approaches to negative supply (here ground), then \( V_{DS} \) will
decrease causing reduction in transistor current \( \text{IDS} \), of course if \( V_{GS} \) remains constant. Now consider the case that \( V_{GS} \) can be increased to a value, which despite of \( V_{DS} \) decrement, maintains the same \( \text{IDS} \). In such a case if it is arranged then makes the transistor current \( \text{IDS} \) well robust against the output voltage variations. This is exactly what has arranged by the novel structure of the proposed current mirror (Fig. 2).

To explain the event in more detail, recalling the aforementioned descriptions about the nested feedbacks in the output node and supposing all transistors except \( M_1 \) and \( M_2 \) (which are always in triode region as will be discussed later) in saturation region, let us assume that due to some unwanted condition the output voltage is decreased from its initial value, then the principal of operation for the proposed circuit can be categorized in two parts: (1) \( M_5 \) is in saturation region and every variation in output voltage is extremely attenuated by negative feedback (related to \( M_5, M_4 \) and amplifier loop gain) that does not vary \( V_{ds} \). In this condition the negative feedback is dominant and the output impedance will be maintained extremely high, which preserves the previous value of the output current (Fig. 3). (2) With further reduction in output voltage, \( M_5 \) will enter the triode region making the negative feedback much less effective; thus \( V_{ds} \) will trace the output voltage variation through \( M_5 \). In this condition the positive feedback dominates and will increase the \( V_{GST,2} \) voltage (due to the output voltage reduction) to compensate the \( \text{IDS} \) deviation, thus keeping it constant (Fig. 3). In other words, since the constant current of \( \text{Ib2} \) flows through \( M_4 \), its gate voltage will follow \( V_{ds} \), which then boosts the gate voltage of mirror transistors \( (M_1 \text{ and } M_2) \) by means of \( M_3 \). The resulted increment in \( V_{GST,2} \) will compensate the reduction in \( \text{Ib2} \), which is caused by channel length modulation effect. In practice, although the transistor has been inevitably entered the linear region, but the aforementioned technique operates such that it keeps \( \text{Ib2} \) fixed by increasing \( V_{GST,2} \) so that we have \( R_{out} = \frac{\Delta V_{GST}}{\Delta \text{Ib2}} |_{\text{Mib=-5}} \) which makes the output impedance very large too. On the other side, in the proposed structure the embedded positive shunt feedback allows output voltage to approach to negative supply (here ground) meanwhile preserving its high output resistance and accurate current transfer features. It seems that the linear region boundary is shifted to lower output voltages, the greatly ever demanded event, now realized by this unique structure.

The conceptual description of the proposed method based on positive feedback is demonstrated in Fig. 3. Some recently proposed techniques used positive feedback schemes and gained high output impedance while achieving very low output voltages [19]. This is in fact a great achievement granted by special feedback arrangement and results a very wide dynamic range.

A very simple construction for gain amplifier suitable for the proposed current mirror of Fig. 2 is shown in Fig. 4. As shown it is implemented by only two transistors (configuring a self-cascode scheme) and a bias current of \( \text{IbA} \).

### 3. Circuit analysis

Analytical formulations to extract parameters of the proposed current mirror are performed in the following subsections, assuming that the source of each transistor is connected to its body. The simulations are also performed based on this assumption.

#### 3.1. Output impedance analysis

In the following analysis, \( g_{m}, r_{o} \) and \( g_{ds} \) stand for the transconductance, the output resistance and the output conductance of the transistors. The transistors’ numbers are indicated as subscripts of these parameters. Subscript “\( p \)” is also used to indicate “\( p \)” type transistors.

\[
V_{out} = V_{ds} + V_{ds5}
\]  

(1)

![Fig. 3. Conceptual description of the proposed method based on positive feedback.](image)

![Fig. 4. Transistor implementation of the proposed current mirror.](image)
In this work, Eq. (14) is satisfied by (1) making $g_{m3}$ sufficiently small via choosing small ($W/L_2$) and ($W/L_4$) and (2) biasing $M_1$ and $M_2$ in their triode region, which cause $r_{o1}$ and $r_{o2}$ to be sufficiently small. These arrangements also help the current mirror to present high input and output compliances.

\[
A \approx \frac{g_{mAC}}{\frac{g_{dsb}g_{dcA}}{1 + g_{dsb}g_{dcA}} + \frac{g_{dsA}g_{dcA}}{1 + g_{dsA}g_{dcA}}}
\]  

(3)

Substituting Eqs. (2) and (3) in Eq. (1) gives

\[
v_{ds} = (I_{in} + g_{m3}v_{gs})r_{o3}
\]  

(1)

\[
v_{g5} = (A + 1)v_{dx}
\]  

(2)

\[
A \approx g_{mA} \left( \frac{g_{dsA}g_{dc}}{1 + g_{dsA}g_{dc}} \right)
\]  

(4)

\[
v_{out} = v_{ds} + g_{m5}r_{o5}(A + 1)v_{dx} + r_{o5}I_{out}
\]  

(5)

\[
v_{d2} = (r_{o2} || r_{o3}) (I_{out} - g_{m2}v_{ds})
\]  

(6)

\[
v_{d3} = -g_{m3} \left( \frac{1}{r_{o1} || r_{o3}r_{o1}} \right) (v_{ds} - v_{d1})
\]  

(7)

\[
v_{d1} = -\frac{g_{m1}}{g_{m3}} v_{d3}
\]  

(8)

This equation can be simplified as

\[
v_{d3} = -\frac{g_{m3} \left( \frac{1}{r_{o1} || r_{o3}r_{o1}} \right) v_{d2}}{1 + g_{m1} \left( \frac{1}{r_{o1} || r_{o3}r_{o1}} \right) v_{d3}}
\]  

(9)

Substituting Eq. (9) in Eq. (5) gives

\[
v_{d2} = \frac{\left( \frac{r_{o2}}{r_{o2} || r_{o3}} \right)}{1 - \frac{g_{m2}r_{o1}}{1 + g_{m2}r_{o1} \left( \frac{1}{r_{o2} || r_{o3}} \right)}}
\]  

(10)

Finally, substituting Eq. (10) in Eq. (4) gives

\[
v_{out} = \frac{r_{o5} + \left( \frac{1 + g_{m5}r_{o5}(A + 1)}{1 + g_{m5}r_{o5} \left( \frac{1}{r_{o2} || r_{o3}} \right)} \right) I_{out}}{1 - \frac{g_{m2}r_{o1}}{1 + g_{m2}r_{o1} \left( \frac{1}{r_{o2} || r_{o3}} \right)}}
\]  

(11)

\[
R_{out} = \frac{r_{o5} + \left( \frac{1 + g_{m5}r_{o5}(A + 1)}{1 + g_{m5}r_{o5} \left( \frac{1}{r_{o2} || r_{o3}} \right)} \right)}{1 - \frac{g_{m2}r_{o1}}{1 + g_{m2}r_{o1} \left( \frac{1}{r_{o2} || r_{o3}} \right)}}
\]  

(12)

Output impedance is then approximated as

\[
R_{out} \approx \frac{g_{m5}r_{o5}(A + 1) \left( \frac{1}{r_{o2} || r_{o3}} \right)}{1 - \frac{g_{m2}r_{o1}}{1 + g_{m2}r_{o1} \left( \frac{1}{r_{o2} || r_{o3}} \right)}}
\]  

(13)

From Eq. (13) it is derived that the output resistance is capable to have negative or positive values. Also assuming ideal circumstances for the fabrication process an infinite resistance seems to be achievable by adjusting the transistors’ aspect ratios. In most applications negative resistance is not required thus to avoid this condition, the following relation should be satisfied:

\[
g_{m3} \left( \frac{1}{r_{o2} || r_{o3}} \right) \leq 1
\]  

(14)

\[v_{ds} = (l_{in} + g_{m3}v_{gs})r_{o3}
\]

\[v_{g5} = (A + 1)v_{dx}
\]

**Fig. 5.** Small signal equivalent circuit of the proposed current mirror ($v_{ds}=v_{g5}=v_{gs}$).

**Fig. 6.** $I_{out}$ versus $V_{out}$ (reflecting $g_{out}=R_{out}^{-1}$).

**Fig. 7.** $V_{gs}$ as a function of $I_{in}$.

**Fig. 8.** Output current versus input current.
3.2. Input impedance analysis

\[ I_{in} = \frac{g_{m} V_{ds} + g_{d1} V_{in}}{g_{m} + \frac{1}{g_{d1}} + \frac{1}{g_{d3}}} \quad (15) \]

\[ V_{d3} = -g_{m} (1 + \frac{1}{g_{d1}}) (V_{g3} - V_{in}) \quad (16) \]

\[ V_{g3} = -\frac{g_{m}}{g_{m} + \frac{1}{g_{d1}} + \frac{1}{g_{d3}}} \quad (17) \]

Substituting Eq. (17) in Eq. (16) gives

\[ V_{d3} = \frac{g_{d3} g_{m} (A + 1)}{g_{m} + \frac{1}{g_{d1} (A + 1)}} \cdot V_{in} \quad (18) \]

Substituting Eq. (18) in Eq. (15) gives

\[ I_{in} = \frac{g_{m} g_{d3} g_{d1} (A + 1) + g_{d1} (A + 1) - g_{m} g_{d3} g_{d1} g_{d1} (A + 1)}{g_{m} g_{d3} g_{d1} g_{d1} (A + 1)} \cdot V_{in} \quad (19) \]

\[ R_{in} = \frac{g_{m} g_{d3} g_{d1} (A + 1) - g_{m} g_{d3} g_{d1} g_{d1} (A + 1)}{g_{m} g_{d3} g_{d1} g_{d1} (A + 1)} \cdot V_{in} \quad (20) \]

where

\[ d1 = g_{m} g_{d1} g_{d1} (A + 1) \]

\[ d2 = g_{d1} g_{m} g_{d3} g_{d1} g_{d1} (A + 1) \]

The input impedance can be simplified as

\[ R_{in} = \frac{g_{m} g_{d3} g_{d1} (A + 1) - g_{m} g_{d3} g_{d1} g_{d1} (A + 1)}{g_{m} g_{d3} g_{d1} g_{d1} (A + 1)} \cdot V_{in} \quad (21) \]

The same as output resistance, it is proved in Eq. (22) that the input resistance can also get positive, zero and finally negative values just by adjusting transistors’ aspect ratios. This ability makes the proposed circuit also well suited for some special applications where negative resistances are needed. On the other hand, to avoid negative input resistance wherever it is undesirable for the considered application, amplifiers’ gain must be kept high enough, which also helps to decrease the input resistance (see Eq. (22)).

3.3. Current transfer analysis

Using KCL at input node \( (v_{in}) \) of proposed circuit (Fig. 5) and performing some approximations gives

\[ I_{in} = \frac{V_{ds} (g_{d3} + g_{m} + 1) + g_{d3} V_{in}}{g_{m} + 1 + g_{d3}} \quad (23) \]

Similarly using KCL at other nodes of proposed circuit results

\[ I_{out} = \frac{V_{d2} (g_{d3} + g_{d2} + 1) + V_{in} (g_{d2} + g_{m} + g_{d3})}{g_{d2} + g_{m} + 1 + g_{d3}} \quad (24) \]

\[ V_{d2} = \frac{g_{d3} (1 + \frac{1}{g_{d4}})}{g_{d2}} V_{g3} = \frac{V_{d3}}{g_{d2}} \quad (25) \]

\[ V_{in} = \frac{g_{d4} + 1 + \frac{1}{R_{op}}}{g_{m}} V_{d2} + V_{g3} \quad (26) \]

\[ \frac{V_{g5}}{g_{m}} = \frac{V_{d2} + V_{g3}}{g_{m}} \quad (27) \]

\[ V_{d4} = \frac{V_{g3} + (1/g_{d4}) + g_{d4} V_{d3}}{g_{m}} \quad (28) \]

\[ V_{g5} = \frac{g_{d2} + g_{d4} - g_{m} (1 + g_{d3})}{g_{d2} + g_{d4}} \quad (29) \]

Now substituting Eq. (28) in Eq. (29) and performing some simplifications, we obtain

\[ V_{g5} = -\frac{g_{m} (1 + g_{d3})}{g_{d2} + g_{d4}} V_{g3} \quad (30) \]

Substituting Eq. (29) in Eq. (27) gives

\[ V_{d2} = \frac{I_{out}}{g_{m}} g_{d2} V_{g3} \quad (31) \]

Substituting Eq. (31) in Eq. (24) gives

\[ I_{out} = \frac{V_{d2} (g_{d3} + g_{d2} + 1) + V_{in} (g_{d2} + g_{m} + g_{d3})}{g_{d2} + g_{m} + 1 + g_{d3}} \quad (32) \]

Substituting Eq. (25) in Eq. (31) gives

\[ V_{g3} = \frac{I_{out} (g_{d2} + g_{m} - g_{d3})}{g_{m} + g_{d2} + g_{d3}} \quad (33) \]

Substituting Eqs. (33) and (26) in Eq. (1) and performing some simplifications gives

\[ I_{in} = \frac{V_{ds} (g_{d3} + 1 + g_{d2})}{g_{m} (1 + g_{d3})} \quad (34) \]

Substituting Eq. (33) in Eq. (32) and performing some simplifications give

\[ V_{d3} = \frac{I_{out}}{g_{m}} \quad (35) \]

Substituting Eq. (35) in Eq. (34) gives

\[ \lambda = \frac{I_{out}}{I_{in}} = \frac{1}{1 + \frac{g_{m} g_{d3}}{g_{d1} g_{d1}}} \quad (36) \]

4. Simulation results

SPICE simulations are carried out using the TSMC 0.18 μm, BSIM3, Level49 and CMOS technologies with HSPICE utilizing single 1 V power supply. Load resistance, RL, of 3 kΩ is used. For all structures (simple, LV cascode, RGC and the proposed one) the aspect ratios of the transistors (if used) are \( M1\_M2 = 45/0.54, M3\_M4 = 4/0.27, M5 = 36/0.18, M6 = 9/0.18, M7 = 9/0.18 \), and \( M_{RGC1-2} = 0.9/0.54 \). Bias currents of \( I_{b1} \) and \( I_{b2} \) are taken to have values of 5 and 2.5 μA, respectively. \( I_{in} \) is taken to have DC value of 15 μA. Fig. 6 shows the DC output characteristic with \( V_{out} \) swept from 0 to 1 V and \( I_{in} \) stepped from 0 to 40 μA in steps of 10 μA. As shown in this figure, the proposed circuit exhibits extremely

<table>
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<th>Reference</th>
<th>[16]</th>
<th>[17]</th>
<th>[12]</th>
<th>[13]</th>
<th>[14]</th>
<th>Simple</th>
<th>LVC (Fig. 1a)</th>
<th>RGC (Fig. 1b)</th>
<th>Proposed</th>
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<tr>
<td>( I_{in} ) (μA)</td>
<td>50</td>
<td>50</td>
<td>NA</td>
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<td>10</td>
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<tr>
<td>( I_{b} ) (μA)</td>
<td>10</td>
<td>5</td>
<td>110</td>
<td>50</td>
<td>25</td>
<td>NA</td>
<td>5</td>
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<tr>
<td>( V_{dm,mm} ) (V)</td>
<td>0.14</td>
<td>0.23</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>0.22</td>
<td>0.363</td>
<td>0.375</td>
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<tr>
<td>( V_{dc} ) (V)</td>
<td>0.25</td>
<td>0.3</td>
<td>0.2 to 0.4</td>
<td>0.23 at ( I_{in} = 10 ) μA</td>
<td>0.15</td>
<td>0.125</td>
<td>0.422</td>
<td>502</td>
<td>0.055</td>
</tr>
<tr>
<td>( R_{o} ) (Ω)</td>
<td>1333</td>
<td>800</td>
<td>0.75</td>
<td>0.012</td>
<td>0.01</td>
<td>1266</td>
<td>266.6</td>
<td>333</td>
<td>13.3</td>
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<tr>
<td>( R_{out} ) (Ω)</td>
<td>11 M</td>
<td>650 M</td>
<td>200 M</td>
<td>23.4</td>
<td>8 G</td>
<td>561 K</td>
<td>22.5 M</td>
<td>42.9 G</td>
<td>34.3 G</td>
</tr>
<tr>
<td>( R_{M}(MHz) )</td>
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<td>620</td>
<td>220</td>
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<td>270</td>
<td>340</td>
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<td>210</td>
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<tr>
<td>( \text{Current transfer error} ) (%)</td>
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<td>0.1</td>
<td>0.05</td>
<td>0.1</td>
<td>7</td>
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<td>35</td>
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<tr>
<td>( P ) (μW)</td>
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<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>30</td>
<td>40</td>
<td>50</td>
<td>42.5</td>
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<tr>
<td>( V_{supply} ) (V)</td>
<td>1.5</td>
<td>1.5</td>
<td>1.8</td>
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<th>0.5 μm AMI</th>
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<th>TSMC 0.18 μm</th>
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Table 1: Comparative results.
high output resistance of 34.3 GΩ along with much higher compliance voltage, which proves the good functionality of embedded positive feedback, making the structure suitable for ultra-low voltage applications. This figure also proves very high accuracy of output current together with negligible current offset, which makes the structure very preferable for modern ultra-high precision applications. Another more interested characteristic of current mirrors is dynamic range, which is depicted in Fig. 6 and validates the superior performance of proposed current mirror compared to other structures. Favorably the minimum input and output voltage of the proposed current mirror are reduced to 0.058 and 0.055 V, respectively, which promise ultra-high compliances at the input and the output nodes. Fig. 7 shows the input voltage as a function of input current. It is shown in Fig. 7 for a DC sweep of $I_{in}$ from 1 to 300 μA, the maximum input voltage variation was found to be 4 mV. Following the same type of measurements performed in [12,13], the aforementioned values correspond to an approximate input resistance of 13.3 Ω, which is also another merit of the proposed current mirror. This figure also proves the capability of the proposed circuit to operate at extremely low input voltages. Fig. 8 shows the output current versus input current sweep. It is shown that the current dynamic range of the proposed current mirror is wider than that of all other current mirrors, i.e. simple, LVC and RGC current mirrors, which are included in the simulations. Favorably the current transfer error is achieved to be as low as 0.02%. The total power consumption of the proposed current mirror is about 42.5 μW. The compared results are summarized in Table 1. For simulating the practical fabrication condition, the Monte Carlo analysis is performed applying 5% mismatch in transistors’ aspect ratios and threshold voltage with Gaussian distribution. The Monte Carlo simulation results are shown in Figs. 9–12. To further investigate the performance of the proposed circuit against PVT (process, VDD and temperature) variations, it is also simulated for various temperatures and supply voltages. The results are depicted in Figs. 13–18. These figures show that the fabrication process does not have significant effect on proposed circuit’s performance, which is another excellent achievement.

The frequency response, the input voltage versus the input current and the output voltage versus the output current for various temperatures of −25, 0, 25, 50 and 75 °C are depicted in Figs. 13–15.

The output current transient response applying sinusoid input current of “$15μ+1μ\sin(2\pi \times 210 \times 1E+6t)$” is shown in Fig. 16. The input voltage versus the input current and the output current versus the output voltage applying ±10% variations in power supply voltage are shown in Figs. 17 and 18, respectively.
5. Conclusion

A novel ultra-high compliance, very accurate and high output impedance current mirror is presented. As shown the proposed current mirror has a very low voltage and consumes very low power. Moreover it is very simple and its frequency response is relatively high. The circuit also has low input and high output impedances along with high current dynamic range and very low current transfer error. The simulation results are performed using
HSPICE/TSMC 0.18 μm, BSIM3, Level49 and CMOS technologies using single 1 V power supply. The proposed current mirror is the best choice for low voltage, highly accurate and high output impedance applications.

References