Active Compensation of Parasitic Capacitances for Very High Frequency CMOS DACs

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Abstract - High frequency DACs requiring an output buffer find a speed limitation in the overall input capacitive load of the buffer. This communication presents an active scheme for the compensation of such a load, including the parasitic capacitances coming from reversely biased junctions associated to analog switches. Computer simulations on a given architecture (10-bit DAC) show the effectiveness of the proposed approach.

I. INTRODUCTION

The requirements made of D/A converters for video applications have become more severe with the introduction of new television standards such as digital TV and HDTV. A resolution of 10 bits and clock rates in the range of many tens of MHz are necessary for the D/A converters used in these applications.

There is a very popular high-speed D/A architecture based on the current cell matrix principle [1] [2]. Here the current fed to the output node is given by the sum of a variable number of elementary current sources, depending on the input code to be converted. This type of D/A converter allows fast and accurate settling. However, glitches occurring at critical changes of the input code cause severe limitations, especially for HDTV applications. This problem can be reduced by using differential switches, whereby the current generated by an elementary cell is fed either to the output node or to a dummy node, in order to always keep all the current sources active. For this reason, a high power supply current is required to obtain the expected output swing [3]. Moreover, for high resolution applications a very careful mutual matching between the elementary current sources is also needed. This cannot be obtained in standard CMOS technology and, therefore, the current cell matrix approach requires trimming or calibration.

Solutions that overcome these limitations use resistor strings. An example is given by the intermeshed architecture in a matrix formation (see Fig. 1) [3] [4]. This solution allows a converter with high integral and differential linearity and with lower power consumption to be designed.

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Fig. 2. Simulations of the settling time of the DAC shown in Fig. 1 assuming n-channel switches, in a conventional 1.2 µm CMOS technology. It is evident that for a given technology and a given resolution, there is an intrinsic speed limitation. Usually, for very high resolution applications, the largest contribution is due to the parasitic capacitances of the analog switches. This paper proposes a solution that overcomes the above described limit by actively compensating the overall output capacitance.

II. PROPOSED SOLUTION

Fig. 3 shows the equivalent schematic diagram of the output section of the converter. \( V_i \) is the converted voltage delivered by the resistive matrix. The resistance \( R \) represents the series between the switches on-resistances and the equivalent resistance of the resistive matrix. The capacitor \( C_p \) is given by:

\[
C_p = C_{in,b} + 2 C_{sw, on} + (2^{N/2} - 1) C_{sw, off}
\]

where \( C_{in,b} \) is the input capacitance of the output buffer, \( C_{sw, on} \) and \( C_{sw, off} \) are the parasitic capacitances of a closed and an open switch, respectively, and \( N \) is the resolution of the converter.

It is evident that for a given accuracy the speed is limited by the time constant \( RC_p \) even when the optimum switch sizing is used. Dynamic performance can be improved by compensating the effect of the capacitance \( C_p \). Unfortunately, bootstrapping is not available since the second terminal of the parasitic is the substrate or a well. The problem can be solved by an active compensation of \( C_p \).

This technique is described in Fig. 4.

An additional capacitor \( C_2 \) connected to the input of the buffer is driven by the voltage \( kV_0 \) obtained from a suitable amplification of the voltage \( V_0 \). The voltage \( V_0 \) can be calculated as follows:

\[
V_0 (1 + s C_p R) (2)
\]

\[
V_i = \frac{1}{1 + s R (C_p - (k - 1) C_2)} (3)
\]

Therefore, the circuit has a single-pole transfer function. The equivalent capacitance \( C_{eq} \), which is multiplied by the resistance \( R \), is equal to

\[
C_{eq} = C_p - (k - 1) C_2 (4)
\]

The value of the new time constant, \( RC_{eq} \), depends on the gain \( k \) and on the value of the injection capacitance \( C_2 \). Proper values of \( k (k > 1) \) and \( C_2 \) give rise to a significant reduction in the time constant. In practice, the additional...
capacitor emulates a negative capacitance placed in parallel to $C_p$, thereby achieving the required compensation. To ensure the stability of the compensation loop, of course, $k$ must be smaller than $1 + C_p/C_2$.

The circuit implementation is shown in Fig. 5. A large-bandwidth operational amplifier is used to sense $V_0$ and to feed it to $C_2$ after a suitable amplification. The resistance $R_f$ is very large and is used just to ensure the low-frequency negative feedback. Of course, at high frequencies the factor $k$ is equal to $1 + C_3/C_4$.

III. SIMULATION RESULTS

The structure of Fig. 5 was simulated with ELDO [6]. The input capacitance of the output buffer was set equal to 1 pF. The ratio $k$ was set equal to 1.6. The values used for the resistance $R$ (3 kΩ) and the parasitic capacitance $C_p$ (2.5 pF) have been calculated from the equivalent circuit of the selection network of the 10-bit converter shown in Fig. 1.

Firstly, the structure was simulated assuming an ideal operational amplifier in the compensation loop. Fig. 6a shows the time response to a positive step of the compensated structure. The response of the non-compensated structure is also reported for comparison. It can be seen that with the used values of the capacitors, which guarantee a good margin of stability, the 0.1% settling time has been improved by a factor of 3. A similar improvement is obtained for a negative input step (Fig. 6b).

The structure was then simulated with a real operational amplifier in the feedback loop. To this end, a large-bandwidth two-stage operational amplifier was designed, using a conventional 1.2-μm CMOS double-poly double-metal technology; its performance is shown in Table I. The high speed has been achieved at the expenses of a relatively high biasing current.

The simulated time response of the compensated structure is shown in Figs. 7a and 7b with an expanded vertical scale. The time response is still good, even though op-amp nonidealties cause some degradation with respect to the ideal case.

| TABLE I |
| PERFORMANCE OF THE USED REAL OPERATIONAL AMPLIFIER |
| Supply voltage | 5 V |
| GBW | 150 MHz |
| DC Gain | 60 dB |
| S.R.+ | 270 V/μs |
| S.R.- | 260 V/μs |
| Power Dissipation | 15.3 mW |
The operation speed of the converter is increased by a factor as large as two, at the cost of a very small increase in silicon area occupation and power consumption.

IV. CONCLUSIONS

This paper has presented a scheme for the active compensation of parasitic capacitances, implemented by means of a high-frequency feedback loop. The proposed scheme is suited to use in high-frequency D/A converters based on resistive strings, where severe limitations on the achievable speed are imposed by the parasitic capacitances of the analog switches. Computer simulations have demonstrated that a great improvement has been obtained in the operation speed of the converter.

REFERENCES