CodeSyn: A Retargetable Code Synthesis System

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Abstract

This paper describes CodeSyn, a retargetable microcode synthesis system for application-specific instruction-set processors (ASIP). With respect to commercial or publicly available compilers, the main strengths of the CodeSyn system are in three main areas:

- Flexible and powerful instruction-set specification style which supports quick retargeting to new processors.
- A pattern matching algorithm and representation that supports complex instruction recognition and utilization.
- Allocation of special purpose registers taking into account the overlapping roles to which a given register can be assigned at a given time.

This leads to effective use of complex instructions and special purpose registers.

We illustrate the use of the CodeSyn system for an in-house custom DSP processor. This is a complex, application-specific, and extremely irregular architecture. It is also a very parallel architecture with a large micro-instruction word that allows up to five parallel operations. It is shown that the code produced by CodeSyn is within 20% of the compactness of hand-generated assembly code.