ABSTRACT
This paper presents the proposed silicon proven design techniques and the performance tradeoffs in the generic digitally variable gain amplifier (DVGA) designs. Two example designs were fabricated in a SiGe BiCMOS technology incorporating these design techniques and measured with good performance. Both the proposed designs, with low power consumption and compact size, are adapted in RF chipset with good interface capability between the RF front-end and the baseband chipsets.

INTRODUCTION

The variable gain amplifier (VGA), with either digital or analog gain control, is a key building block to control the gain of a RF transceiver chain to maintain the signal level according to the baseband requirements and support mobile applications with dynamic receiving and transmitting signal strengths [1]. The system requirement of a generic VGA in the RF transceiver is to provide a seamless (unchanged) integration with a minimum tolerance for the deviation of impedance matching, interface common mode DC, bandwidth, gain flatness, DC power consumption, and stability over the entire VGA's gain control range [1]. For the digitally variable gain amplifier (DVGA), the digital gain control can be achieved by discretely varying one of the design parameters using the transistor switches such as the load resistance, biasing voltage, biasing current, degeneration resistance and the transistor size, that influence the amplifier gain [1]. This paper discusses the basic DVGA design techniques implemented in the preliminary proposed DVGA [2] followed by the enhanced DVGA design techniques that are included in the second proposed DVGA design [3] that are required in a IEEE 802.11ad standard complaint RF transceiver chipsets.

BASIC DVGA DESIGN TECHNIQUES

To interface the baseband IC with a better common mode noise cancellation and at the other end with a balanced mixer design, the preliminary proposed DVGA [2] is fundamentally implemented as a fully differential topology at the expense of double the total power consumption. To meet this requirement and to provide a wideband gain independent characteristics, the first stage and the last stage of the DVGA [2] is implemented as fixed gain common base amplifier and emitter follower configuration, respectively. The DVGA [2] utilizes NMOS transistors for amplifier current biasing along with the digital gain control and the bipolar transistor (BJT) differential pairs for amplification. The DVGA core comprises of a common emitter (CE) differential amplifier along with a 6 bit digital gain control achieved by switching the bias current and correspondingly varying the transconductance. The proposed topology [2] achieves low power consumption and a compact layout without using capacitors and inductors. Hence the proposed design achieves a wideband matching, stable common mode DC interface, and a wide 3dB bandwidth along with a wideband gain flatness which is independent of the DVGA gain. The proposed design [2] additionally incorporates (1) a diode connected transistor linearizer that stabilizes the DVGA core amplifier’s voltage bias point which improves the linearity performance against the input power level, (2) linear gain control circuit by using NMOS transistor based current mirrors with binary weighted aspect ratios (W/L), and (3) power down

![Fig. 1: Proposed DVGA circuit schematic](attachment:dvga_circuit.png)
In the differential drive circuits that operate with differential drive input signals, the DC offset may be introduced due to the process mismatch and fabrication inaccuracies of the differential paired devices and may also be amplified, resulting in the saturation of the following building blocks along the RF signal chain [4]. This frequency independent DC component can be suppressed by using high pass filtering (HPF) in the RF forward path [3] or by subtracting the extracted DC component by feedback low pass filtering (LPF) DCOC schemes [5]-[6]. Among these two contrasting methods to eliminate the DC offsets, the scheme chosen for the proposed design [3] is based on the AC coupling with HPF DCOC technique with passive resistors and capacitors as shown in Figure 1. This technique avoids the large insertion loss (see Figure 2 (c)) that has to be compensated by using additional amplifiers in the feedback LPF and also need to overcome the potential feedback instability issues [6].

**Common mode feedback (CMFB)**

The direct coupled stages require common mode DC at the input and output to be unaltered by the amplifier gain variation. In the proposed design [3], the common mode DC is stabilized at the input terminals by using the input fixed gain amplifier and at the output by using the CMFB in the buffer stage as shown in Figure 1. This ensures a stable biasing of the blocks operating at this low frequency and avoids large decoupling capacitors. The CMFB circuit which is incorporated in the output buffer stage of the proposed DVGA [3] is a pair of back-to-back diode connected NMOS transistors that regulates the output DC voltage. The buffer stage provides a stable output common mode voltage using the CMFB and also provides a 100-Ω output wideband differential impedance matching.

**DB-linearity with temperature compensation**

The gain control in the proposed design [3] is achieved by changing transconductance of amplifying transistors by using the biasing current \( I_{\text{bias}} \). For obtaining a digitally controlled gain, the variable bias

![Exponential current converter](image)

**ENHANCED DESIGN TECHNIQUES**

To provide a robust system performance that is compliant with the IEEE 802.11ad baseband standard, the preliminary proposed DVGA design [2] is enhanced as the second proposed DVGA design [3] by incorporating DC offset cancellation (DCOC), common mode feedback (CMFB), linear-in-decibel gain control (dB-linearity) and an improved linearizer using transimpedance load as shown in Figure 1 with suitable performance tradeoffs.

**DC Offset Cancellation (DCOC)**

In the differential drive circuits that operate with differential drive input signals, the DC offset may be introduced due to the process mismatch and fabrication

![DCOC schemes](image)
current is provided from a NMOS transistor switch using mirrored current from a bandgap reference as shown in Figure 1. To regulate the power level of the baseband signal, the DVGA is incorporated as an automatic gain control (AGC) with a 6-bit digital gain control information determined by the baseband section and it is provided by using serial peripheral interface (SPI). To enhance the AGC settling time a linear-in-decibel gain variation is desired. This is achieved by using the bipolar junction transistor’s (BJT) exponential transfer characteristics as the dB-Linearizer shown in Figure 3. A PTAT current provides compensation against the temperature dependent BJT’s thermal voltage ($V_T$) as shown in Figure 1 [3].

**SIMULATION AND MEASUREMENT**

The microphotograph of both the proposed DVGA designs shown in Figure 4 are fabricated using 0.18μm SiGe BiCMOS process from Tower Jazz Semiconductors. The simulated gain and the noise figure plots of the proposed DVGA against the frequency are shown in Figure 5 and Figure 6, respectively. The plots indicate gain independent bandwidth and gain flatness over the operating frequency range. The measured gain transfer characteristics against the digital gain control information without dB-linearizer [2] and with dB-linearizer [3] is shown in Figure 7. The plot signifies that linear-in-decibel response accuracy is enhanced by the proposed dB-linearizer. Figure 8 highlights the gain independent matching achieved by the proposed DVGA topology. The measured performance of the proposed DVGA designs are summarized in Table I that provides the significance of the design tradeoffs of both the proposed designs. Table I summarizes and compares the measured performance of the proposed DVGA designs that are achieved as a result of the design tradeoffs acknowledged by each of the designs. By introducing dB-linearity, CMFB and DCOC that are essential for the application scenario, the design in [3] has to tradeoff the bandwidth, DC power consumption and die area as compared to [2]. The main merit of the proposed designs [2]-[3] over the [5]-[6] designs is the direct digital gain control that avoids the complex digital to analog converter (DAC).
TABLE I: MEASURED PERFORMANCE SUMMARY OF STATE-OF-THE-ART VGA

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm BiCMOS</td>
<td>0.18 μm BiCMOS</td>
<td>0.18 μm CMOS</td>
<td>90 nm CMOS</td>
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<tr>
<td>Gain range</td>
<td>-16.5 to 6.5 dB</td>
<td>-10.6 to 78 dB</td>
<td>-38.8 to 553 dB</td>
<td>-10 to 50 dB</td>
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<tr>
<td>3-dB bandwidth</td>
<td>DC to 5.6 GHz</td>
<td>2 M to 1.9 GHz</td>
<td>4 M to 0.9 GHz</td>
<td>0.1 M to 2.2 GHz</td>
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<tr>
<td>±0.75 dB flatness</td>
<td>DC to 4 GHz</td>
<td>2.8 M to 1.2 GHz</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power consumption</td>
<td>7.9 mW</td>
<td>12.2 mW</td>
<td>20.5 mW</td>
<td>2.5 mW</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>-17 to -27 dBm</td>
<td>≧ -12.5 dBm</td>
<td>-10.8 to -59.1 dBm</td>
<td>-13 to -55 dBm</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>16.5 to 27.1 dB</td>
<td>21.4 to 27.1 dB</td>
<td>6.8 dB (Sim.)</td>
<td>17 to 30</td>
</tr>
<tr>
<td>Core Area</td>
<td>0.01 mm$^2$</td>
<td>0.048 mm$^2$</td>
<td>0.195 mm$^2$</td>
<td>0.014 mm$^2$</td>
</tr>
<tr>
<td>dB-Linearity</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>On-chip DCOC</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Temperature stability</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Gain control mode</td>
<td>Digital</td>
<td>Digital</td>
<td>Analog</td>
<td>Analog</td>
</tr>
</tbody>
</table>

Fig. 7: Measured DVGA gain characteristics of both the proposed DVGA designs.

CONCLUSION

This paper provides the topology and design techniques implemented in two DVGA designs that are capable of providing enhanced and robust performance that are essential for the low power mobile applications. Both the compact designs provide an easy interface to the digital baseband chipset by using SPI and without the need of a complex digital to analog converter (DAC).

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REFERENCES


