An Accurate Quality Factor Tuning Scheme for IF and High-Q Continuous-Time Filters

Jan-Michael Stevenson, Member, IEEE, and Edgar Sánchez-Sinencio, Fellow, IEEE

Abstract—A quality factor (Q) tuning technique for IF and high-Q continuous-time filter biquads is proposed. The method is based on the existing magnitude locked loop Q-tuning technique, but it utilizes a modified version of the continuous-time adaptive least-mean-squares algorithm to improve the attainable precision. The technique is resistant to center frequency tuning errors, and can use an easily generated clock pulse as its reference signal. Discrete component tests were conducted, with the Q value being tuned to within 1.1% in the worst case. A test chip consisting of a fourth-order bandpass filter at 10.7 MHz with biquad Q-values of 20 was fabricated in a 1.2-µm n-well CMOS process. Experimental results show that the proposed Q-tuning scheme improves on existing methods, with measured accuracies of less than 1% error.

Index Terms—Bandpass filters, CMOS analog integrated circuits, continuous-time filters, IF systems, Q-factor.

I. INTRODUCTION

HIGH-FREQUENCY continuous-time filters are important parts of many electronics systems in today’s technology. These range from video applications [1] to the swiftly growing business of radio-frequency (RF) communications. The use of high-frequency and high-Q filters is widespread throughout the design of RF/IF transceivers [2].

One of the major goals of RF/IF researchers is to devise a “one-chip” transceiver which can operate with very little, if any, peripheral support. An important aspect of this is being able to place the high-frequency filters on chip, therefore, eliminating the large discrete filters which are now used. However, on-chip continuous-time filters have a large drawback inherent to them. The parasitics and process variations involved in monolithic filter implementations severely limit the attainable accuracy. In order to obtain the needed accuracy for these applications, the filters must be automatically tuned in both center frequency and quality factor (Q).

Several different schemes exist for both center frequency and Q-tuning. The methods of center frequency tuning have been proven to work very well, with accuracies of less than 1% error [3]. However, Q-tuning is not as well defined, with the best results shown in the literature to be within only 20–30% accuracy [4]. The focus of this research is to develop a quality factor tuning method which will improve the maximum attainable accuracy. Although an integrated test version of the proposed scheme is presented here, the main goal of its design was only to obtain the best possible Q-tuning. Therefore, normal filter performance specifications [such as distortion and signal-to-noise ratio (SNR)] were measured, but the circuit was not specifically designed to achieve set values.

For the remainder of the paper, the following topics will be discussed. In Section II, the major existing Q-tuning schemes will be described. Section III will focus on the theory behind a proposed Q-tuning method which uses the properties of adaptive signal processing. Section IV will describe the design of an integrated high-frequency bandpass filter which utilizes the proposed Q-tuning method. In Section V, the experimental results of a discrete component implementation and the fabricated test chip will be presented, and Section VI will summarize the work.

II. EXISTING QUALITY FACTOR TUNING TECHNIQUES

This section briefly describes the previously reported Q-tuning techniques found in the literature. For low frequencies and low quality factors, Q-tuning is normally unnecessary because the Q-value is set by a ratio of like components (resistors, capacitors, transconductors, etc.) [5]. But at high frequencies and high Q’s, tuning is a necessity due to the quality factor’s high sensitivity to parasitics. Existing Q-tuning methods are not very accurate, and much improvement is needed in this area.

All methods discussed below, as well as the method proposed in this paper, utilize the well documented master-slave tuning technique [6]. Obviously, the accuracy of tuning can only be as good as the matching between master and slave, but this is a well documented problem that is shared by most existing filter tuning techniques.

A. Magnitude Locked Loop

The magnitude locked loop (MLL) Q-tuning method utilizes the fact that the gain of a filter biquad at exactly its center frequency is equal to Q. This relationship is described in (1) and (2)

\[ H(s) = \frac{\omega_0 s}{s^2 + \omega_0^2} \]

\[ H(s)|_{s=j\omega_0} = \frac{j\omega_0^2}{-\omega_0^2 + \frac{j\omega_0^2}{Q} + \omega_0^2} = Q. \]
III. A PROPOSED QUALITY FACTOR TUNING SCHEME

Now that the existing methods of tuning have been discussed, a new $Q$-tuning scheme based on the magnitude locked loop technique and the adaptive technique is proposed. The new adaptive $Q$-tuning scheme is very similar to the magnitude matching method shown in Section II. However, the new technique uses the continuous-time LMS algorithm taken from adaptive signal processing as the mechanism for updating filter parameters, similar to the frequency tuning circuit used in [10]. This section will provide a brief analysis of the LMS algorithm with the slight modifications used in the tuning scheme, and then the tuning method itself will be discussed along with its inherent advantages.

A. Continuous-Time Adaptive LMS Algorithm

The continuous-time Widrow LMS algorithm matches the output of a tunable circuit to a desired output by minimizing the mean-squared error between them [11]. The equation for the adaptive LMS algorithm is

$$v(t) = \mu[d(t) - y(t)]g(t) \tag{3}$$

where $w(t)$ = tuning signals, $\mu$ = integration constant, $d(t)$ = desired response, $y(t)$ = actual response, and $g(t)$ = gradient signal (direction of tuning). Ideally, $g(t)$ is the partial derivative of $y(t)$ with respect to $w(t)$. A block diagram of the generalized LMS scheme is shown in Fig. 3. The quantity $[d(t) - y(t)]$ is also known as $e(t)$, or the error signal. The tuning signals $w(t)$ become constant (reach steady-state) when their time derivative $v(t)$ is zero or has a time average of zero. This occurs when $e(t)$ becomes zero, meaning that the actual output equals the desired output and the circuit is tuned. A more detailed derivation and explanation of the continuous-time LMS algorithm can be found in [12].

B. Description of Proposed $Q$-Tuning Scheme

The new $Q$-tuning scheme for filter biquads is a combination of the magnitude locked loop tuning method and the LMS algorithm. Its theory is very similar to the MLL method because it also is based on the fact that the gain of a biquad at exactly its center frequency is equal to $Q$ [see (1) and (2)]. However, instead of trying to match the magnitudes of the desired and actual sinusoids using peak detectors, the amplitudes of the sinusoids themselves can be matched by using the LMS algorithm.

The LMS algorithm as used in this tuning scheme is basically the same as the original version. The only difference is that while the original equation holds for several different tuning weights ($i = 1$ to $n$), only one tuning signal is needed in the $Q$-tuning version. The modified LMS equation for the new tuning scheme is

$$\dot{V}_Q(t) = \mu(V_{in} - V_{ip})V_{ip} \tag{4}$$

where $V_Q$ is the $Q$-tuning signal, $V_{in}$ is the input reference, and $V_{ip}$ is the bandpass output. The block diagram of the proposed $Q$-tuning scheme is given in Fig. 4. The input reference is a sinusoid (or clock pulse, see Section III-C)
that has a frequency equal to the center frequency of the filter \([\hat{V}_{in} \sin(\omega_0 t)]\). This signal will be available from the frequency tuning circuit which utilizes a phase-locked loop (PLL) with a voltage-controlled oscillator, but other types of reference signals such as clock pulses may also be used as shown later. Note that the input reference sinusoid is attenuated by a factor of \(Q_d\) before being input into the master biquad (\(Q_d\) is the desired \(Q\) value). This attenuation can be very accurate, especially in monolithic implementations, because it can be built with a voltage divider utilizing similar components (capacitors, etc.) [13], or by other techniques such as accurate current or voltage dividers [14], [15]. It can also be made scalable so that the desired \(Q\) will be programmable. The bandpass output is used in the tuning algorithm because it has a phase shift of zero degrees at the center frequency. Therefore, if the filter is ideally tuned, the error signal \([\hat{V}_{in}(t) - \hat{V}_{bp}(t)]\) would be exactly zero instead of having a time average of zero, leading to less noise on the \(Q\)-tuning voltage that is sent to the slave filter. The bandpass output will be

\[
\hat{V}_{bp} = \hat{V}_{in} \sin(\omega_0 t) = \frac{Q_d(V_Q)}{Q_d} \hat{V}_{in} \sin(\omega_0 t)
\]

or

\[
\hat{V}_{bp} = \frac{Q_a(V_Q)}{Q_d} \hat{V}_{in} \bigg|_{\omega=\omega_0}
\]

where

\[
Q_a(V_Q) \quad \text{actual } Q \text{ of filter (function of } V_Q)\]

\[
Q_d \quad \text{desired } Q \text{ of filter.}
\]

Notice in the above equation that the \(Q\) will be tuned, i.e., \(Q_a(V_Q) = Q_d\), when \(\hat{V}_{bp}\) is equal to \(\hat{V}_{in}\). Therefore, the LMS algorithm will work by trying to match the filter output \((\hat{V}_{bp})\) to the desired signal \((\hat{V}_{in})\) and making the overall gain equal to one.

As Fig. 4 shows, the tuning gradient \(g(t)\) is simply the bandpass output. This is done because the bandpass output is an easily produced approximation to the unavailable ideal gradient signal \(\partial \hat{V}_{bp}/\partial V_Q\). Using the bandpass output as the gradient also provides resistance to errors in frequency tuning, a very useful trait when dealing with high-\(Q\) circuits. This and the other advantages of the scheme are shown in the next subsection. One thing to note in Fig. 4 is the presence of a “dummy” summer in the path of the bandpass output to the multiplier. This is to equalize any delay added by the real summer in generating the error signal. The delay amount through these two paths should remain as matched as possible to prevent tuning errors.

C. Advantages of the Proposed \(Q\)-Tuning Scheme

The most important advantage of the new adaptive magnitude matching tuning scheme is that the inaccurate peak detectors have been removed. Errors due to offset voltages, improper magnitude detection, and poor high-frequency performance of the peak detectors are, thus, greatly reduced. By using the bandpass output as the tuning gradient, much of the method’s dependence on frequency tuning errors is also removed. A frequency tuning error corresponds to inputting a reference signal which is not exactly at a frequency of \(\omega_0\). Because of this, the bandpass output will have a phase shift.
\( \phi(\omega) \), and its magnitude will be

\[ H_{bp}(s) = \frac{Q_a}{Q_d} V_{in} \cos[\phi(\omega)] \]  

(7)

which is simply \( \hat{V}_{bp} = \frac{Q_a}{Q_d} V_{in} \cos[\phi(\omega)] \) when \( Q_a \) is tuned correctly. Equations (8)–(10) show that if the reference frequency is not at \( \omega_0 \) (leading to a phase shift of \( \phi \) at the bandpass output), the proposed \( Q \)-tuning scheme tunes until the bandpass magnitude is \( \hat{V}_{in} \cos \phi \). This means that the \( Q \) is still tuned correctly, even though there is a frequency tuning error

\[ \hat{V}_{bp} = V_{in} \]  

(8)

where

\[ V_{in}(t) = \hat{V}_{in} \sin(\omega t + \phi) \]

after several trigonometric substitutions and the cancellation of all but the dc components (due to the integration of \( \hat{V}_Q \)), we are left with the following. Note that when tuning is complete, \( \hat{V}_Q = 0 \) and \( V_Q \) is a constant

\[ \hat{V}_Q(t) = \mu \left[ \frac{V_{in} V_{in} \cos \phi}{2} - \frac{V_{in}^2}{2} \right] = 0 \]

(9)

\[ V_{in} = \hat{V}_{in} \cos \phi. \]

(10)

Ideally, the \( Q \) is tuned correctly even in the presence of frequency tuning errors.

Another large advantage is the ability to use highly distorted input reference signals such as clock pulses. For implementation purposes, all that would be needed is a limiter to bring the clock signal amplitude down into the dynamic range of the tuning circuitry. It can also be shown mathematically that a square wave reference will be sufficient for \( Q \)-tuning.

Since a clock signal can be approximated by a square wave, this is what as used in the mathematical analysis. A square wave can be represented as a sum of sinusoids as in (11) [16]

\[ V_{square}(t) = \frac{4A}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin(n\omega_0 t). \]

(11)

If the square wave is input into a second-order bandpass filter, its output will be, from (7)

\[ V_{bp}(t) = \frac{4A}{\pi} \sum_{n=1,3,5}^{\infty} \frac{Q_a}{Q_d} \cos[\phi(n\omega_0)] \frac{1}{n} \sin[n\omega_0 t + \phi(n\omega_0)]. \]

(12)

If the square wave and the resulting bandpass output are put into the main \( Q \)-tuning (4) and all but the dc components are removed, the resulting expression is

\[ \hat{V}_Q(t) = \mu \left[ \frac{16A^2}{\pi^2} \sum_{n=1,3,5}^{\infty} \cos[\phi(n\omega_0)] \frac{Q_a}{Q_d} \cos[\phi(n\omega_0)] \right]. \]

(13)

When tuning is complete, \( \hat{V}_Q \) will be zero and

\[ \sum_{n=1,3,5}^{\infty} \cos[\phi(n\omega_0)] \frac{Q_a}{Q_d} \cos[\phi(n\omega_0)] \]

(14)

or \( Q_a/Q_d = 1 \). Therefore, the \( Q \)-factor is tuned \( (Q_a = Q_d) \) even when using a square wave as an input. The theory is proven by a discrete component test in Section V.

IV. INTEGRATED TEST CHIP IMPLEMENTATION

For the purpose of testing the proposed \( Q \)-tuning scheme, an operational transconductance amplifier (OTA)-C bandpass filter has been fabricated in a 1.2-\( \mu \)m n-well CMOS technology. The filter is a fourth-order structure consisting of two cascaded bandpass biquads with a \( Q \) value of 20, and the power supply is \( \pm 1.5 \) V. The center frequency is 10.7 MHz, and center frequency tuning is provided using the well-known PLL with a voltage controlled oscillator method [17]. Quality factor tuning is done using the proposed adaptive \( Q \)-tuning scheme. Both tuning schemes use the master-slave technique as shown in the block diagram of the overall circuit given in Fig. 5. All blocks labeled LPF in the diagram are simple RC passive low-pass filters used to remove noise from the control signals.

A. Biquad Implementation

The chosen biquad for the integrated test filter is an OTA-C two-integrator loop [18]. This type of biquad provides much better high-frequency performance than other implementations such as switched-capacitor or MOSFET-C. One problem that can occur at very high frequencies is a lowering of the maximum attainable quality factor due to the finite output resistances of the OTA’s. This is because OTA’s at very high frequencies must be designed with the smallest amount of parasitic poles and zeros possible, thus, eliminating output resistance enhancing techniques such as cascading and even multistage designs. The finite output resistance effectively makes the integrators in the two-integrator loop lossy, so \( Q \) enhancement may be needed in some applications. A possible solution is to introduce some partial positive feedback in parallel with the normal \( Q \) loop of the two-integrator loop. By doing so, the \( Q \) can be made as high as desired, even up to infinity where the two-integrator loop becomes an oscillator. Adding this partial positive feedback must be done very carefully however, as increasing the positive feedback too much could lead to instability.

The addition of the positive feedback effectively makes the output resistance of the OTA’s very high by acting as a negative resistor. A similar approach is reported in [19], where the positive feedback was used to compensate the OTA itself before being used as an integrator in a ladder filter implementation.

Fig. 6 shows the fully differential biquad used in the integrated test chip. Notice that each OTA is controlled by a biasing voltage, where \( V_{\omega} \) controls the center frequency and \( V_{Q+k} \) controls the quality factor. Assuming each OTA has a finite output conductance \( g_{ds} \), the transfer function of the
Fig. 5. Block diagram of overall filter.

The most important issue when designing an OTA for use in high-frequency circuits is simplicity [21]. With this in mind, the OTA chosen for use in the test filter is the simple one-stage linearized OTA with common-mode control shown in Fig. 7 [17]. Transistors M5a and M5b provide the common-mode control and are working in the linear region [21]. To implement the design, three OTA’s were designed with $g_{m}$’s of 620, 100, and 20 $\mu$A/V in a 1.2-μm n-well CMOS process. The OTA’s were designed to have as large of a $g_{m}$ tuning range as needed to handle the worst case process and temperature shifts. A larger tuning range effectively increases the loop gain of both the $f_{o}$ and $Q$-tuning loops, so stability can become an issue if careful design practices are not used.

It should be noted that the OTA’s designed for this test chip could actually be used to form higher-frequency filters, but the frequency was limited for two reasons: first, matching is better at lower frequencies due to larger design capacitors, and second, the 3-dB points of the tuning circuitry such as the summer and multiplier (both of which are based on the OTA’s) should be higher than that of the filter.

The multiplier used in the tuning circuits is based on the general cross-coupled differential pairs [22], [23], with the $g_{m}$ modulation by a source degeneration MOSFET resistor [24], [25]. The entire multiplier structure, including the same common-mode control scheme employed by the OTA’s, is shown in Fig. 8. Since the multiplier is only providing phase information, its linearity is not a critical issue. However, offset can be a minor problem since the dc information in the output of the multiplier is the driving force for the tuning signal. The problem is not very critical because both inputs of the multiplier are sinusoids. Because of this, the input referred offset (of both inputs) is modulated by the other input and, therefore, has no dc value. The only dc error is the two offsets multiplied together, a small error relative to the original offset values.

The sinusoidal oscillator for the PLL-VCO frequency tuning scheme is a bandpass based oscillator with exactly the same structure as the slave bandpass biquad. The only difference is that the OTA which forms the positive feedback $Q$ loop in
the biquad is not linearized. This increases its $g_m$, making it unstable at low oscillation amplitudes, but due to the nonlinearity it quickly becomes stable at higher amplitudes, thus, making it a very effective nonlinear amplitude control device [26].

The integrator which is used in the LMS $Q$-tuning circuit is simply the 20-$\mu$A/V OTA with a large integrating capacitor attached. The input offset of the LMS integrator is important to the accuracy of the tuning scheme, so careful attention should be paid during design and layout to minimize offset. The effect of the integrator offset on the $Q$-tuning accuracy is more sensitive to smaller input signals, so it is desirable for the multiplier to have enough gain to maximize the input amplitude into the integrator.

The single most important circuit in the proposed $Q$-tuning scheme is the voltage divider. Inaccuracies in this device will
translate to a one-to-one error ratio in the Q-tuning. Therefore, the design of the divider must be done very carefully. Very accurate attenuators are reported in [14] and [15], but for this design it was decided to use the simple capacitive voltage divider shown in Fig. 9. The MOSFET resistor has a large resistance value and is used to discharge what would be a floating node without the resistor’s presence. The attenuation for the divider (neglecting the MOS resistor) is

\[ \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}} = \frac{C_p}{C_1 + C_2 + C_p} \]  

(18)

where \( C_p \) is the parasitic capacitance. Special attention must be paid to the design of this attenuator, and the parasitic capacitance must be taken into consideration. For this design, the capacitors in the voltage divider were made very large (about 10 pF) and an estimate of the parasitic cap was used. A more efficient method should be used for practical implementations.

V. EXPERIMENTAL RESULTS

This section presents the measured results of both a discrete component test version of the Q-tuning scheme and the integrated test chip.

A. Discrete Component Testing

Preliminary tests using discrete components showed that the theory behind the proposed Q-tuning scheme is sound and matches well with simulation results. An active-RC biquad bandpass filter biquad with a desired Q of ten was constructed for testing and the proposed Q-tuning circuit was applied. After tuning was complete, the value of \( V_Q \) was measured, the tuning circuit was disconnected, and a dc voltage source of the value of \( V_Q \) was applied (a master-slave scheme will not work with discrete components due to the poor matching between the discrete OTA’s and passive components). The frequency response of the filter was then obtained.

The Q-value without tuning (using the designed resistor values) was 6.19. After the Q-tuning circuit was applied, the Q was tuned to 10.04, only a 0.4% error in Q-tuning.

The accuracy of using different types of input reference signals was also tested. A sine wave with a frequency error of 3% was input to simulate an \( f_o \) tuning error. The Q after tuning was measured to be 10.11, or a 1.1% error. Tests were also performed with a triangular wave (Q value tuned to 10.11, a 1.1% error), and a square wave (Q value tuned to 9.90, a 1.0% error) to show that the method works for distorted input reference signals. Fig. 10 shows the frequency responses of the tuned bandpass filters for each of the separate test cases. The curves for the triangular reference signal and the sine wave with 3% frequency error reference signal are directly on top of each other. A gain of one in the figure is equivalent to a Q of ten.

B. Integrated Test Chip

Some overall chip performance characteristics such as the SNR of the fabricated chip were not as good as possible because of a common-mode offset in the designed OTA, but as this section will show, the tuning aspects of the filter still worked very well, tuning both center frequency and quality factor to less than 1% error.

1) Center Frequency and Quality Factor Tuning: The tuning for the 10.7-MHz filter was very good. The center frequency of the filter was measured to be 10.64 MHz, or a 0.56% error, and the Q was tuned to 19.85, or a 0.75% error. The Q of the biquads was calculated by measuring the bandwidth of the fourth-order filter at –6 dB. Fig. 11 shows the tuned response of the bandpass filter. The accuracy of the tuning was due in part to careful matching of the parasitics between the master and slave.

2) Common-Mode Response: The simple common-mode control scheme which was used on the OTA’s in the filter design had some problems. The common-mode rejection properties are adequate, but since the common-mode output voltage is set by a matched transistor in the bias circuit, the circuit is sensitive to mismatches between the bias circuit and the common-mode controller. The layout was not optimized to reduce this mismatch, and as a result there is a large common-mode offset present in the OTA’s which leads to distortion problems. The input signals had to be reduced, making the SNR lower. The measured common-mode rejection ratio was around 40 dB, which is what was expected, but the common-mode offset is around 300 mV. A better common-mode control scheme should be used to eliminate this problem.
3) Noise and Distortion: Because of the previously mentioned common-mode offset problem, the input signal amplitude had to be lowered to reduce the total harmonic distortion (THD) to 1%. As a result, the input voltage amplitude was cut down to 50 mV, and the measured SNR was only 47 dB. Fig. 12 shows the noise floor of the filter, where the signal reference level is at \(-38\) dB. Some noise is added by an on-chip buffer which is used to keep the capacitance of the pads from loading the filter, and some noise is also added by two off-chip buffers and a transformer.

4) Power and Area: The total power consumption of the entire chip, including two on-chip buffers, is 108 mW. Without the buffers, it would be somewhat lower, but this was not experimentally measured. The chip area, including the pad frame, is 2.2 mm \(\times\) 2.2 mm. The actual circuit area is 1.8 mm \(\times\) 1.8 mm, or 3.24 mm\(^2\). Fig. 13 shows a chip micrograph of the 10.7-MHz bandpass filter with automatic tuning, and Table I summarizes the measured results of the filter.

VI. CONCLUSIONS

An accurate method for the tuning of quality factors in high-\(Q\) and high-frequency filters has been proposed. The method utilizes the continuous-time LMS algorithm to improve on the already existing magnitude-locked-loop \(Q\)-tuning scheme. The theory has been proven by both discrete component tests and integrated circuit implementations. The discrete component tests showed that the accuracy of the \(Q\)-tuning even when using highly distorted reference signals such as square waves was within 1.1%. Experimental results of the IC test chip yield a measured \(Q\) accuracy of less than 1% error.

REFERENCES


Jan-Michael Stevenson (S’97–M’98) was born in Texarkana, TX, on October 18, 1972. He graduated *magna cum laude* from Texas A&M University, College Station, in December 1994. He received the M.S. degree in electrical engineering, also from Texas A&M, in December 1997. His major fields of study were high-frequency continuous-time filters and adaptive on-chip filter tuning.

He is currently a Design Engineer for Dallas Semiconductor Corporation, Dallas, TX.

Edgar Sánchez-Sinencio (S’72–M’74–SM’83–F’92) was born in Mexico City, Mexico, on October 27, 1944. He received the degree in communications and electrical engineering (professional degree) from the National Polytechnic Institute of Mexico, Mexico City, in 1966. He received the M.S. degree in electrical engineering from Stanford University, Stanford, CA, and the Ph.D. degree from the University of Illinois at Champagne-Urbana in 1970 and 1973, respectively. He worked in an industrial postdoctoral position with Nippon Electric Co., Kawasaki, Japan, in 1973–1974. Currently, he is with the Department of Electrical Engineering at Texas A&M University, College Station, as a Professor. He is the coauthor of *Switched-Capacitor Circuits* (New York: Van Nostrand–Reinhold, 1984) and coeditor of *Artificial Neural Networks: Paradigms, Applications, and Hardware Implementation* (Piscataway, NJ: IEEE Press, 1992). His present interests are in the area of solid-state processing circuits, including BiCMOS, CMOS RF communication circuits, data converters, and testing.

Dr. Sánchez-Sinencio has been the Guest Editor or Coeditor of three special issues on neural network hardware (IEEE *Transactions on Neural Networks*, March 1991, May 1992, May 1993) and one special issue on low-voltage low-power analog and mixed-signal circuits and systems (IEEE *Transactions on Circuits and Systems Part I: Fundamental Theory and Applications*, November 1995). He was the IEEE/ACAS Technical Committee Chairman on Analog Signal Processing (1994–1995). He has been Associate Editor for different IEEE magazines and transactions from 1992 until the present. He was the IEEE Video Editor for the IEEE *Transactions on Neural Networks*. He was IEEE Neural Network Council Fellow Committee Chairman in 1994 and 1995. He was a member of the IEEE Press Editorial Board. Currently, he is the Editor-in-Chief for the IEEE *Transactions on Circuits and Systems Part II: Analog and Digital Signal Processing*. He has been co-recipient of the 1997 Darlington Award for his work on high-frequency filters and also a co-recipient of the 1995 Guillemin–Cauer Award for his work on cellular networks. He was awarded with a Halliburton Professorship in 1993. In 1992, he was elected as a Fellow of the IEEE for contributions to monolithic analog filter design. In 1995, he received an Honoris Causa Doctorate from the National Institute for Astrophysics, Optics and Electronics, Puebla, Mexico.