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Optimizing and Comparing CMOS Implementations of the C-element in 65nm Technology: Self-Timed Ring Case

Oussama Elissati[1,2], Eslam Yahya[1,3], Sébastien Rieubon[2], Laurent Fesquet[1]
[1]TIMA Lab. – CIS Group, Grenoble, France
[2]ST-Ericsson, Grenoble, France
[3]Higher Institute of Technology, Banha, Egypt

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Oscillators and VCO

Oscillators are mandatory for :

- Generating the clock synchronization signal.
- Modulating and demodulating signals.
- Retrieving signals in noise.

- Communication applications :

  ➔Phase-Locked Loops (PLL) with strong requirements on stability, phase noise and power consumption.

Self-Timed Ring Oscillators

- Well-suited characteristics for managing process variability [Hamon 08]
- Considered as promising solution for generating clocks. [Fairbanks 04]
- Generating High-speed Multi-phase Clocks. [Elissati 10]
- Offering an appropriate structure to limit the phase noise.[Elissati 10]

Outlines

1 Self-Timed Rings

2 C-element Implementations

3 Design of the ring stages

4 Simulation results

5 Conclusion

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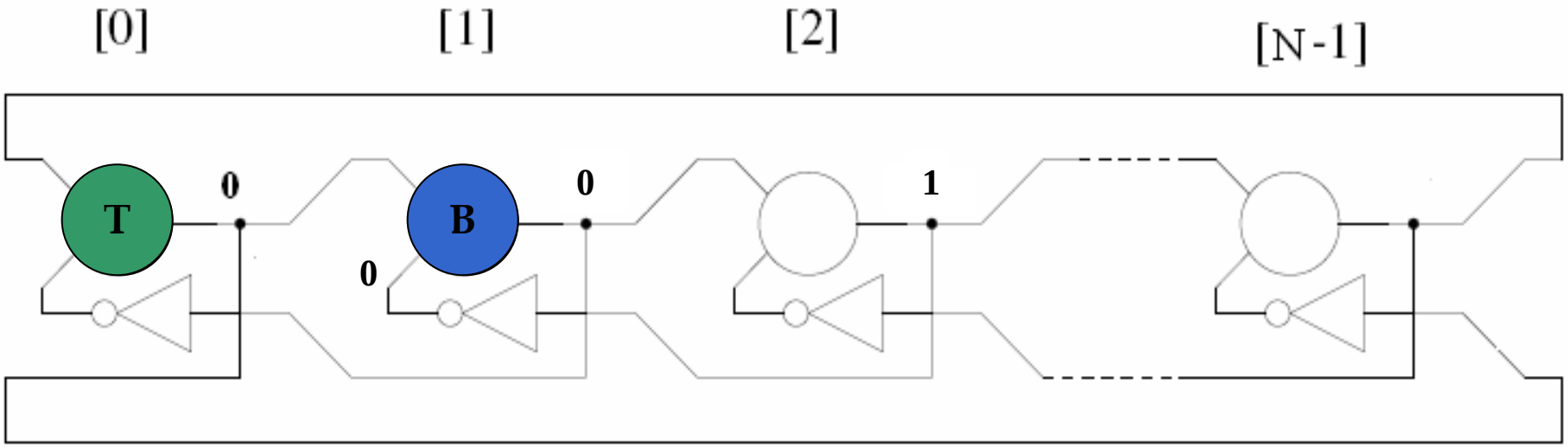
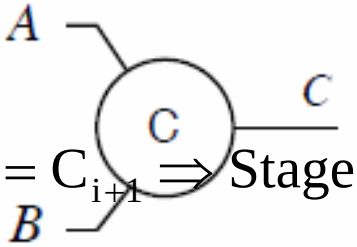
Self-Timed Ring





A	B	C
0	0	0
0	1	C^{-1}
1	0	C^{-1}
1	1	1

Propagation rules

$C_i = C_{i+1} \Rightarrow Stage_i = \{Bubble\}$

$C_i \neq C_{i+1} \Rightarrow Stage_i = \{Token\}$

$$Stage_{i-1} \underset{bubble}{\overset{token}{\rightleftarrows}} Stage_i \quad \Leftrightarrow \quad C_{(i-1)\%L} \neq C_i = C_{(i+1)\%L}$$

Self-Timed Ring

The frequency depends on the initialization

$$F_{OSC} = \frac{1}{2.D.(R+1)}$$

$$(D,R) = \begin{cases} (D_{rr}, N_T/N_B) & \text{if} \quad D_{ff}/D_{rr} \geq N_T/N_B \\ (D_{ff}, N_B/N_T) & \text{if} \quad D_{ff}/D_{rr} \leq N_T/N_B \end{cases}$$

The maximal frequency is reached when $D_{ff}/D_{rr} = N_T/N_B$

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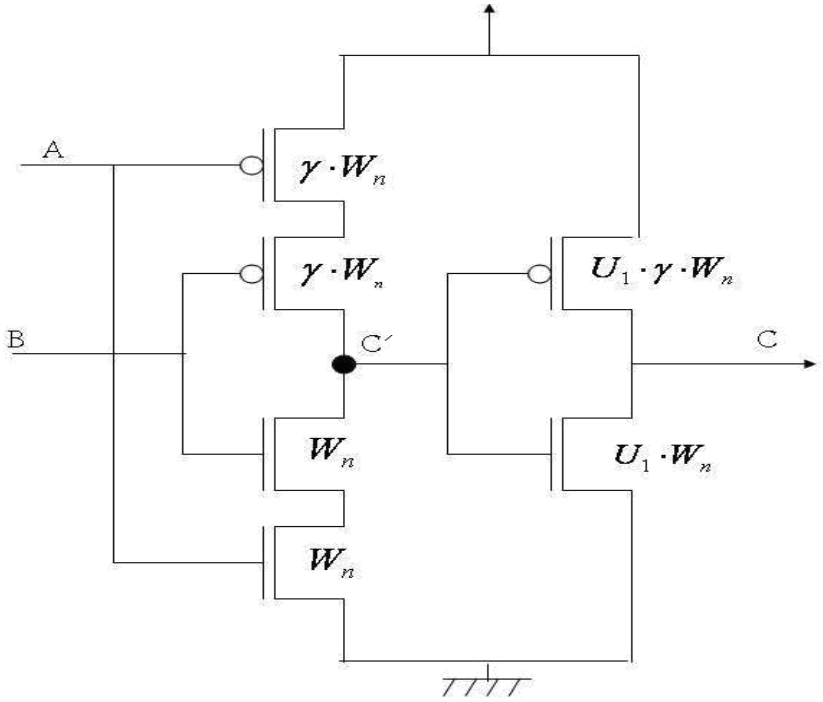
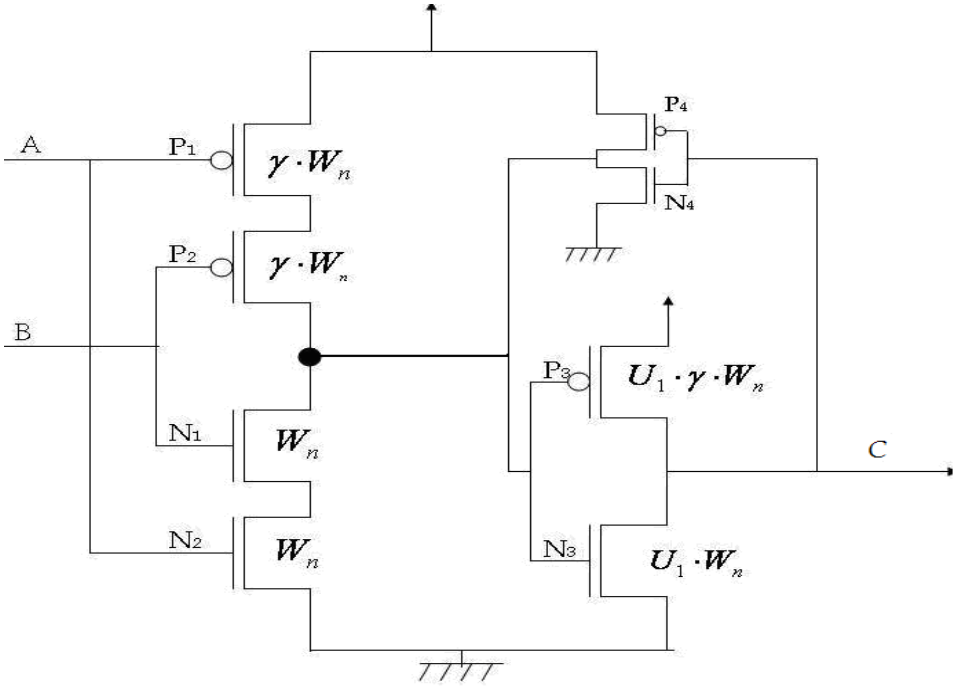
C-element implementations

Dynamic & Weak feed-back



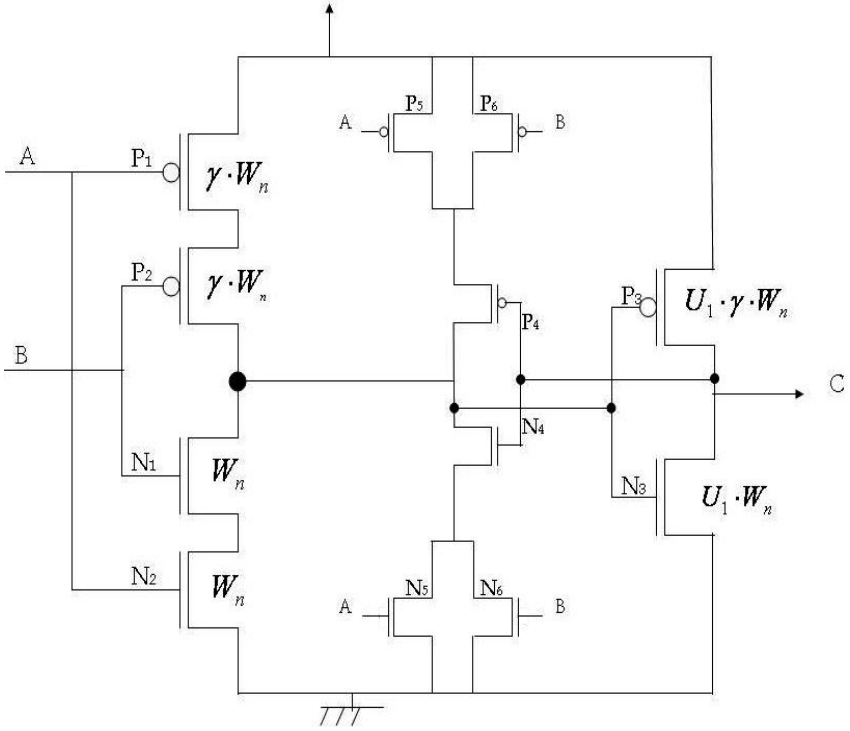
Dynamic



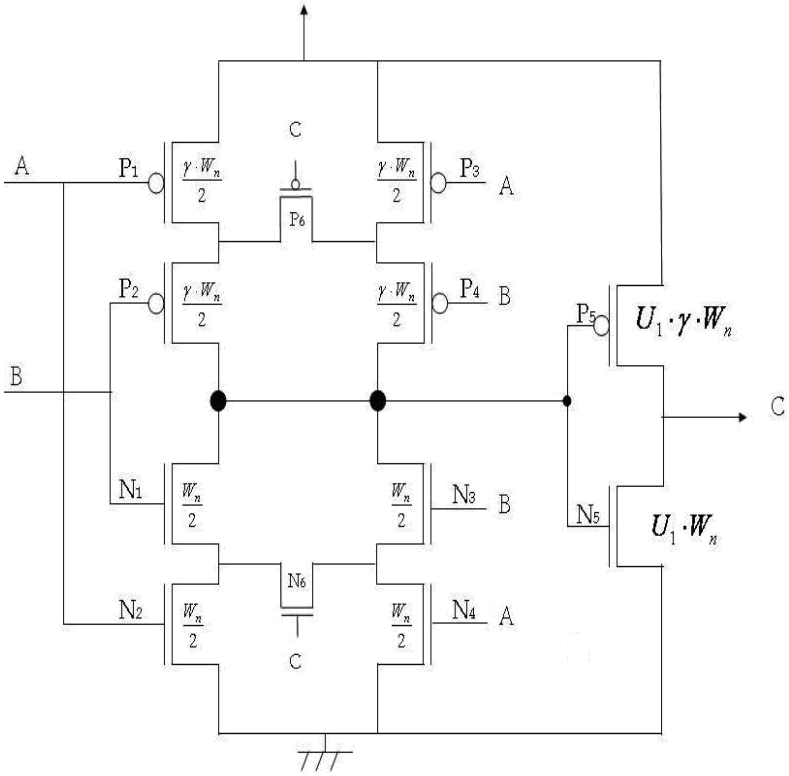
Weak feed-back **[Martin 89]**

C-element implementations

Conventional & Symmetric



Conventional **[Sutherland 89]**



Symmetric **[Berkel 94]**

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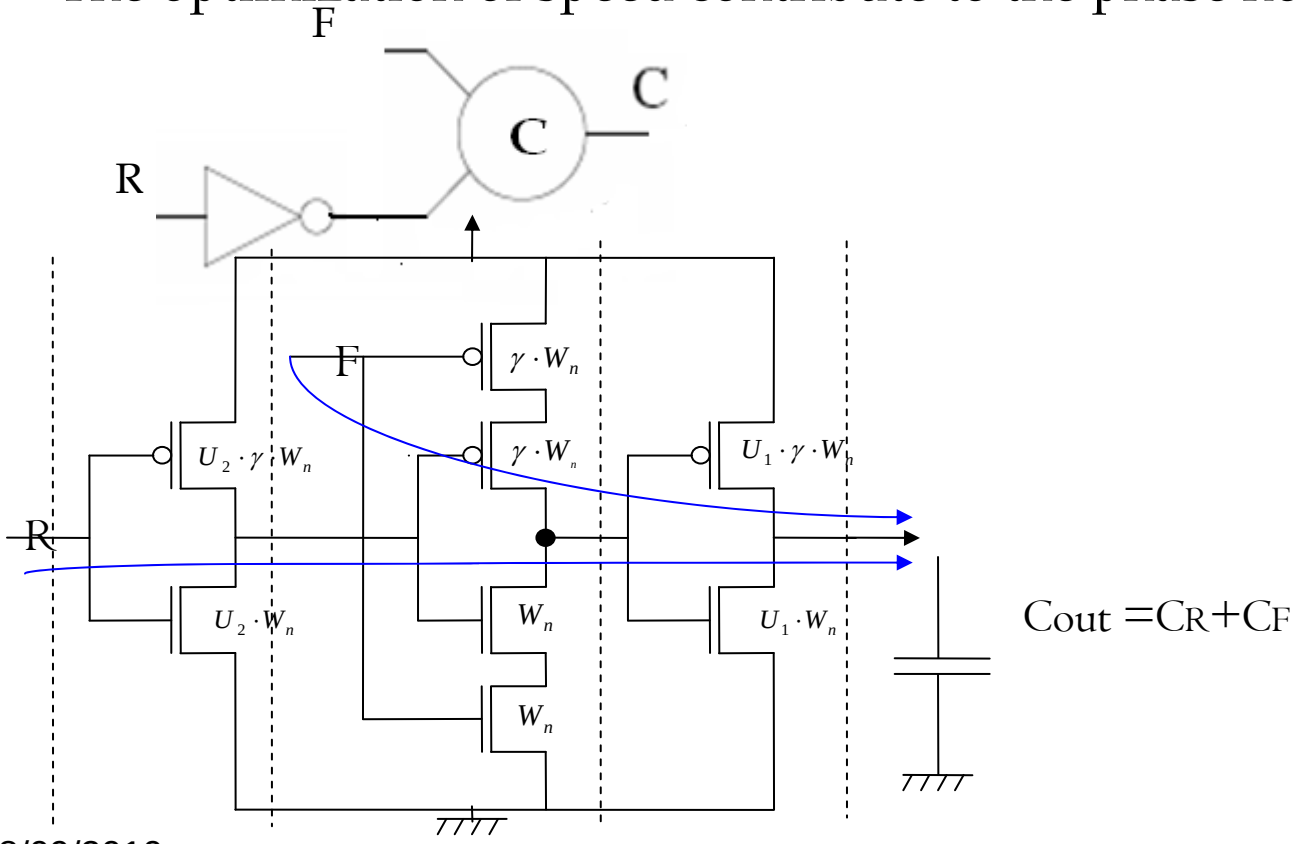
Design of the ring stages

Logical effort*

***From [Sutherland 99]**

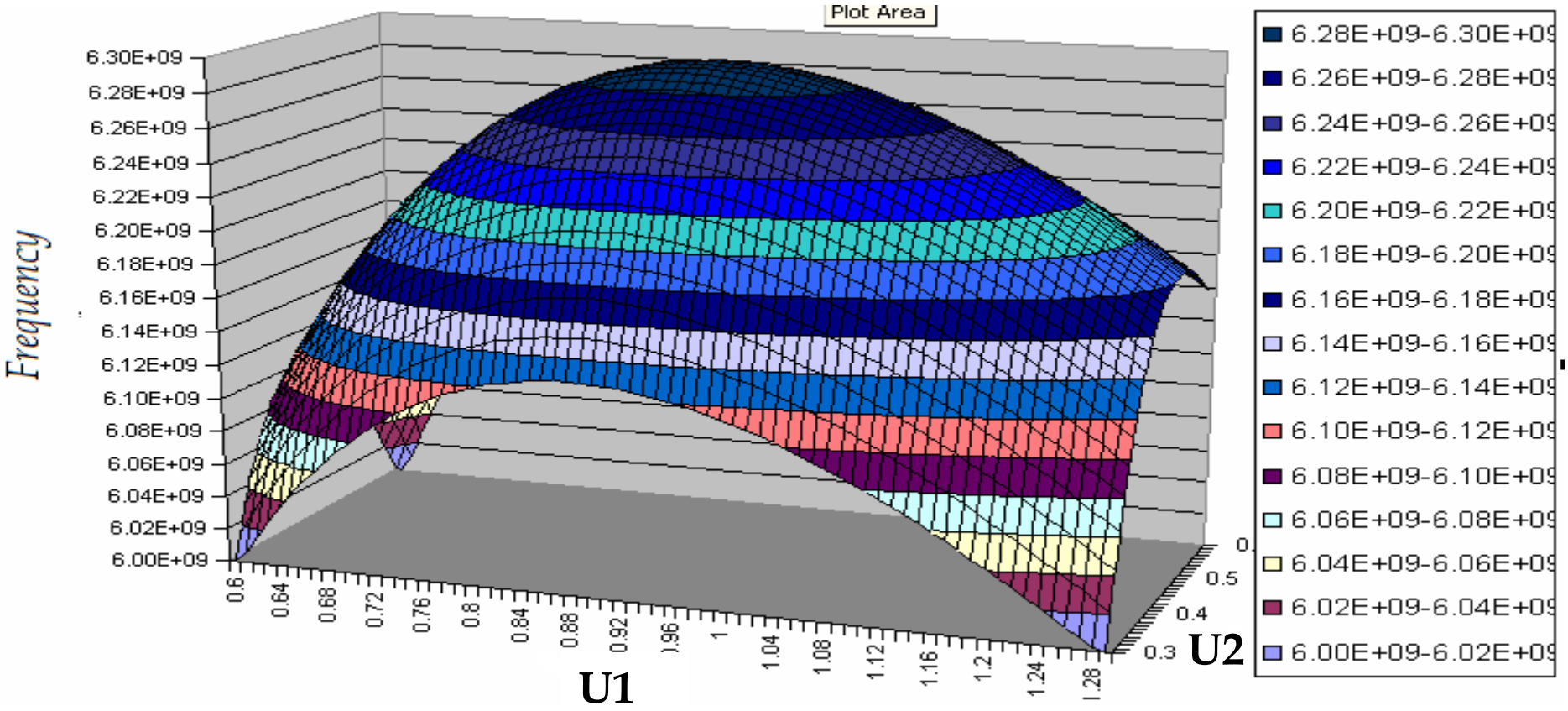
- Optimize the stage speed (Logical, Electrical and Branching efforts)
- The optimization of speed contribute to the phase noise reduction.



U1=0.89
U2=0.56

Design of the ring stages

Electrical simulations



2T/3B conventional implementation

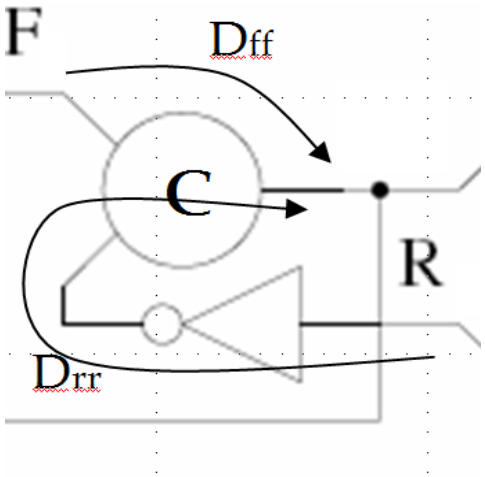
Same figure shape whatever the implementation, the initialisation and the power consumption

Design of the ring stages

Comparaison

Ring (conventional)	Optimal frequency	
	U_1	U_2
3 stages 1B/2T	1	0.9
4 stages 2B/2T	1	0.9
5 stages 1B/4T	1	0.9
5 stages 3B/2T	0.9	0.5

Logical effort
U1=0.89
U2=0.56



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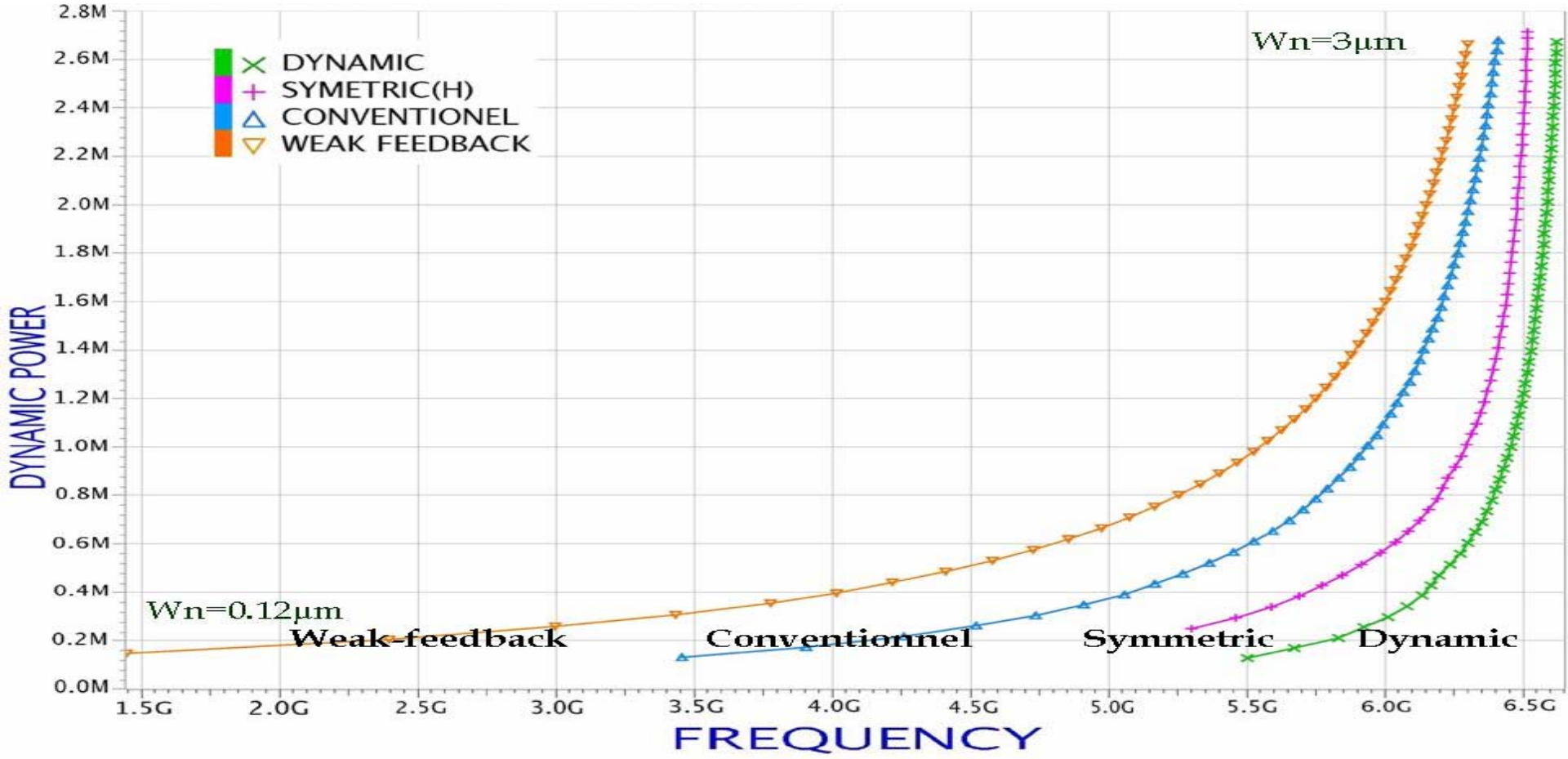
Simulation results

Frequency vs. Power

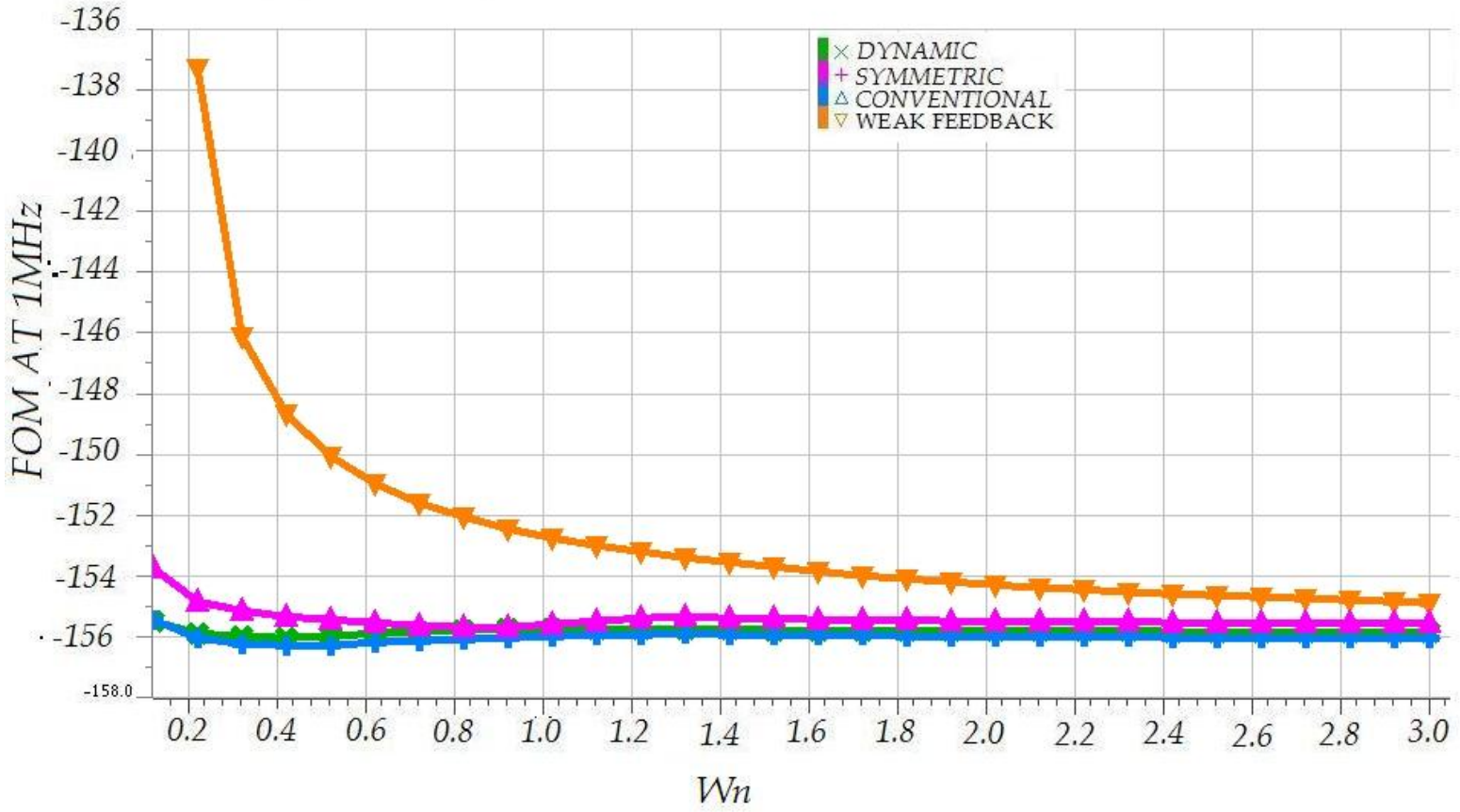


2T/3B U1 et U2 optimal

Simulation results

Figure of Merit (FOM)

$$FOM = L(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_s}{1mW}\right)$$



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Conclusions

- A C-element implementation comparison in terms of:

  speed, power and phase noise.

What to keep in mind:

- For high speed, low-power applications: use dymanic or symmetric
- For small area and low frequency: use conventional or weak feedback
- For low-phase noise applications: avoid the weak feedback, prefer the conventional

References

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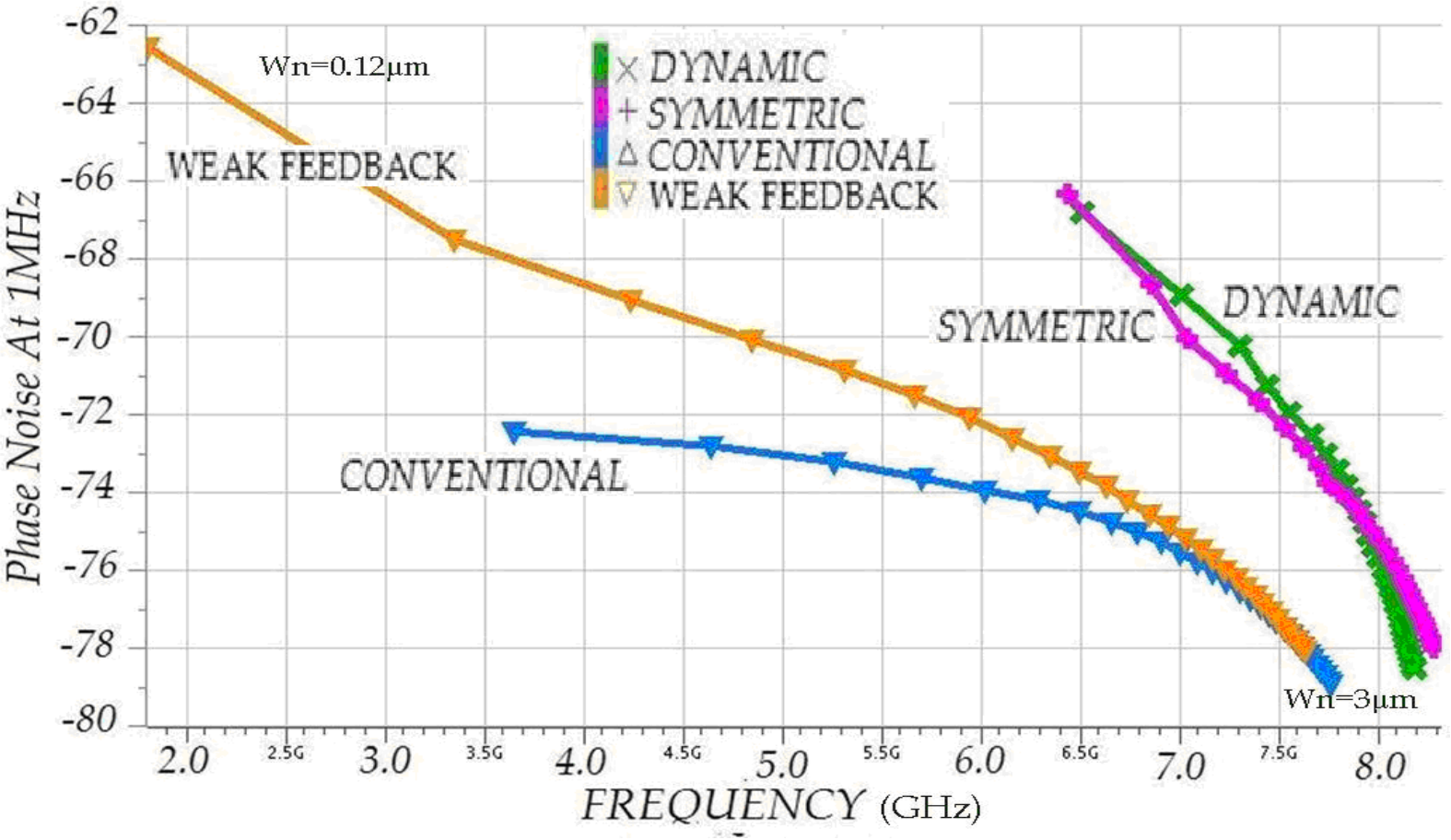
Performances comparison

Phase noise