Interference in Digital Circuits and Some Techniques for EMI Suppression

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Abstract—Noise generated by a logic gate in a simple digital circuit is considered in this paper. Appropriate circuit design and usage of electromagnetic interference (EMI) components are methods intended to suppress noise radiation by reducing/eliminating the noise flowing through conductive lines. Because of that, commercially available ferrite component is tested in a simple digital circuits realized on a PCB. Different configurations of digital circuit are analyzed: circuit printed on single-sided and double-sided board, with and without EMI suppressors placed on the conductive line at the input of circuit. With attention to the current distribution, the mounting position is observed for ferrite where it has significant noise effect. The measurements are obtained by digital oscilloscope TDS 2024B in the frequency range up to 200 MHz, and CTM030 Scan EM-EC magnetic probe with frequency response 2 MHz – 2 GHz which observe the waveform of the current. The measured data showed variations in noise suppressing effect depending on the design of circuit and by adding EMI suppressors.

I. INTRODUCTION

Integrated circuits (ICs) often play an important role in the electromagnetic compatibility (EMC) of an electronic system. ICs are generally the ultimate source and/or victim of an EMC problem. Noise coupled to the input or conductive lines of ICs may cause them to malfunction. As more attention is focused on the EMC design of integrated circuits, it is important to reduce the parasitic emission intra-chip [1].

For EMC purposes even a circuit, which is only intended to operate at low frequencies, must exhibit good immunity from RF interference. It is important to emphasize that although it may be the designer’s intent for the signals to return to their source through designated ground equipotential conductor paths, there is no guarantee that this will occur. In fact, some frequency components of that same signal may return through one path, while other frequency components of that same signal may return through another path. Different ground levels can lead to threshold shifts large enough for a logic error to occur [2]. The most important EMC function of a ground system is to minimize interference voltages at critical points compared to the desired signal [3].

The way that a circuit is laid out on a PCB is crucial to its EMC performance. Each track must be regarded as a component in its own right at high frequency. Proper PCB layout should be regarded as an integral aspect of circuit design, and should start with the ground plain [4].

The goal of this investigation is to show how the electronic circuits emit EMI noise, and how EMI noise is conducted through the circuits. Some noise reduction techniques are presented on the example of simple digital circuit [5], where a combination of appropriate ground design and usage of the EMI suppressors can significantly improve the EMC of the digital circuits. Noise reduction effectiveness of commercially available ferrite component 20805R82K7F [6], [7] in a simple digital circuit realized on PCB is shown.

II. SIMPLE DIGITAL CIRCUIT FOR ANALYSIS OF NOISE SOURCES

Different configurations of digital circuits are analyzed: with and without EMI suppressors placed on the conductive line at the input of the circuit, which is the potential “victim” of the interference (Fig. 1), printed on PCB with attention on ground plain design. Measured data on single-sided and double-sided boards with and without implemented EMI suppressors are presented.

In order to evaluate ground bounce and the factors that affect it, a simple digital circuit realized on PCB is used (Fig. 2). The analyzed digital circuit consists of a compatible crystal clock oscillator (frequency 8MHz), two quad two input NAND gates 74LS00, which are connected via two conductive lines (\(l = 10\) cm long, \(w = 1\) mm wide, and \(t = 33\) µm thick). The distance between the signal and the return conductor is \(d = 0.33\) cm.

![Figure 1. A simple digital circuit and added EMI suppressor with impedance \(Z(\omega)\).](image1)

![Figure 2. The double-sided PCB of tested digital circuit.](image2)
Although conductors are not normally considered components, they do have characteristics that are very important to the noise and transient performance of electronic circuits. At frequencies above 1 MHz, all conductors show their finite impedance, generally consisting of both resistance and inductance.

The self-inductance $L$ (in nH) of a straight conductor with rectangular cross section can be calculated as [8]:

$$ L = 2l \left( \ln \frac{2l}{w+t} + 0.25094 + \frac{w+t}{3l} + \frac{\mu T}{4} \right) $$

where $l$ is length, $w$ is width, $t$ is thickness of conductor in cm, $\mu$ is permeability, $T$ is frequency correction parameter.

The mutual inductance $M$ (in nH) of two parallel straight conductors with a length of $l$ (cm) and a distance of $d$ (cm) between them is represented as [9]:

$$ M = \frac{\mu}{2\pi} \left( \ln \left( \frac{l}{d} \right) + \left( 1 + \frac{l}{d} \right)^2 - \left( 1 + \frac{d}{l} \right)^2 \right) $$

Two conductors carrying current in opposite directions (such as the signal and ground leads) have a total inductance $L_{TOT}$ equal to:

$$ L_{TOT} = L_1 + L_2 - 2M $$

where $L_1$ and $L_2$ are the self-inductances of the two individual conductors and $M$ is the mutual inductance between them. In order to minimize the total inductance of the complete current path, the mutual inductance between the conductors must be maximized. Therefore, the two conductors should be placed closer together (to minimize the area between them). The inductances are calculated using equations (1)-(3) are $L=111.04$ nH, $M=62.74$ nH, and $L_{TOT}=96.59$ nH. The impedance $Z(\omega)$ of the ferrite EMI suppressor can be determined as a sum of real $Z_r(\omega)$ and imaginary part $Z_i(\omega)$:

$$ Z(\omega) = Z_r(\omega) + jZ_i(\omega) = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC} $$.  

III. MEASUREMENT RESULTS

A. Digital signal and harmonic components as noise sources

A digital signal on the signal line has the highest frequency in a circuit. Such signal contains several hundred MHz harmonic components and generates noise. The signal comprises of several tenth or higher-order harmonics and the frequency of those harmonics reaches several hundred MHz. Those harmonics included in the digital signal are considered the principal cause of EMI noise emission from the electronic circuit.

The inductor type EMI suppression filter is connected to a signal line in series to suppress unnecessary harmonic current. Figures 3 shows the harmonics included in signal line with and without additional ferrite EMI suppressor. The spectrum has been reduced using ferrite component, as it can be seen in Fig. 3b.

B. Approaches to Suppressing ground bounce

Using a digital oscilloscope voltage $v_{DiffG}$ has been measured between two ends of the ground line. The voltage between the opposite points of the ground line is:

$$ v_{DiffG} = L \cdot \frac{di_G}{dt} $$

where $i_G$ is the ground line current. As a result, the driving and the driven circuit experience different ground levels, which can lead to threshold shifts large enough for a logic error to occur.

In order to make the ground bounce more moderately, either $L$ or $\frac{di_G}{dt}$ should be made smaller. Since $L$ depends on the conductive lines geometry (their length, width etc.), and in given circumstances they usually can not be changed, the second option is to make the current's rate of change, $\frac{di_G}{dt}$ as small as possible. To achieve that goal, a ferrite suppressor can be added to the signal line. It is easy to notice that the ground bounce peak-to-peak amplitude is considerably smaller with the ferrite suppressor (Fig. 4). When the ground is provided on the front surface of the PCB, the ground bounce is non-negligible so ground line is designed on the back side of the board. In that way, the unwanted voltage between the ground terminals is significantly reduced. Inserting the EMI suppressor between the IC1 output and the signal line on the double-sided board, that noise can be almost eliminated (Fig. 5).
C. Analyzing the mounting position of EMI suppressor

The current/voltage in a transmission line varies depending on the length of conductor and measuring position on the line. To analyze suppressing effects of ferrite depending on the signal line length, current distribution is observed in the longer signal line ($l=15$ cm) by a magnetic field probe and oscilloscope.

The impedance can be calculated by dividing the current value by the voltage value. Since the ferrite component has frequency-dependent impedance, it provides a significant noise suppressing effect when the impedance at the ferrite mounting position is small.

On the other hand, when the impedance at the mounting position is large, it can hardly provide a sufficient noise suppressing effect. The EMI suppressor is located near a noise source, at the output of first gate (i.e. at the distance $x=0$), as it can be seen in Fig. 6a. Second ferrite EMI component is placed at the distance $x=9$ cm, in order to further improve suppressing effect (Fig. 6b).

Since the current distribution has its maximum at the distance $x=9$ cm from the IC1 output (Fig. 7), suppressor is added at that position. When a single ferrite cannot provide a sufficient noise suppressing effect, another component can be added on the place where the current distribution has maximal value.

D. Effectiveness of suppressors on noise problems in circuit

Magnetic field radiation from a loop, which is carrying a high $di/dt$, can be minimized by reducing the loop area or by reducing $di/dt$. The output circuit is often at a lower voltage than the input, and therefore carries higher $di/dt$. It is therefore important
to pay attention to the output circuit loop area. At the distance of 1 mm from the signal conductor, a rectangular contour 150 mm long and 33 mm wide is added, in order to serve as noise antenna. Since the additional contour is open, no current flows through it and therefore its self-inductance does not influence the voltage that can be measured between its terminals. Hence, the induced voltage is completely determined by the mutual inductance of the tested circuit and the additional contour $M_{12}$, and the signal current change rate:

$$v_{A12} = M_{12} \cdot \frac{dt}{dt}. \quad (6)$$

Since the mutual inductance between the signal and additional contour $M_{12}$ is the same for both configurations (with and without EMI suppressor), the induced voltage is proportional to the $di/dt$.

The magnetic field and current distribution between conductors of rectangular cross section is considered. This involves the case in which there is no current in one of the conductors. As it is shown in Fig. 8 and Fig. 9 currents rate of change can be reduced by adding EMI suppressors. It is also important that the ferrite components should not couple magnetically with the leakage flux.

IV. CONCLUSION

The tested circuit has a working frequency of 8 MHz (the base frequency of the signal). Because of that, the frequency range of interest is in the range of 8 MHz and above.

From the ferrite component characterization, presented in the previous work [10], it can be seen that the resonant frequency of the ferrite EMI suppressor is above 100 MHz, where ferrite component has a sharp rise of impedance, and provides less damage to the signal waveform in the analyzed digital circuit. As it can be concluded from the positive imaginary part of the impedance, in the frequency range of interest the component acts as an inductor and it is therefore well suited for this application.

The inductor type EMI suppression filter is easy to mount on PCB, it does not need to be connected to a ground line and provides a stable noise suppressing effect. In addition, the inductance of the EMI suppressor, determined by characterization, is 820 nH [10]. This inductance value is eight times greater than the inductance of the signal and ground line, which is 96.59 nH.

With the addition of the ferrite suppressor, the inductance of the whole contour rises around 1 µH, which is significantly higher than the original inductance. In these conditions, the change rate of the current can be significantly influenced and the ground bounce becomes smaller.

Proper PCB layout should be regarded as an integral aspect of circuit design, and should start with the ground plain. By implementing the EMI suppressor, the amplitude between the two ends of the ground conductor is reduced about 70 %.
By printing tested circuit with separated continuous ground path on the back plain of the board, ground bounce peak-to-peak amplitude is minimized. The ground bounce magnitude on that type of circuit is almost totally eliminated by installing ferrite component.

The combination of appropriate ground design and usage of EMI suppressors can significantly improve the EMC of digital circuits, as it is shown in this paper.

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REFERENCES


