A Method to Estimate Slew and Delay in Coupled Digital Circuits

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Abstract—Coupling capacitance has substantial impact on signal delays and arrival times. It is not always correct to de-couple them using the Miller Factors of 0 or 2X. Towards this end various de-coupling techniques have been studied in literature. We extend them and suggest their use in static timing analysis. Our approach uses the Switching Factor based de-coupling approximation idea to compute impact of coupling capacitors on signal slews and delays. We suggest an iterative table lookup scheme. The slew and delay tables for the library cell elements are looked up to compute slew and arrival times of signals in the presence of coupling capacitors. The method is easy to use with existing static timing analysis tools. It works with slew and delay tables, which are usually available with technology libraries. Other than table lookups it requires minimal computation of two switching factors per coupling capacitor per iteration. Analysis and HSPICE simulation results are given to support the suggested method.

I. INTRODUCTION

With the advent of recent fabrication technologies, device and interconnect feature sizes have reduced tremendously. Geometries in XY plane have scaled down, but the vertical dimension has not reduced as much due to resistance concerns. This has rendered coupling capacitance significantly more relevant [1]. Most of the EDA tools were designed in the era when coupling capacitances could either be ignored or modeled as a grounded capacitance of appropriate equivalent value. Incorporating coupling capacitance without any approximations will require large run times as we will need to solve the exact differential equations governing the behavior of coupled circuits. It is desirable to have a solution around the existing EDA tools. To address this, various de-coupling approximations have been suggested in recent literature. The idea is to replace the coupling capacitance by two grounded capacitances at the coupled nodes. The values of these grounded capacitances need to be determined. Earlier methods for this used simplistic Miller Factor of 0 or 2X (depending upon the directions of the signals switching across the coupled nodes) for the de-coupling approximations. Recent methods tend to look into the waveforms across the coupled nodes to compute de-coupling approximations. However, these waveforms cannot be computed until we either solve the coupled circuit or have a ‘good enough’ de-coupling approximation. We discuss a technique, which iteratively predicts these waveforms looking into the slew/delay tables of driver gates. Before discussing our technique we briefly review the methods reported in literature.

II. BACKGROUND

Reported methods talk about analytical as well as numerical techniques to handle coupling capacitors. The voltage glitch introduced onto the coupled line due to signal switching on the adjacent line is termed as crosstalk. Introduction of this crosstalk onto an adjacent line could speedup or slowdown the signal transition on it. The exact amount of speedup or slowdown and its impact on slew and delay depends on the relative signal transitions on aggressor and victim lines. The peak value of crosstalk voltage and its implication on signal delay is reported in many publications [2] [3] [4] [5]. Becer and Hajj give analytical formulae for the delay and crosstalk in [2]. The suggested closed form model takes interconnect capacitance, driver resistance and driver strengths into account. In [6] Devagan gives a detailed analysis of crosstalk injection on a victim net under the application of infinite ramp as an input to the aggressor net. The infinite ramp causes the crosstalk estimators to become very pessimistic. Kulhman, Sapatnekar and Parhi [5] give a better estimator, which matches with HSPICE simulations. In case of multiple aggressors it becomes important to consider the worst-case scenario which introduces maximum delay. Gross et. al. in [7] talk about the computation of aggressor arrival times, which result in worst case delay on victim net. It uses linear superposition of waveforms. Since the complete system is not linear this introduces errors in the delay estimation. Chen et. al. [8] compute the aggressor alignment for the worst case crosstalk noise. In [9] Dutta and Pileggi give bounds on worst case gate delay due to capacitance coupling.

Most of the crosstalk aware timing analysis methods implicitly perform de-coupling of the coupled capacitor. Khang, Muddu and Sarto suggest that the values of de-coupled capacitors be computed as per the switching activity across the coupled nodes [10]. The de-coupling capacitor is expressed as Switching Factor (SF) times the coupled capacitor. Two SFs are to be computed, one each for the coupled nodes. Both these SFs are proved to be bounded between -1 to 3. Its computation is shown to be dependent on the relative slews and arrival times. In [11] Chen, Kirkpatrick and Keutzer present a formal SF based de-coupling idea to de-couple capacitors during timing analysis. The reported method gives efficient method to compute the SF through Newton-Raphson iterations. We closely follow this method to suggest our technique.

The effect of coupling capacitor on crosstalk noise and hence on signal delay and slew is also well researched. There are several approaches reported in literature [12] [13] [14] [15] which use the switching window idea to handle coupling capacitors during static timing analysis. Switching window is defined as the time interval during which at least one of the signals across the coupled nodes is expected to switch. Most of these methods are iterative in nature. The method suggested by Franzini et. al. [14] is based on combination of static timing analysis and reduced order macro modeling. The method works in two steps. The first step computes worst case timing and the second step uses reduced order models for the coupled network to achieve less pessimistic delay and slew numbers. Ideas based on replacing the entire coupled distributed RC interconnect model by an effective capacitance are explored in [16] [17] and [18]. Tehranl et. al. reports in [19] a method, which considers the functional relationship across the signals present on coupled nets to further avoid the pessimism. Xiao et. al. also exploit functional correlation to achieve better convergence in [15]. The fact that crosstalk delay in dependent on signal arrival times is emphasized by Cao et. al. in [13]. The method describes the generation of delay change curves, which are then used to compute the dynamic delay (the delay introduced due to crosstalk), during the timing analysis. The delay change curves relate dynamic delay to relative arrival time of coupled signals. Zhou, Nichols and Shenoy give an abstract framework of performing timing analysis in presence of crosstalk in [20]. The timing
analysis iterations are modeled as fixed-point computations. The solutions of timing analysis are shown to form a lattice and the convergence properties of iterative methods are addressed.

In this paper, we consider the problem of computing slews and arrival times of the signals during the static timing analysis. We start with lumped capacitance (grounded and coupled) models for the coupled nets. We use SF based de-coupling idea to compute iterates of de-coupling capacitance values. These values are then used to compute the total load capacitance to the gates driving the coupled lines. Using the load capacitances we predict the waveforms across the coupled nodes. These waveforms are predicted using slew and delay lookup tables of driving gates. The waveforms are used to recompute better iterates of the de-coupling capacitances. Upon the termination of this iterative process we get the slew and delay numbers at the output of driving gates. The method is general enough and can be routinely extended to handle cases where more than two nets are coupled together.

In Section III we give the problem formulation for a simple two-coupled line case. We sketch the well known Switching Factor based de-coupling method in the same section. We also formulate our iterative scheme to effectively use the switching factor computations and slew/delay table lookups to compute the slew and delay numbers across the coupled lines. In Section IV we sketch the generalization of our method to handle couplings of more than two nets. Section V contains HSPICE simulation results to support the method. De-coupling approach has certain inherent issues when used during static timing analysis. These are discussed in Section VI. We conclude the paper in Section VII.

III. BASIC DE-COUPLING APPROXIMATION

The de-coupling problem, which we address in this paper, is depicted in Figure 1. Gate 1 and Gate 2 are driving two coupled lines with coupling capacitor $C_x$. We seek to compute slew and arrival times at nodes 3 and 4. These should be as close as possible to the slew and arrival times at nodes 3 and 4 respectively. For this we compute a set of two de-coupling capacitors as shown in Figure 1(b). If required we compute two sets of de-coupling capacitors, one matching the slews and other matching the arrival times.

![Fig. 1. Coupled circuit and its de-coupling approximation.](image)

The impact of coupling capacitance on slew and delay is highlighted in Figure 2. A falling digital signal is applied at node 1 and a rising signal is applied at node 2. The rising waveform at node 3 and falling waveform at node 4 crosstalk with each other. With increasing coupling capacitance, the waveform at node 4 in Figure 1(a) deteriorates in terms of its slew and delay. The waveforms shown in Figure 2 are HSPICE simulation traces for coupled circuits modeling coupled lines of length 10u, 25u, 50u, 75u, 100u, 125u, 150u, 175u, 200u, 300u and 500u length running parallel at minimum separation on the fifth layer of metal (M5) in a 0.18u technology. All coupled circuits have the same circuit wherein the arrival time of signal at node 1 is varied, keeping the coupling capacitance constant. The simulations are performed for 200u parallel lines in M5, with arrival time of signal at node 2 fixed at 10ns and arrival time of signal at node 1 varied as 9.8ns, 9.9ns, 10.02ns, 10.04ns, 10.06ns, 10.15ns and 10.25ns. Note that the position and the peak value of the crosstalk voltage vary with the relative arrival times. This in turn varies the point to point delay and the slew of the signal at node 4 with the arrival time of the signal at node 1.

![Fig. 2. Voltage waveforms at node 4 for the circuit in Figure 1 with the line length varied between 10u - 500u, with lines running at minimum separation in M5 in a 0.18u technology. All waveforms are plotted simultaneously with line lengths (10u, 25u, 50u, 75u, 100u, 125u, 150u, 175u, 200u, 300u and 500u) marked alongside them. Coupling capacitance is proportional to the line length. Slew/Delay at the node 4 can be seen as function of coupling capacitance.](image)

We now consider the notations given in Figure 4. The slews and arrival times at the input of gate 1 and gate 2 are denoted by $(S^1_1, T^1_1, S^2_2, T^2_2)$. We seek to compute the slews and arrival times...
(S1, T1, S2, T2) at the output of these gates. This is a standard procedure in conventional static timing analysis. It is solved using the slew/delay tables. Each gate has a slew table and a delay table. Library vendors provide these tables to capture the timing behavior of each gate in their library. The delay table provides the input pin to output pin delay as a function of the signal slew at the input pin and the effective load capacitance at the output pin. The slew table provides the signal slew at the output pin as a function of signal slew at the input pin and the effective load capacitance at the output pin. Under a non-coupled scenario, the load seen at the output of gates 1 and 2 can be taken as the self capacitance of the interconnect lines plus the input capacitance of the successive gates, i.e., the gates 3 and 4 respectively. Using these lumped loads, slew and delay tables of gate 1 and gate 2 are looked into to compute slew and delay at node 3 and node 4 respectively. The arrival time at node 3 (node 4) equals the arrival time at node 1 (node 2) plus the delay incurred by gate 1 (gate 2). However, in the presence of coupling capacitance Cx, we need to compute the lumped load capacitances carefully.

\[ S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \]

\[ S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \]

Fig. 4. Coupled Lines with input slew and arrival times and slew and arrival times to be computed.

\[ S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \]

\[ S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \]

Fig. 5. Model for the coupled lines.

\[ S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \quad S_1 T_1 \]

\[ S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \quad S_2 T_2 \]

Fig. 6. De-coupling model for the coupled lines in Figure 5.

Since the slew and delay tables are characterized for lumped load capacitance, we need to convert the coupled lines to something that resembles the lumped load. This is achieved by putting equivalent de-coupling capacitors whose values must be determined appropriately. We modify the model given in Figure 4 to handle this. Referring to Figure 5 and Figure 6, let C_{d1}, C_{d2} be the input capacitances of the gates driven by Gate 1 and Gate 2 respectively. Also, let C_{i1}, C_{i2} be the lumped grounded capacitances of the interconnect nets connected at the output of Gate 1 and Gate 2 respectively. Let C_{i1} = C_{d1} + C_{i1} and C_{i2} = C_{d2} + C_{i2}. We seek to compute C_{d1}, C_{d2} as de-coupling approximations for the coupling capacitor Cx. These de-coupling approximations can be computed by equating the charge supplied by gates in two models. For this we first compute the currents supplied by two driver gates in coupled and de-coupled models. The currents I_1(t) and I_2(t), in coupled and de-coupled circuit respectively, can be computed as,

\[ I_1(t) = (C_x + C_{i1}) \frac{dV_1}{dt} - C_x \frac{dV_2}{dt} \]  
(1)

\[ I_2(t) = (C_{i1} + C_{i2}) \frac{dV_1}{dt} \]  
(2)

Now looking at the coupled case. The total charge \( \Delta Q \) supplied by the Gate 1 during the time interval when the V_i(t) changes from its stable state, let say 0 volts, to a threshold voltage V_{th}, volts is given as,

\[ \Delta Q = (C_x + C_{i1})V_{th} - C_x \Delta V_2 \]

\[ = (C_x + C_{i1})\left(1 - \frac{\Delta V_2}{V_{th}}\right) + C_{i1} \]  
(3)

where, \( \Delta V_2 \) is the voltage change at the output of Gate 2, when the output of Gate 1 has changed from 0 to V_{th}. Now looking at the de-coupled case. The total charge \( \Delta Q' \) supplied by Gate 1 under the same assumptions is

\[ \Delta Q' = (C_{i1} + C_{i2})V_{th}. \]  
(4)

Equating the charges \( \Delta Q \) and \( \Delta Q' \) we get a de-coupling approximation. Taking \( \beta_1 = \frac{\Delta V_1}{V_{th}} \), we get \( C_{d1} = C_{i1}(1 - \beta_1) \). By a similar analysis for charge supplied by Gate 2 we get \( C_{d2} = C_{i2}(1 - \beta_2) \), with \( \beta_2 = \frac{\Delta V_2}{V_{th}} \), where \( \Delta V_1 \) is the voltage swing at \( V_1(t) \) during the time interval when \( V_2(t) \) swings from 0 to \( V_{th} \). Note that if \( V_2(t) \) is switching from \( V_{DD} \) to 0, then \( \beta_2 = \frac{\Delta V_1}{V_{DD} - V_{th}} \). In general it is the ratio of the voltage swings when one of the voltage swings from its current logic value (\( V_{DD} \) or ground) to a threshold value \( V_{th} \). The factors \( (1 - \beta_1) \) and \( (1 - \beta_2) \) are called Switching Factors (SFs). These factors are dependent on relative switching of the waveforms present at the coupled nodes. For idealized digital signals as waveforms, it depends on slew and relative arrival times of the signals across the coupled nodes. Next we formalize the computation of these SFs for two digital signals.

A. Computation of Switching Factor

We assume for the rest of the discussion that the waveforms at the output of a gate can be approximated by a piece-wise linear function. It is completely described by the slew and delay tables as a function of the input slew and output capacitance. The switching factors are dependent on the voltage swings \( \Delta V_1 \) and \( \Delta V_2 \) of the waveforms present at the output of the driver Gate 1 and Gate 2 respectively. In Figure 7 we draw two interacting voltage waveforms at these nodes. The voltage swing \( \Delta V_2 \) is the change in \( V_2(t) \) waveform during the time window when \( V_1(t) \) has changed from 0 to \( V_{th} \). Similarly \( \Delta V_1 \) is the change in \( V_1(t) \) waveform during the time window when \( V_2(t) \) has changed from \( V_{DD} \) to \( V_{th} \). Formally, \( \Delta V_1 \) and \( \Delta V_2 \) can be computed as per the following non-linear formulae comprising of the slew and time variables.

\[ \Delta V_1 = S_1 \Delta T_1 = S_1 \left\{ \text{Max} \left(0, \left(\text{Max}(T_1^a, T_2^b) - \text{Min}(T_2^{th}, T_1^f)\right)\right) \right\} 
(5) \]

\[ \Delta V_2 = S_1 \Delta T_2 = S_1 \left\{ \text{Max} \left(0, \left(\text{Max}(T_1^a, T_2^b) - \text{Min}(T_1^{th}, T_2^f)\right)\right) \right\} 
(6) \]

\( S_1 \) and \( S_2 \) are the signed slews (positive for rising signals, negative for falling signals) for \( V_1(t) \) and \( V_2(t) \) respectively. The time variables in the above equations are shown in Figure 7.

B. Static Timing Analysis

We now formulate the problem of computing slews and arrival times at the coupled nodes as a problem of computing a fixed point of an iterative scheme. Note that, in order to compute \( \Delta V_1 \) and \( \Delta V_2 \) we need to know the slews and arrival times of the waveforms \( V_1(t) \) and \( V_2(t) \) respectively. The waveforms \( V_1(t) \) and \( V_2(t) \) can be computed only if we know the total load capacitance (including the de-coupled capacitances) as seen by Gate 1 and Gate 2 respectively. This induces
an iterative scheme as follows. Rewriting Equation 5 and Equation 6 for \( \Delta V_1 \) and \( \Delta V_2 \) as,

\[
\Delta V_1 = f_1(S_1, T_1, S_2, T_2, V_{ih}) 
\]

and

\[
\Delta V_2 = f_2(S_1, T_1, S_2, T_2, V_{ih}) 
\]

Note that, \( V_{ih} \) is also included into the formulation of functions \( f_1(.) \) and \( f_2(.) \). \( V_{ih} \) should be taken as the voltage point at which point to point delay is measured. Its typical value is \( V_{DD}/2 \).

To compute \( \Delta V_1 \) and \( \Delta V_2 \) we need to compute \( S_1, T_1, S_2, \) and \( T_2 \). These are computed through appropriate lookups in Slew and Delay tables for Gate 1 and Gate 2. Let \( \text{ST}_1(S_{in}, C_{load}) \) be the Slew Table for Gate 1, which gives the slew at the output of the gate for specified input slew and load capacitance. Let \( \text{DT}_1(S_{in}, C_{load}) \) be the Delay Table for Gate 1, which gives the gate delay for specified input slew and load capacitance. The slew and delay tables \( \text{ST}_2 \) and \( \text{DT}_2 \) are similarly defined for Gate 2.

C. Slew/Delay Matching as Fixed Point Computations

We write slews and arrival times \( S_1, T_1, S_2, T_2 \) as functions of \( S_1^*, T_1^*, S_2^*, T_2^* \) and total load capacitance \( C_1 \) and \( C_2 \). The arrival time \( T_1^* \) at the output of Gate 1 equals arrival time \( T_1 \) at its input plus its gate delay. We have,

\[
S_1 = \text{ST}_1(S_1^*, C_1) 
\]

\[
S_2 = \text{ST}_2(S_2^*, C_2) 
\]

\[
T_1 = T_1^* + \text{DT}_1(S_1^*, C_1) 
\]

\[
T_2 = T_2^* + \text{DT}_2(S_2^*, C_2) 
\]

where, \( C_1 = C_{in} + C_{d1} + C_{x1} \) and \( C_2 = C_{d2} + C_{x2} \) are total load capacitances at Gate 1 and Gate 2 respectively. Analyzing the slew lookup at Gate 1 closely,

\[
S_1 = \text{ST}_1(S_1^*, C_1) 
\]

\[
= \text{ST}_1(S_1^*, C_{in} + C_{d1} + C_{x1}) 
\]

\[
= \text{ST}_1(S_1^*, C_{in} + C_{x1}) 
\]

\[
= \text{ST}_1(S_1^*, C_{in} + C_{x1} + C_{x}(1 - \beta_1)) 
\]

\[
= \text{ST}_1(S_1^*, C_{in} + C_{x1} + C_{x}(1 - \Delta V_2/V_{ih})) 
\]

\[
= \text{ST}_1 \left( S_1^*, C_{in} + C_{x1} + C_{x} \left( 1 - \frac{f_2(S_1, T_1, S_2, T_2, V_{ih})}{V_{ih}} \right) \right) 
\]

\[
S_1 = \text{ST}_1 \left( S_1^*, C_{in} + C_{x1} + C_{x} \left( 1 - \frac{f_2(S_1, T_1, S_2, T_2, V_{ih})}{V_{ih}} \right) \right) = 0 
\]

Similar analysis for slew lookup at Gate 2 gives,

\[
S_2 = \text{ST}_2 \left( S_2^*, C_{d2} + C_{x} \left( 1 - \frac{f_1(S_1, T_1, S_2, T_2, V_{ih})}{V_{ih}} \right) \right) = 0 
\]

Rewriting Equation 13 to Equation 16 as,

\[
F_T^0 (S_1, T_1, S_2, T_2, V_{ih}) = 0 
\]

\[
F_T^0 (S_1, T_1, S_2, T_2, V_{ih}) = 0 
\]

\[
F_T^0 (S_1, T_1, S_2, T_2, V_{ih}) = 0 
\]

\[
F_T^0 (S_1, T_1, S_2, T_2, V_{ih}) = 0 
\]

Solution of these equations gives us the required slew and arrival time numbers. These are non-linear equations, which can be solved by usual Newton Raphson iterations. Evaluation of the functions \( F_T^0 (.) \), \( F_T^0 (.) \), \( F_T^0 (.) \), \( F_T^0 (.) \) etc. and their derivatives with respect to \( S_1, T_1, \) etc. can all be interpreted in terms of table lookups into slew and delay tables for Gate 1 and Gate 2. The big catch however is that these functions are not differentiable at all points. This is mainly due to the \( \text{Min}(.) \) and \( \text{Max}(.) \) functions sitting inside \( f_1(.) \) and \( f_2(.) \) functions. The usual advantages of NR iterations are not thus forthcoming in this case. Something simpler, which works even better, is given below.

An alternative approach to solve Equation 17 to Equation 20 comes from their formulation itself. We start with initial values for \( C_{x1} \) and \( C_{x2} \). This could be computed using Miller Factor of 0 or 2X depending on the directions of signal switching at node 1 and node 2. Then we look-up into the slew and delay tables for Gate 1 and Gate 2 and hence compute \( V_1(t) \) and \( V_2(t) \). Finally calculate switching factors using these waveforms and then compute \( C_{x1} \) and \( C_{x2} \) using these switching factors. We iterate till convergence is obtained on the values of looked up slews and delays. The fixed-point solution of these equations is thus computed using an iterative table lookup scheme. Each iteration involves 4 table lookups (slew and delay tables for both the gates) and evaluation of \( \Delta V_1 \) and \( \Delta V_2 \) to compute the switching factors.

IV. MULTIPLE NET COUPLINGS

Simultaneous coupling of more than two nets can easily be handled. Note that in each iteration of the suggested scheme we get iterate values for slews, arrival times and de-coupling capacitance values at each coupled node. For an \( n \)-net coupled system having potentially \( n^2 \) couplings, we can perform fixed-point iterations computing a pair of switching factors for each coupling. Note that, in the presence of all possible couplings, the functions given in Equation 17 to Equation 20 get modified. We have for each node \( i \),

\[
F_T^0 (S_i, T_i, V_{ih}) = 0 
\]

\[
F_T^0 (S_i, T_i, V_{ih}) = 0 
\]

Where \( S = (S_1, S_2, \ldots, S_n) \) are the slews and \( T = (T_1, T_2, \ldots, T_n) \) are the arrival times at the output node of \( n \) driver gates \( G_1, G_2, \ldots, G_n \) respectively. Further,

\[
S_k = \text{ST}_k \left( S_{k', C_{ik} + \sum_{j \neq k} C_{j}} \right) 
\]

\[
T_k = T_k' + \text{DT}_k \left( S_{k', C_{ik} + \sum_{j \neq k} C_{j}} \right) 
\]
where, \( ST_x (.) \) and \( DT_x (.) \) are the Slew and Delay tables for \( k \)-th gate \( G_k \). \( C_{jk} \) is the lumped load capacitance at \( G_k \) (including the grounded interconnect capacitance and the input capacitances of the driven gates, and excluding the de-coupling capacitances) and \( C^\prime_{jk} \) is the de-coupled capacitor at the \( k \)-th node representing the de-coupling of the coupling capacitor between \( j \)-th and \( k \)-th node. Representing \( S^1, S^2, \ldots, S^n \) as \( k \)-th iterate for Slew and \( T^1, T^2, \ldots, T^n \) as \( k \)-th iterate for arrival times, we can solve the equations at each node as per the Gauss-Seidel scheme as follows,

\[
F^T_i (S^1_{j+k}, S^2_{j+k}, \ldots, S^n_{j+k}, T^1_{j+k}, T^2_{j+k}, \ldots, T^n_{j+k}, V_{ih}) = 0 \quad (25)
\]

\[
F^S_i (S^1_{j+k}, S^2_{j+k}, \ldots, S^n_{j+k}, T^1_{j+k}, T^2_{j+k}, \ldots, T^n_{j+k}, V_{ih}) = 0 \quad (26)
\]

Note that we have two equations (similar to Equation 25 and Equation 26) for each node \( i \). These equations are solved exactly as in the case of two single net coupling. Only that the slew and arrival times are computed at each net in succession, and the most recent iterates of the slew and arrival times are used in each such computations.

V. EXPERIMENTAL RESULTS

We conducted experiments to validate the correctness and efficacy of our method. We chose 0.18micron technology to obtain HSPICE models for gates and interconnect. Inverters of varying driving strengths were chosen as gates, and lines with length varying from 10 microns to 500 microns were chosen as interconnects. BSIM3 (Version 3.1, level 49) models were used for NMOS and PMOS devices in the CMOS inverters. Lumped C models were used for the interconnects.

We first generated slew and delay tables for a couple of inverter gates, INV1 and INV2. INV1 was a single stage inverter with input capacitance 11.50ff, and INV2 was a three stage inverter with input capacitance 23.0ff. The rise/fall times for the input signals were taken as 30ps for fast signal, 50ps for typical signal and 150ps for slow signals. For each of these input slews the load capacitance was varied from 10ff to 150ff. We measured the slew of the output waveform and the point to point delay at \( V_{DD}/2 \) point across input and output signals for each simulation. We would like to emphasize that these slew/delay tables are available with any static timing library. In order to have substantial coupling we took lines of length 200a. Typically such lines are found in higher layers. We use the technology parameters for the fifth layer of metal (M5) where the grounded capacitance for 200u line was 1.54ff and the coupling capacitance with other line running parallel at minimum separation was 18.7ff. All experiments were done for the simplified model shown in Figure 1.

In Figure 8 we give a simulation trace for the de-coupling approximation done with Gate 1 selected as INV2 and Gate 2 selected as INV1. The figure contains input voltage signals (\( V_1 \) and \( V_2 \)) and output voltage signals in coupled circuit (\( V_3 \) and \( V_4 \)) and de-coupled circuit (\( V_{3a} \) and \( V_{4a} \)). The de-coupling capacitors as computed by our method are \( C_{3a}=22.39ff \) and \( C_{4a}=56.09ff \). Note that the waveforms \( V_4 \) and \( V_{4a} \) have same delay at \( V_{DD}/2 \) point from input waveform \( V_2 \). This is achieved by taking \( V_{ih}=0.5V_{DD} \) in de-coupling computations.

The HSPICE simulation trace given in Figure 9 contains a slew matching approximation. Here \( V_{ih} \) is taken as 0.9\( V_{DD} \). Note that the transition time for 0.1\( V_{DD} \) to 0.9\( V_{DD} \) is identical in \( V_4 \) and \( V_{4a} \) waveforms. The coupling capacitor \( C_s \) for this case is also 18.7ff. The de-coupled capacitors are computed as \( C_{3a}=20.76ff \) and \( C_{4a}=35.66ff \).

We now report a de-coupling approximation on a three net-coupled circuit. The circuit is shown in Figure 10 and the simulation traces are given in Figure 11. Both the coupling capacitors are 18.7ff. The total de-coupling capacitor (summation of de-coupling capacitors due to both the couplings) at middle line is 37.39ff. Note that the delay of \( V_4 \) and \( V_{4a} \) are identical. The slew is also approximated nicely. The lines are 200u long at minimum separation in M5. \( V_{ih} \) was taken to be 0.5\( V_{DD} \).

The convergence of the iterative scheme is commonly achieved in 5-10 iterations. If it does not converge, then it usually oscillates between two solutions. In such cases we take the average of these solutions. If the iterative scheme diverge then we take the worst case value for the decoupling approximation. In the case of circuit given in Figure 10 the iterations oscillated between two solutions. The results reported in Figure 11 correspond to the average of these two solutions.

Each iteration involves computation of switching factors and table lookups. It took 4 seconds (on a 450MHz machine) to compute 1 million switching factors and to perform 1 million table lookups. The computational overhead to incorporate the suggested method in any static timing analysis tool is thus insignificant.
VI. COMMENTARY ON DE-COUPLED APPROXIMATIONS

Through de-coupling we are trying to ‘roughly’ approximate a second order (for a two net coupling) non-monotonic waveform with a first order monotonic waveform. There are bound to be errors. Consider the case shown in Figure 12, wherein a rising waveform is victimized by falling waveform in an adjacent net. This results in a dip in the waveform. The waveform no longer remains monotonic. With a de-coupling approximation we are trying to approximate the waveform with a monotonically increasing waveform. If the approximation matches the $V_{th}$ point (to match delay) then the slews are not matched. On the other hand, if it matches the slew then the delay is not matched. This problem can be avoided by computing multiple de-coupling approximations and using only the relevant slew and delay numbers from each approximation. The delay matching approximation can be obtained by choosing $V_{th}$ as $V_{DD}/2$. The slew matching approximation can be obtained by choosing $V_{th}$ as $0.9V_{DD}$. An even better slew number can be computed by choosing $V_{th}$ as $0.1V_{DD}$ and $0.9V_{DD}$ and computing the time-stamps at which $0.1V_{DD}$ and $0.9V_{DD}$ voltage points are crossed, and from there computing the slew.

As with Newton Raphson iterations, the iterative scheme given in Section III is not guaranteed to converge. It could lead into oscillations across two or more solutions. In such cases, a good engineering approximation is to take the arithmetic mean of these solution iterates and proceed forward. If instead of oscillations, divergence is observed then the worst case decoupling capacitance value can be used for computations.

VII. CONCLUSIONS

We have reported an iterative table lookup algorithm to efficiently account for the coupling effects during static timing analysis. The method is based on de-coupling of coupled capacitors through appropriately computed switching factors. The computation of these switching factors is done through predicted digital signals at the coupled nodes. The slew/delay results computed by our method are validated for 0.18-micron technology using HSPICE simulations. The salient features of the suggested method are as follows.

- The method is general enough to take into account multiple coupled nets.
- With the switching factor approach, the relative arrival times are naturally taken into account.
- The driver strengths are accommodated through the slew delay tables.
- The method is easy to implement in existing timing analysis tools. It only requires the usually available slew and delay tables for the driver gates.
- The computation of switching factors is very inexpensive.
- The emphasis is given not to the convergence of decoupling capacitance values, but to the convergence of slew and delay numbers. This may require multiple runs of iterations using different values of $V_{th}$.

REFERENCES