Development of a High-Rate High-Resolution Detector for EXAFS Experiments

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***Abstract*—A new detector for EXAFS experiments is being developed. It is based on a multi-element Si sensor and dedicated readout application specific integrated circuit (ASIC). The sensor is composed of 384 pixels, each having 1 mm^2 area, arranged in four quadrants of 12×8 elements and it is wire-bonded to 32-channel ASICs. Each channel implements low-noise preamplification with self-adaptive continuous reset, high-order shaper, bandgap referenced baseline stabilizer, one threshold comparator, and two digital-analog converter (DAC) adjustable window comparators, each followed by a 24-bit counter. Fabricated in 0.35 μm CMOS, the ASIC dissipates about 8 mW per channel. First measurements show at room temperature a resolution of 14 e^- rms without the detector and 40 e^- rms (340 eV) with the detector connected and biased. Cooling to -35 C a full width at half maximum (FWHM) of 205 eV (167 eV from electronics) was measured at the Mn-Kα line. A resolution of about 300 eV was measured for rates approaching 100 kc/s per channel, corresponding to an overall rate in excess of 10 $\mathrm{Mc/s/cm^2}$. Channel-to channel threshold dispersion after DAC adjustment 2.5 was e^- root mean square.**

***Index Terms*—EXAFS, readout ASIC, SI pixel sensor.**

I. Introduction

EXTENDED X-ray absorption fine structure (EXAFS) experiments impose stringent requirements on a detection system due to the need for processing ionizing events at a high rate, typically above 10 $\mathrm{Mcps/cm^2}$, and with a high resolution, typically better than 300 eV FWHM 35 e^- root mean square (rms) in Si.

The detection system described here is being developed to address these stringent requirements. It is the result of a cooperation, started in mid 2001, between the Instrumentation Division and the National Synchrotron Light Source (NSLS) of Brookhaven National Laboratory (BNL) and it will be used at one of the NSLS beam lines. It is composed of a pixellated Si sensor fabricated at BNL and dedicated low-noise application specific integrated circuit (ASIC). The combination of high rate, high resolution and moderate complexity makes this system attractive in comparison to others [1], [2]. Sections II–V the sensor, electronics, front-end interconnects, and readout interface are described, respectively. Section VI reports on the first experimental results on single-quadrant prototypes.

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II. Multi-Element Si Sensor

The Si sensor is composed of 384 pixels each having a 1 mm $\times$ 1 mm area, arranged in four quadrants of 12×8 elements (Fig. 1) and it was fabricated at the Semiconductor Detector Laboratory of the Instrumentation Division, BNL. The pixels were formed using p^+ boron implant ($\approx 10^{14}/\mathrm{cm^2}$ at 40 keV) on a high-resistivity (4–6 $\mathrm{k\Omega cm}$) n-type 250 μm thick wafer with (111) orientation, with a planar n^+ ohmic contact on the back side, using phosphorous implant ($\approx 10^{14}/\mathrm{cm^2}$ at 150 keV). Connectivity to each pixel is provided by a 100 μm$\times$ 100 μm aluminum bond pad. The pattern of pads was developed to minimize the complexity of the wire-bonding operation (see Section IV and Fig. 4).

The silicon extends about 8 mm beyond the active area on each side in order to accommodate the readout ASICs and the Peltier cooling elements.

The opening in the center allows the beam to pass through the detector from the pixellated side, and the fluorescence from the sample is measured on the nonpixellated side. With this approach it is possible to place the sensor very close to the sample, thus increasing the solid angle and rate, with consequent reduction of the EXAFS measurement time.

In order to address the problem of pixel-to-pixel charge sharing and inter-pixel charge trapping [3], sensors were fabricated having inter-pixel gaps of 10 μm, 20 μm, and 50 μm. A test structure with gaps variable from 6 μm to 16 μm was also fabricated and tested in order to evaluate spectral degradation with respect to the pixel gap. Two 8 mm strip versions with 125 μm pitch and gap of 10 μm and 50 μm (compatible with the ASICs) were also fabricated to expand the range of applications.

III. Mixed-Signal Front-End ASIC

A mixed-signal ASIC was designed at the Instrumentation Division and fabricated in 0.35 μm CMOS, dual-poly, four-metal (DP-4M) 3.3 V technology. It is composed of 32 channels plus bias circuitry and digital interface, a total of 180 000 MOSFETs, and it dissipates about 8 mW per channel. The layout, which is optimized for minimization of pick up from mixed signal activity, measures 6.3×3.6 $\mathrm{mm^2}$ (Fig. 2).

Each channel implements (Fig. 3) a low-noise preamplifier, a high-order shaper with baseline stabilizer, one threshold and two window discriminators with digital-analog converters (DACs)

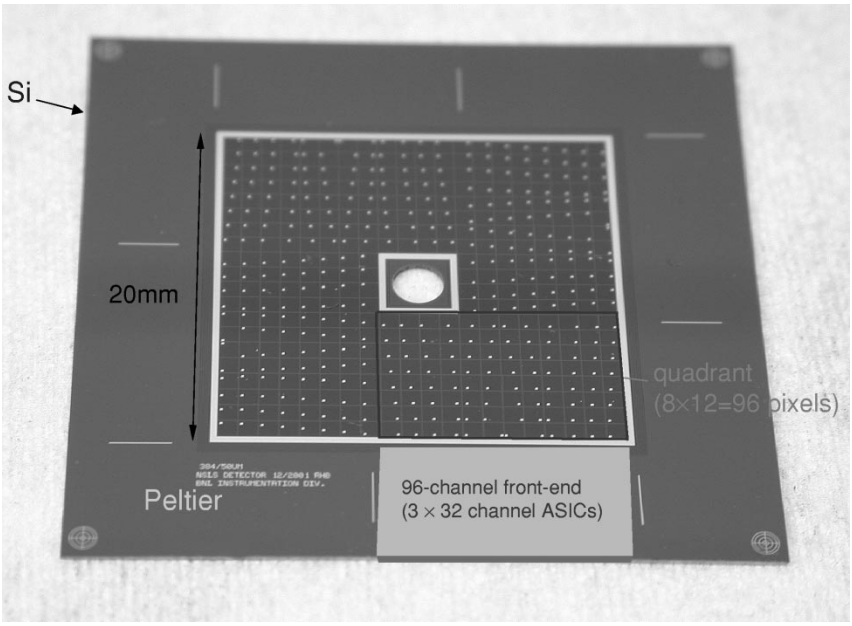

Fig. 1. Photo of the Si sensor (384 square pixels, 1 mm^2 each). The ASICs sit on Si, off the long side of each quadrant; the Peltier elements sit on Si, on the remaining passive area. The center is opened for beam-through operation.

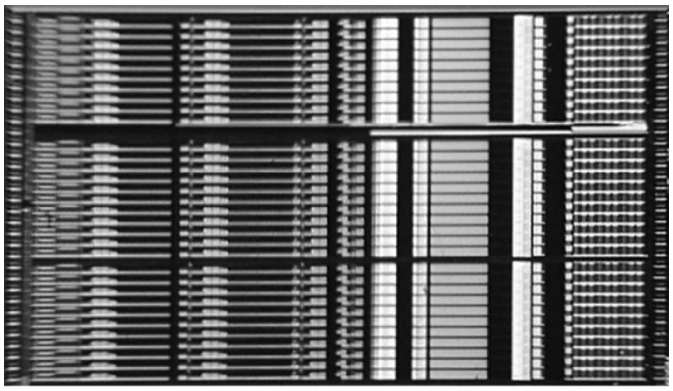

Fig. 2. Photo of the 32 channel ASIC, composed of 180 000 MOSFET. Three ASICs serve one quadrant (96 pixels) of the Si sensor.

for fine adjustment, one counter per discriminator. A detailed description of the electronics is reported below.

The preamplifier has a p-channel input MOSFET with $W/L = 400/0.35$, $I_d = 850\ \mu\mathrm{A}$, $V_{ds} = 800\ \mathrm{mV}$, $g_m = 8.6\ \mathrm{mS}$, and $C_g = 620\ \mathrm{fF}$. The p-channel was selected because of its lower 1/f noise when compared to the n-channel, and the size was optimized taking into account its operating regime. The input parasitic capacitance (pad plus wire-bond) ranges from around 270 fF to 420 fF, depending on the wire-bond length.

The preamplifier incorporates an n-channel MOSFET in feedback, operating in saturation to realize a low-noise fully compensated continuous reset circuit of the type described in [4]. The configuration is self-adaptive to leakage currents from the sub-pA to the nA scale. The reset circuitry contributes parallel noise, which, in the worst case of weak inversion operation, is equal to the shot noise of the pixel leakage current. A charge gain of 32 is provided. A cascade of two of these stages, the second of which, based on p-channel MOSFET in feedback, provides an overall gain of $32 \times 32 = 1024$ from the detector to the input of the first stage of the shaper. The 192 $\mathrm{k}\Omega$ feedback resistor of the shaper thus contributes an equivalent input shot noise of 240 fA.

The second and third stages of the shaper provide two pairs of complex conjugate poles, forming a fifth order complex semi-Gaussian shaper. The high-order shaper was chosen for its better noise filtering performance (up to 2.6 times compared to a low order) in the high-rate regime, where white series noise dominates. The output stage adds a gain of four. Its output baseline is referenced to a bandgap circuit and an error voltage is fed back to the input of the second stage of the shaper through a slew-rate limited follower and a very low frequency filter, thus realizing a BLH configuration [5] for the baseline stabilization. The analog processing chain has an adjustable peaking time (0.5 μs, 1 μs, 2 μs, 4 μs), and gain (750 mV/fC, 1500 mV/fC). The analog output and a pixel leakage current monitor, with equivalent gain $\approx 8\ \mathrm{G}\Omega$, can be routed to two global analog outputs through digital setting.

The shaper output is fed to one single-threshold and two window-discriminators. The five threshold levels are coarsely set through external voltages common to all channels. Each threshold level of the two windows can be individually adjusted through a 6-bit DAC with 1.6 mV step. Each discriminator is followed by a 24-bit counter (three counters per channel). During the data readout phase, the counters of all 32 channels are converted into a single shift register for serial reading.

A serial peripheral interface is also included for global settings, monitor enabling, channel masking, DAC adjustment, and counter readout. The channel area is 5854 $\mu\mathrm{m}$ by 102 $\mu\mathrm{m}$. In the long dimension, 1929 $\mu\mathrm{m}$ is dedicated to the comparators and DACs and 690 $\mu\mathrm{m}$ to the three 24-bit counters.

The power dissipated by the overall chain is 8 mW, with 3 mW dedicated to the preamplifier.

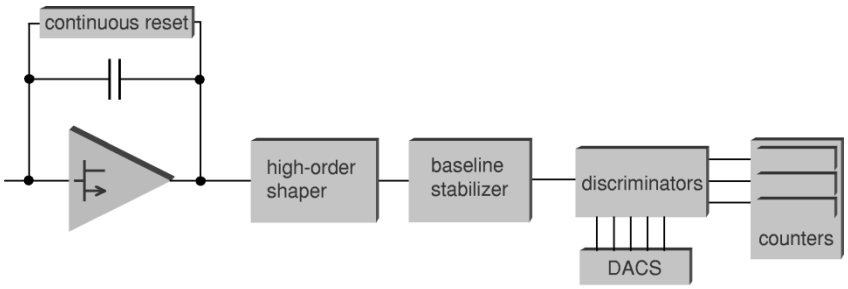

Fig. 3. Simplified schematic of one channel of the ASIC.

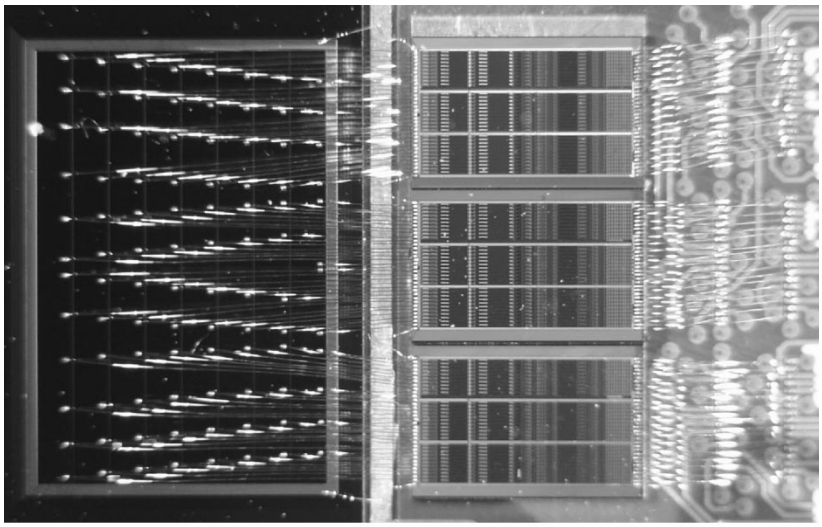

Fig. 4. Photo of a single-quadrant prototype. The 96 pixels are wire-bonded to the inputs pads of three 32-channel ASICs.

IV. Front-End Interconnects

Four pixel-to-electronics interconnect solutions were initially considered: (i) adoption of strips in place of pixels to minimize the wire-bond length to the input pads of the front-end ASICs; (ii) metal traces integrated on the Si sensor to bring the wire-bond pads closer to the input pads of the front-end ASICs; (iii) adoption of pixellated ASIC layout with low-capacitance ball grid array for direct bump-bonding to the pixellated Si sensor; and (iv) direct wire-bond of each pixel to corresponding input pad of the front-end ASIC.

The major drawback of solution (i) was the increase in perimeter/area ratio when compared to square pixel, with consequent degradation of the spectral quality arising from the increased capacitance and enhanced charge sharing.

Solution (ii) was affected, along with the excessive interconnect capacitance C_p, by the contribution to the ENC from dielectric loss in the insulator under the metal traces (polyimide, SiO_2, Si_3N_4 were considered). This contribution is given by [6]

$$\delta\mathrm{ENC} \approx \sqrt{2kTC_p \tan(\delta)} \tag{1}$$

where $\tan(\delta)$ is the dielectric loss of the material. For example, in the case of a Si_3N_4 dielectric ($\varepsilon_r \approx 6.5$, $\tan(\delta) \approx 0.001$) with thickness 2 μm, an interconnect line measuring 6 mm $\times$ 10 μm, the loss contribution would be $\delta\mathrm{ENC} \approx 20e^-$ rms. This contribution is in addition to the increase in series noise due to C_p itself.

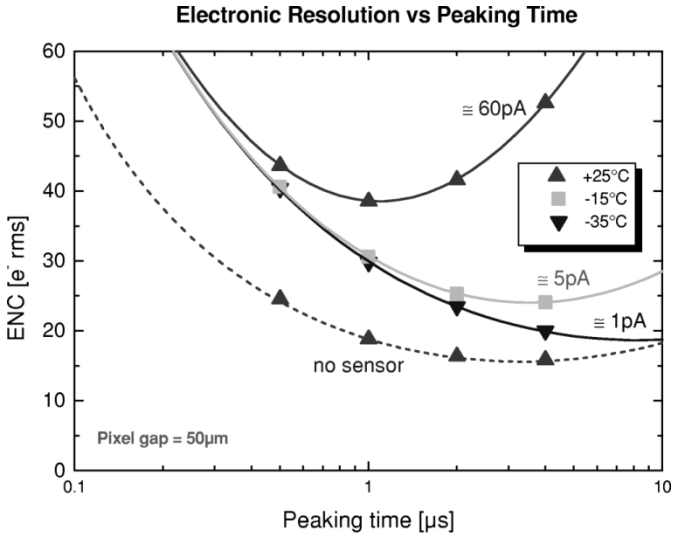

Fig. 5. Measured electronic resolution (ENC) versus peaking time at different temperatures for a pixel with 50 μm gap. The ENC without bonding the pixel to the ASIC input pad is also shown. Curve fitting is theoretical.

Drawbacks of solution (iii) were the ball grid material, which, if not carefully selected could lead to anomalous fluorescence

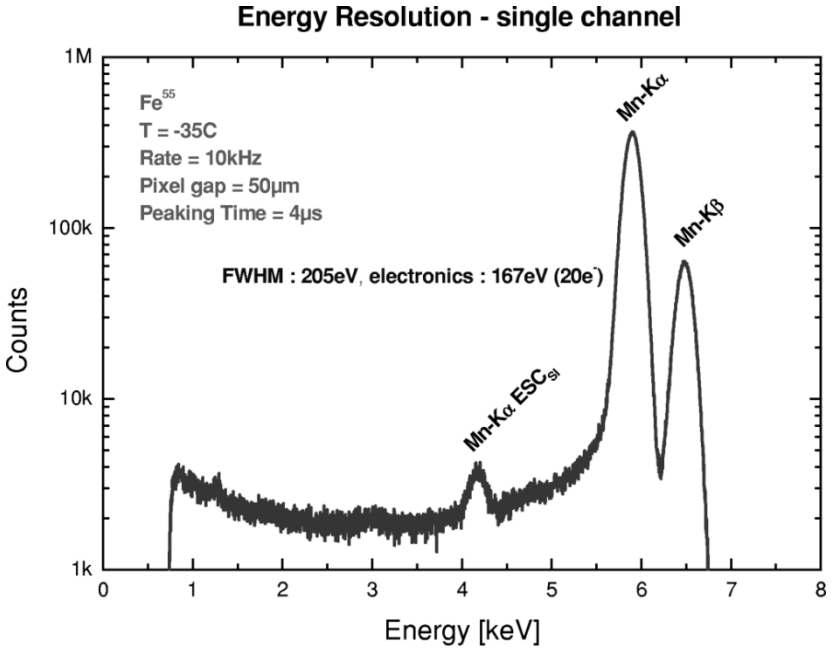

Fig. 6. Spectrum of an $^{55}\mathrm{Fe}$ source measured at $-35\,^{\circ}\mathrm{C}$. The FWHM of Mn-Kα peak is 205 eV (167 eV = 20 e^- from electronic noise).

peaks in the measured spectra, and the constraints imposed to the area and layout of the ASIC. It would also prevent the use of the same ASIC for the Si strip versions. Furthermore, this solution precludes the option to illuminate the sensor from the active side for test purposes.

Solution (iv) was selected on the basis of lack of complexity plus low parasitic capacitance. This capacitance is in the region of 50–200 fF which is negligible when added to other sources of load capacitance present at the front-end ($\approx$ 950–1250 fF). Stability and microphonics related to the length of the bonds, originally considered an issue, have shown to be of negligible effect throughout the first phase of measurements.

Single-quadrant prototypes (96 pixels) were assembled and tested up to now (see Fig. 4). Corresponding experimental results are reported in Section VI.

V. Readout Interface

In order to set and read out the 32-channel ASICs an interface board was developed. It includes one Microcontroller module (MC78VZ328), RAM, two DACs, RS232, and Ethernet interfaces. It offers multichannel analysis capability through the implementation of one high-resolution peak detector, recently developed at the Instrumentation Division [7] and one analog-digital converter (ADC).

Software with a user-friendly interface aimed to fully control the system was also developed. It provides several useful functions along with multichanneling and automatic threshold equalization.

VI. First Experimental Results

To date, only single-quadrant prototypes (with 96 pixels) have been assembled and characterized. The resolution versus temperature, pixel gap, pixel rate, and switching noise from the digital circuitry of the ASIC have been investigated.

Fig. 5 shows the electronic resolution, expressed in equivalent noise charge (ENC), as function of the peaking time for a pixel with 50 μm gap. The resolution was measured at room temperature without bonding the pixel to the ASIC input pad (up triangle, dashed line) and with the pixel bonded and biased (up triangle, solid line).

In the first case, an internal 2.5 pA current source $\approx$ simulating the pixel leakage current was enabled. This current is required in order to activate the feedback MOSFET of the continuous reset in absence of pixel leakage current [4] and contributes shot noise.

Once the pixel is bonded and biased, the increase in ENC at short peaking times is due to the increase in input capacitance, from 220 fF (ASIC bonding pad) to 1050 fF (wire-bond, pixel). The increase in ENC at long peaking times is related to the pixel leakage current, which is $\approx$ 60 pA for this sample. An ENC $\approx$ 39 e^- rms at a peaking time of 1 μs was measured in this case, to be compared to 14 e^- rms with a 4 μs peaking time of the previous case.

At $-15^{\circ}\mathrm{C}$ and $-35^{\circ}\mathrm{C}$ the leakage current decreases and the resolution improves to 20 e^- rms at a peaking time of 4 μs.

In Fig. 6 the spectrum of an Fe^{55} source measured at $-35^{\circ}\mathrm{C}$ with a 4 μs peaking time and for 50 μm pixel gap is shown. A FWHM of 205 eV (167 eV = 20 e^- due to electronic noise) at Mn-Kα peak can be extracted. The average resolution for this kind of pixel was measured to be 220 eV, with a $\pm 7\%$ dispersion and very few bad channels exhibiting a noise one order of magnitude higher or more than average. In Fig. 6 the Si escape from Mn-Kα can also be observed.

A version of the Si sensor with pixel gaps varying from 6 μm to 15 μm in steps of 1 μm was measured. In Fig. 7, these Fe^{55} spectra, along with the 50 μm gap case, are shown. The

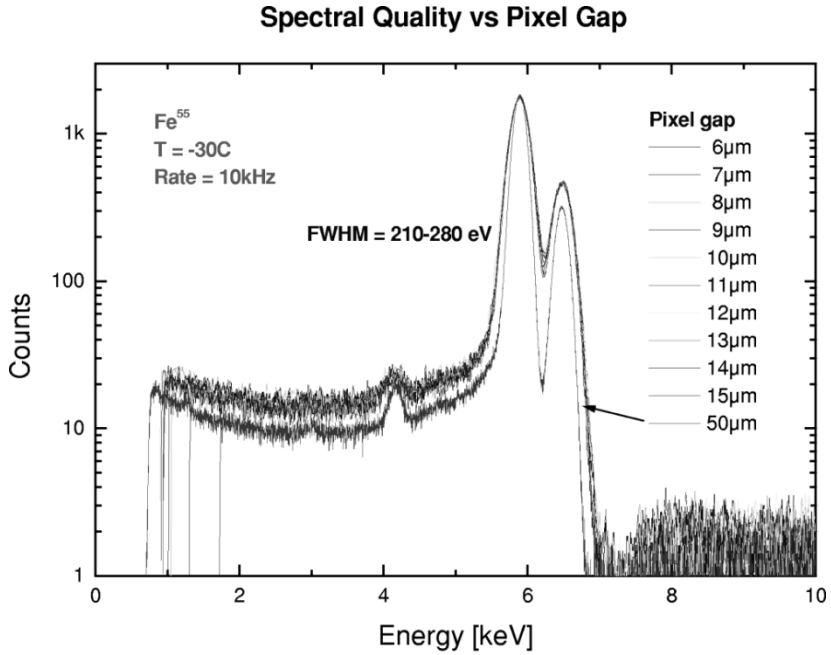

Fig. 7. Spectrum of an $^{55}\mathrm{Fe}$ source measured at $-30^{\circ}\mathrm{C}$ for pixel gaps 6–15 $\mu\mathrm{m}$ 50 $\mu\mathrm{m}$.

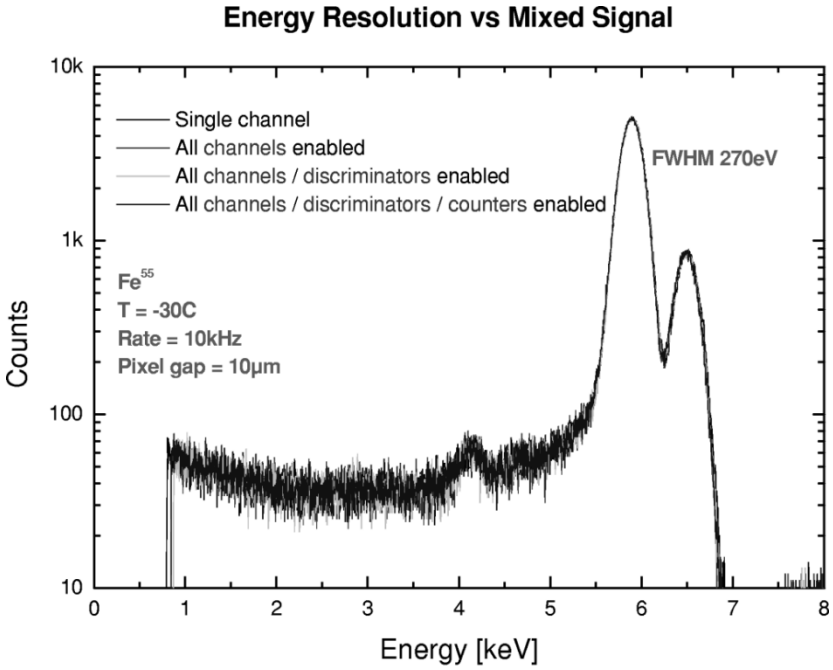

Fig. 8. Spectra of an $^{55}\mathrm{Fe}$ source measured at $-30^{\circ}\mathrm{C}$ for pixel gap 50 $\mu\mathrm{m}$, while progressively enabling all channels, discriminators, and counters.

better spectral quality (FWHM, peak-valley, and peak-tails) of the 50 $\mu\mathrm{m}$ case is due to the lower pixel capacitance (700 fF plus interconnect, compared with 1000 fF plus interconnect for the 10 $\mu\mathrm{m}$ case). No appreciable degradation due to fixed charges in the oxide for the large gap [3] was observed at this level.

Layout techniques aimed at minimizing the pickup from mixed signal activity (from comparators, counters and adjacent channels) on the resolution were developed. These techniques included dedicated analog and digital supply and ground, a dedicated line for substrate/body contacts of digital MOSFETs and wide substrate contacts between the analog, the comparator and the digital sections of each channel, and between channels.

In Fig. 8 the effect of pickup from mixed signal activity on the resolution is shown on a spectrum of a Fe^{55} source measured at $-30^{\circ}\mathrm{C}$ with a 4 $\mu\mathrm{s}$ peaking time and for a 10 $\mu\mathrm{m}$ pixel gap. No degradation was observed in starting from a fully analog single channel activity and progressively enabling adjacent channels, discriminators, and counters.

In Fig. 9, the dependence of the resolution on the rate, expressed in terms of full width at half maximum (FWHM) of the Mn-Kα peak from an Fe^{55} source, for a 10 $\mu\mathrm{m}$ pixel gap is shown. A resolution at 100 kHz of 350 eV at a peaking time of 1 $\mu\mathrm{s}$ was measured, compared to 300 eV measured for a 50 $\mu\mathrm{m}$ pixel gap.

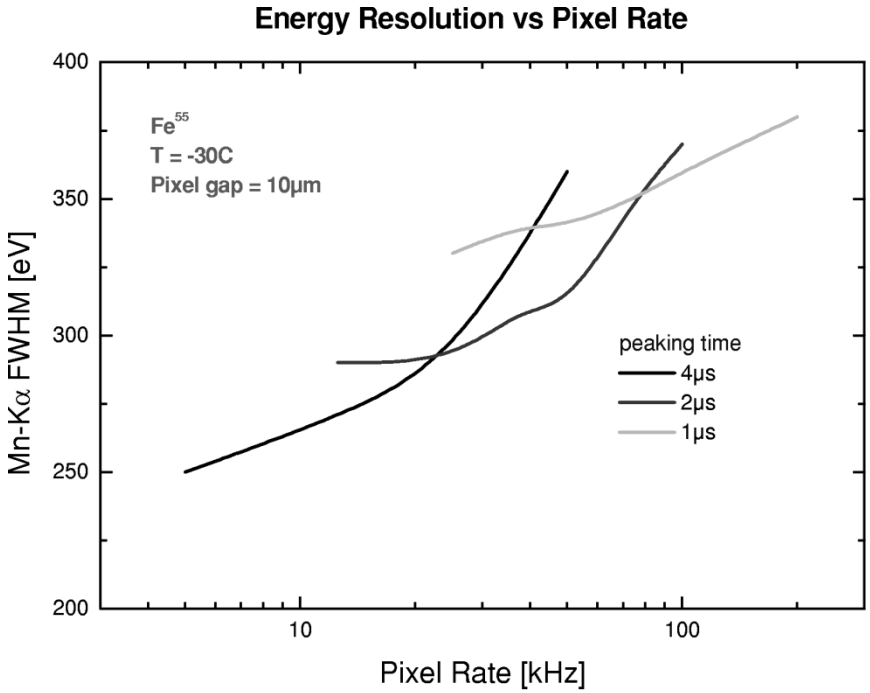

Fig. 9. Resolution expressed in Mn-Kα FWHM of an Fe^{55} source measured as function of the pixel rate for different peaking times.

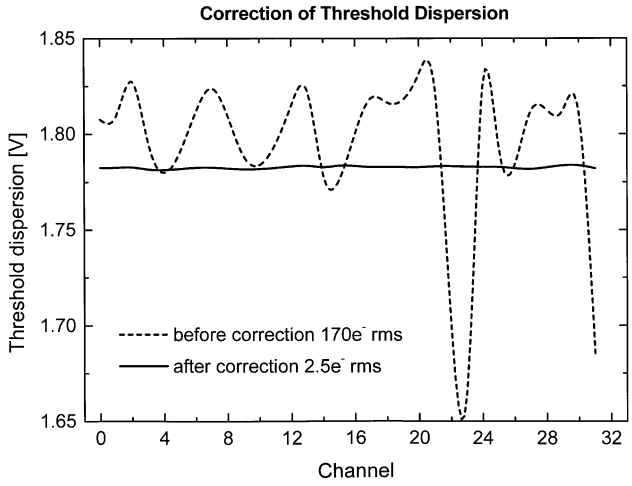

Fig. 10. Measured threshold dispersion before (circles) and after (squares) DACs adjustment.

EXAFS measurements with multi-element sensors require a high channel-to-channel threshold uniformity. A channel-to-channel threshold dispersion is equivalent to an additional source of noise. In this ASIC the major source of threshold dispersion is the mismatch between the input MOSFETs of the comparators. The dispersion can be contained within the noise by individually adjusting the threshold of each comparator. To this purpose each channel implements two 6-bit DACs per window-discriminator. The channel-to-channel threshold dispersion before and after DAC adjustment was measured and it is shown in Fig. 10 for one threshold. The standard deviations before and after adjustment correspond to 170 and 2.5 e^- rms, respectively.

Noise measurements made with threshold scans, direct measurement of the analog monitor output and X-ray resolution are in good agreement. A baseline shift with temperature of less than one megavolt was also observed.

VII. Conclusion and Future Work

First experimental results on single quadrant (96 pixels) prototypes show stability, rate, resolution, and uniformity within the expectations. The version with larger pixel gap of 50 $\mu\mathrm{m}$ appears preferable in terms of spectral quality. Prototypes with gap larger than 50 $\mu\mathrm{m}$ may be considered for next fabrication cycle.

The four-quadrant version (384 pixels) will be assembled and tested in near future. Overall results indicate that this version should approach the required 40 MHz global rate with a resolution on the order of 300 eV.

For optimization purposes, a second ASIC iteration and a second sensor iteration are being considered.

Acknowledgment

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