Minimum Component Based First-Order All-Pass Filter with Inverting and Non-Inverting Outputs

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Abstract—In this paper, a new voltage-mode first order all-pass filter using minimum active and passive components is presented. The proposed circuit employs one fully differential second generation current conveyor (FDCCII), one grounded capacitor, one resistor and offers the following advantages: the use of only grounded capacitor which is attractive for integrated circuit implementation, low active and passive sensitivities, providing inverting and non-inverting voltage-mode all-pass responses simultaneously from the single configuration and no requirement for component matching conditions. The theory is validated through PSPICE simulation using TSMC 0.35µm CMOS process parameters.

Index Terms—analogue signal processing, all-pass filter, voltage-mode.

I. INTRODUCTION

First order all-pass filters are an important class of analogue signal processing circuits which have been extensively researched in the technical literature [1-2] due to their utility in communication and instrumentation systems, for instance as a phase equalizer, phase shifter or for realizing quadrature oscillators band pass filters etc. A voltage-mode all-pass filter with minimum component is expected to use two passive components and one active element. Since two component based circuits are free from matching problems as both pole and zero frequency depend on the same two components such circuits would benefit from easy control over the pole frequency, as only a single element need to be controlled unlike the circuits require three components. In the literature, several voltage-mode all-pass filter circuit employing different types of active elements such as current conveyors and its different variations have been reported [3-20]. Some voltage-mode circuits benefit from minimum component count and hence require no matching constraints [10-11, 13-14, 16-17]. However, none of the reported circuit using minimum component count provides inverting and non-inverting all-pass response simultaneously from the single configuration. This paper proposes a new configuration for realizing inverting and non-inverting voltage-mode all-pass filters with different phase responses together using single active element, and two passive components. This feature not collectively exhibited in any of the reported work in the literature, including the most recent and useful circuit [19-20]. The proposed circuit is based on FDCCII, an active element to improve the dynamic range in mixed mode application, where fully differential signal processing is required [21]. PSPICE simulation results using TSMC 0.35µm CMOS parameters are given to validate the circuits.

II. CIRCUIT DESCRIPTION

The fully differential second generation current conveyor (FDCCII) is an eight terminal analog building block with the defining matrix equation of the form

\[
\begin{bmatrix}
\frac{I_1}{V_1} \\
\frac{I_2}{V_2} \\
\frac{I_3}{V_3} \\
\frac{I_4}{V_4} \\
\frac{V_{X+}}{V_X} \\
\frac{V_{X-}}{V_X} \\
\frac{I_{Z+}}{V_Z} \\
\frac{I_{Z-}}{V_Z}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -1 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 \\
V_4 \\
I_{X+} \\
I_{X-} \\
I_{Z+} \\
I_{Z-}
\end{bmatrix}
\]

(1)

The CMOS implementation of FDCCII is shown in Fig. 1 [21]. FDCCII is a useful and versatile active element for analog signal processing [21-22].
The proposed voltage-mode all-pass filter circuit using a single FDCCII, one grounded capacitor and one resistor is shown in Fig. 2. The circuit is characterized by the following voltage transfer functions:

\[ \frac{V_{\text{OUT}1}}{V_{\text{IN}}} = \frac{s - (1/RC)}{s + (1/RC)} \]  

\[ \frac{V_{\text{OUT}2}}{V_{\text{IN}}} = \frac{s - (1/RC)}{s + (1/RC)} \]  

Equations (2)-(3) is the standard first-order all-pass transfer function. The circuits of Fig. 2, thus provides a unity gain at all frequencies and frequency dependent phase function (\(\Phi\)) with a value \(\Phi = -2 \tan^{-1}(\omega RC)\) for (2) and \(\Phi = 180^\circ - 2 \tan^{-1}(\omega RC)\) for (3).

The salient features of the proposed circuit is realizing inverting and non-inverting voltage-mode all-pass filters with different phase responses simultaneously using single active element, and two passive components, the feature not exhibited together in any of the available works [3-20]. The circuit also enjoys one of the voltage output at low impedance thus making them suitable for voltage-mode cascading.

### III. NON-IDEAL ANALYSIS

To account for non ideal sources, two parameter \(\alpha\) and \(\beta\) are introduced where \(\alpha_i (i=1,2)\) accounts for current transfer gains and \(\beta_i (i=1,2,3,4,5,6)\) accounts for voltage transfer gains of the FDCCII. These transfer gains differ from unity by the voltage and current tracking errors of the FDCCII. More specifically, \(\alpha_i = 1 - \delta_i\) (where \(|\delta_i| \ll 1\)) where current tracking error \(\delta_i\) (from \(X^+\) to \(Z^+\)) and \(\delta_2\) (from \(X^-\) to \(Z^-\)). Similarly, \(\beta = 1 - \epsilon_i\) (where \(|\epsilon_i| \ll 1\)) where voltage tracking errors \(\epsilon_1\) (from \(Y_1\) to \(X^+\)), \(\epsilon_2\) (from \(Y_2\) to \(X^+\)), \(\epsilon_3\) (from \(Y_3\) to \(X^+\)), \(\epsilon_4\) (from \(Y_1\) to \(X^-\)), \(\epsilon_5\) (from \(Y_2\) to \(X^-\)), and \(\epsilon_6\) (from \(Y_4\) to \(X^-\)), respectively. Incorporating the two sources of error onto ideal input-output matrix relationship of the modified FDCCII leads to:

\[
\begin{bmatrix}
I_{V_1} \\
I_{Y_2} \\
I_{Y_3} \\
I_{V_4} \\
V_{\text{out}+} \\
V_{\text{out}-}
\end{bmatrix}
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 & 0 \\
-\beta_4 & \beta_5 & \beta_6 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \alpha_4 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \alpha_2 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_{V_1} \\
V_{V_2} \\
V_{V_3} \\
V_{V_4} \\
V_{X^+} \\
V_{X^-} \\
V_{Z^+} \\
V_{Z^-}
\end{bmatrix}
\]  

The circuits of Fig. 2 is analyzed using (4) and the non-ideal voltage transfer functions are found as
Thus, the pole frequency \( \omega_o \) of the first order all-pass filter circuit of Fig. 2 can be expressed as

\[
\omega_o = \frac{\beta \alpha _2}{RC}
\]

(7)

From (7), the pole frequency \( \omega_o \) sensitivities can be expressed as

\[
S_{R,C}^{\omega_o} = -1; \quad S_{\beta \alpha}^{\omega_o} = 1; \quad S_{\beta \beta \alpha \alpha}^{\omega_o} = 0;
\]

(8)

From (8), the sensitivities of active and passive components with respect to pole frequency \( \omega_o \) are within unity in magnitude. Thus, the circuit enjoys attractive active and passive sensitivity performance.

IV. SIMULATION RESULTS

The proposed circuits were verified using PSPICE simulation. The FDCCII was realized using CMOS implementation as shown in Fig. 1 [21] and simulated using TSMC 0.35\( \mu \)m, Level 3 MOSFET parameters as listed in Table 2. The aspect ratio of the MOS transistors are listed in Table 3, with the following DC biasing levels \( V_{dd}= -V_{ss}=3V, V_{bp}=V_{bn}=0V, \) and \( I_B=I_{SB}=1.2mA. \)

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W(( \mu )m)</th>
<th>L(( \mu )m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M6</td>
<td>60</td>
<td>4.8</td>
</tr>
<tr>
<td>M7-M9, M13</td>
<td>480</td>
<td>4.8</td>
</tr>
<tr>
<td>M10-M12, M24</td>
<td>120</td>
<td>4.8</td>
</tr>
<tr>
<td>M14, M15, M18, M19, M25, M29, M30, M33, M34</td>
<td>240</td>
<td>2.4</td>
</tr>
<tr>
<td>M16, M17, M20, M21, M26, M31, M32, M35, M36</td>
<td>60</td>
<td>2.4</td>
</tr>
<tr>
<td>M22, M23, M27, M28</td>
<td>4.8</td>
<td>4.8</td>
</tr>
</tbody>
</table>

The circuit of Fig. 2 was designed with \( C=1 \) nF and \( R=1 \) k\( \Omega \). The designed pole frequency was 159.2 KHz. The phase and gain plot is shown in Fig. 3. The phase is found to vary with frequency from 180\(^{\circ}\) to 0 for \( V_{OUT1} \) and from 0 to -180\(^{\circ}\) for \( V_{OUT2} \) with a value of 90\(^{\circ}\) and -90\(^{\circ}\) at the pole frequency, and the pole frequency was found to be 155.6 KHz, which is in error by \( \approx 2\% \) with the designated value. The circuit was next used as a phase shifter introducing 90\(^{\circ}\) and -90\(^{\circ}\) shift to a sinusoidal voltage input of 1volt peak at 155.6 KHz was applied. The input and \( \pm 90^{\circ} \) phase shifted output waveforms (given in Fig. 4) which verify circuit as a phase shifter. The THD variation at the output for varying signal amplitude at 155.6 KHz was also studied and the results shown in Fig. 5. The THD for a wide signal amplitude (few mV-1000mV) variation is found within 4.3\% at 155.6 KHz.

![Figure 3](image-url)  
**Figure 3.** Simulated gain and phase response of Fig. 2 at voltage output terminals.

![Figure 4](image-url)  
**Figure 4.** Time-domain waveforms of the Fig. 2 at input frequency 155.6 KHz.
V. INTEGRATION ASPECTS

The proposed circuit is can be conveniently implemented in CMOS technology. The resistor can be replaced by active-MOS resistor with added advantage of tunability through external voltage [23]. Similarly, there are techniques of implementing capacitor in MOS technology [24]. Since the used capacitor is in grounded form, it is further favorable as far as implementation is concerned. Thus the proposed circuits are quite suitable for IC implementation.

VI. CONCLUSION

This paper has presented a new voltage-mode first order all-pass filter employing one FDCCII, one grounded capacitor and resistor. The salient features of the proposed circuit is use of grounded capacitor, suitable for IC implementation, providing inverting and non-inverting voltage-mode all-pass responses simultaneously from the circuit and also providing one of the voltage output at low impedance thus making them suitable for voltage-mode cascading. The proposed circuit is verified through PSPICE simulation using 0.35µm TSMC parameters. The integration of the proposed circuit is an open area for further research.

REFERENCES