POWER EFFICIENT DESIGN OF MULTIPLEXER USING ADIABATIC LOGIC

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ABSTRACT

This paper provides low power solutions for Very Large Scale Integration design. The dynamic power consumption of CMOS circuits is rapidly becoming a major concern in VLSI design. By adiabatic technique dynamic power consumption in pull up network can be reduced and energy stored on the load capacitance can be recycled. In this paper different logic style multiplexes have been analyzed and low power 2:1 multiplexer is designed using positive feedback adiabatic logic. It has been observed that adiabatic multiplexer consumes 53.1% less power than energy economized pass-transistor (EEPL) multiplexer. An adiabatic compressor has been designed using PFAL logic, which has shown 79% improvement than conventional CMOS compressor in terms of power. All the simulations are carried out by Microwind 3.1 tool.

KEYWORDS: *MUX, PFAL, CMOS, VLSI, BSIM4.*

I. INTRODUCTION

In today's world of portable devices such as laptops, cell phones, computer power consumption has become major concern in VLSI design. Due to the limited power supplied by the batteries, the circuitry involved in these devices must be designed to consume less power. Also large power dissipation requires expensive and noise cooling machinery, batteries and power conservation circuits. Multiplexer is essential component in digital design. It is extensively used within datapath-intensive designs. Thus minimizing the power dissipation of the multiplexer is one of the main concerns of low power design [1].

Most of the power saving techniques involved scaling of the power supply, which results, substantial increase in subthreshold leakage current also it causes uncertainty in the process variation. Therefore some other technique is required which is independent of voltage scaling. It has been found that there is fundamental connection between computation and power dissipation. That is if somehow computation could be implemented without any loss of information, then energy required by it could be potentially reduced to zero. This can be achieved by performing all the computation in a reversible manner. Thus minimum power consumption during charge transfer phase is known as adiabatic switching. Conventional CMOS based designs consume a lot of energy during switching process. Adiabatic switching technique reduces the energy dissipation through PMOS during charging process and reuses some of the energy which is stored on load capacitor during the discharging phase [2-3].

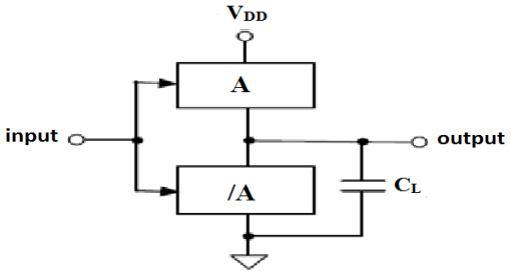

Fig.1 Conventional CMOS logic circuit with pull-up (A) and pull down (/A) network

In fig. 2 output load capacitance is charged by a constant current source instead of a constant voltage source used in conventional CMOS structures. On resistance of pull up PMOS network is represented by R and C_0 is the output capacitance [3]. Amount of energy dissipated through R can be given as

$$E_{diss} = I_s^2.R.T \quad (1)$$

$$E_{diss} = \frac{RC_0}{T} C_0 V_c^2(T) \quad (2)$$

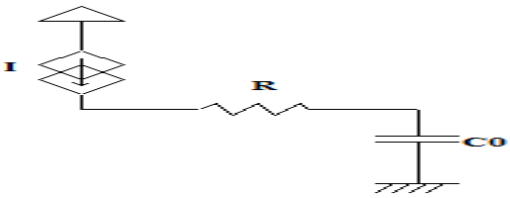

Fig. 2 Equivalent model during charging process in adiabatic circuits.

Thus energy dissipation depends upon on resistance R, by reducing it energy dissipation can be minimized. Also by increasing the charging time greater than $2RC_0$ dissipation can be reduced up to large extent. By reversing the direction of constant current source energy stored on capacitor can be achieved. Adiabatic circuits do not employ standard power supplies as in CMOS circuits, it uses pulsed power supply [4].

A multiplier can be divided into 3 parts: a Booth encoder, a partial product summation tree and a final adder. The partial product summation tree is responsible for a significant portion of the total multiplication delay and 4-2 compressor can be used to construct the tournament adder with a regularly structured Wallace tree, giving low complexity load capacitances [5]. Multiplexer and XOR based compressor realization is shown in Fig. 3.

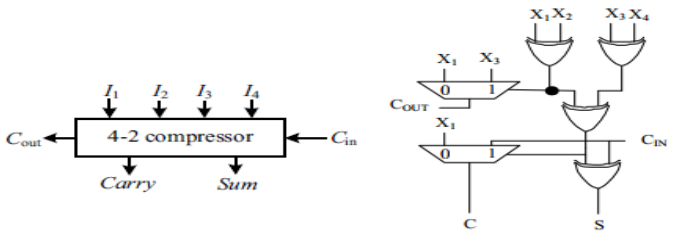

Fig. 3 4-2 Compressor using XOR and Multiplexer [6]

II. MULTIPLEXER DESIGNS

A logic style is the way how a logic function is derived from a set of transistors. It affects the speed, size, and power consumption and wiring complexity of a circuit. All these characteristics may vary considerably from one logic style to another and thus make the proper choice of logic style crucial for circuit performance [7]. DCVSL MUX is shown in Fig. 4.

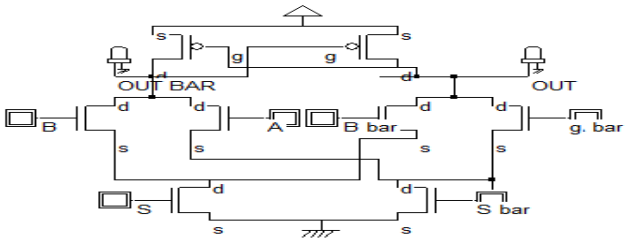

Fig. 4 Schematic design of DCVSL 2:1 Multiplexer [9].

The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. All functions are implemented using NFETS only, and PFETS serve only as the pull-up devices. DCVSL circuit can be divided into two basic parts: A differential latching circuit and a cascaded complementary logic array [8]. The latch in these logic circuits is realized with two cross-coupled PMOS transistors. The cascode complementary logic array is realized with a NMOS logic tree [9].

The MDCVSL stands for modified differential cascode voltage switch logic. Delay has been improved by adding two NMOS in the previous design [9]. It is shown in fig.5. The CPL circuit requires complementary inputs and generates complementary outputs to pass on to the next CPL that is in this logic for every signal its complement is generated. Elimination of PMOS transistors reduces the parasitic capacitances associated with each node in the circuit Gates are static, because the output is connected to either VDD or GND.

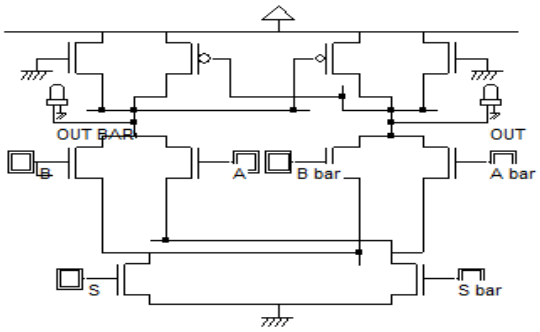

Fig. 5 Schematic design of MDCVSL 2:1 Multiplexer [9].

Design is modular; same cell can produce various gates by simply permuting the input signals. CPL requires fewer transistors. The threshold voltages of NMOS must be reduced to zero through threshold adjustment implants. It performs very fast operation as compare to CMOS. The advantages of CPL logic are good output driving capability due to output inverters, fast differential stage due to cross coupled PMOS structure and small input loads. The main disadvantage of CPL logic is large number of nodes and high overhead due to dual rail signal [10]. Schematic design of CPL MUX is shown in Fig. 6.

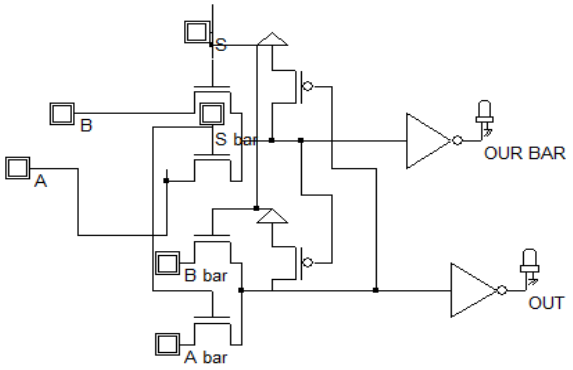

Fig. 6 Schematic design of CPL 2:1 Multiplexer [10].

In the energy economized pass-transistor logic (EEPL), the sources of the PMOS pull-up transistors of a CPL gate are connected to the complementary output signal instead of Fig. 6.The main advantage of smaller delay and smaller power dissipation compared to CPL [10-11]. Because of regenerative positive feedback which provides shorter delay than CPL logic. It has same structure as CPL MUX employing two PMOS and four NMOS instead of a positive feedback [12]. It is shown in Fig.7.

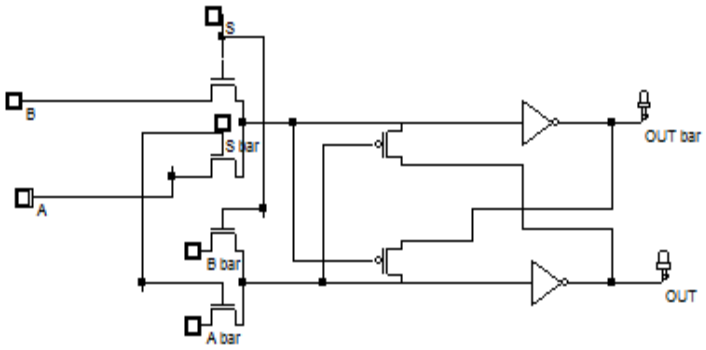

Fig. 7 Schematic design of EEPL 2:1 Multiplexer [10].

III. PROPOSED SCHEMATIC DESIGN

This design 2:1 MUX is based upon a pair of cross coupled inverters. In this latch is made from two PMOS and two NMOS that avoids the degradation of the logic level at the output node. These NMOS devices are connected between output and ground. A sinusoidal supply is applied [13-14]. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. It is known as positive feedback adiabatic logic [15]. Schematic is shown in Fig.8

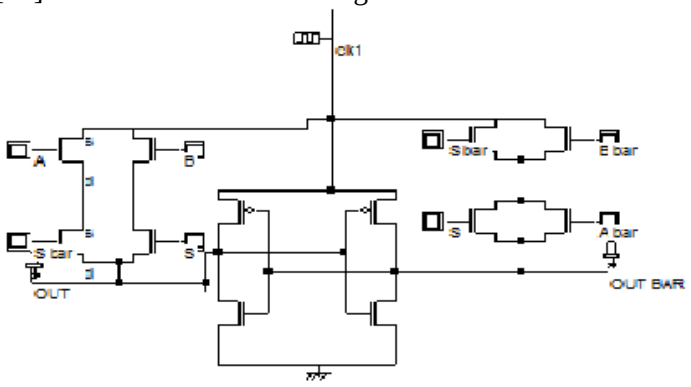

Fig. 8 Schematic design of proposed 2:1 adiabatic multiplexer.

Timing diagram of proposed 2:1 Mux is shown in Fig. 9. It logically verifiy the different states the circuit. Timing simulation is performed at schematic design.

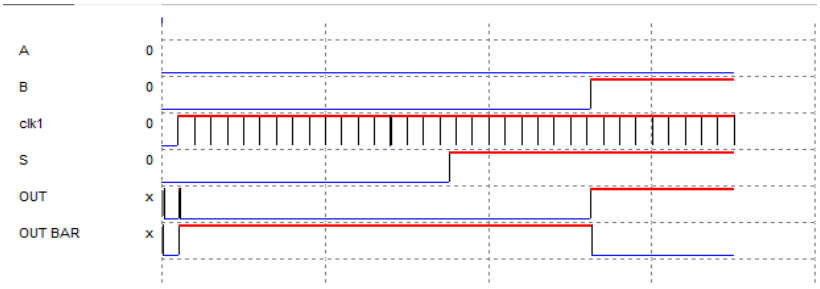

Fig. 9 Timing diagram of proposed 2:1 adiabatic multiplexer.

A 4-2 compressor has three five input and three outputs. It receives an input *C*in from the preceding module of one binary bit order lower in significance, and produces an output *C*out to next compressor module of higher significance. To accelerate the carry save summation of the partial products, the output Cout must be independent of the input *C*in [16]. In the proposed compressor multiplexer and X-OR based module is used. In this design multiplexer and X-OR is implemented through PFAL logic. Fig. 10 4-2 Multiplexer based adiabatic compressor design is presented.

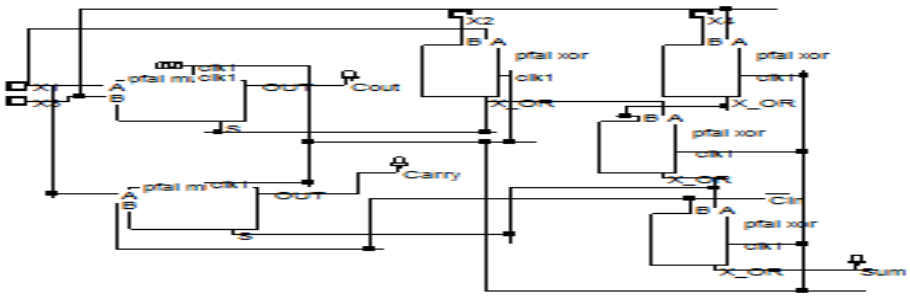

Fig. 10 Adiabatic multiplexer based 4-2 compressor.

IV. LAYOUT & SIMULATION

All the simulations have been done using Microwind 3.1 CAD tool. All the schematics are drawn using 0.12-µm technology with a 1.2V supply voltage. Layout out design of proposed multiplexer is shown in Fig. Regular layout style is used in order to simplify the overall geometry and the signal routing. Layout occupies the area 152.2µm at 0.12µm technology shown in Fig.9.

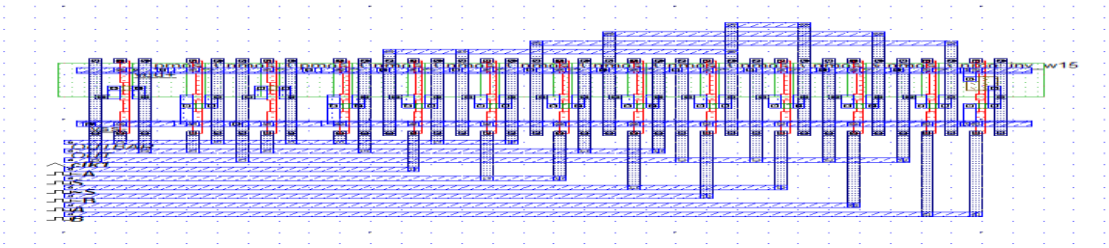

Fig. 11 Layout of proposed 2:1 Multiplexer.

Layout simulation is performed on the layout of proposed design. Fig.12 shows time domain simulation of Multiplexer. Logic '0' corresponds to a zero voltage and logic '1' corresponds to 1.2V. A sinusoidal signal is applied as power clock supply. Simple clocks are applied as inputs and select lines [17].

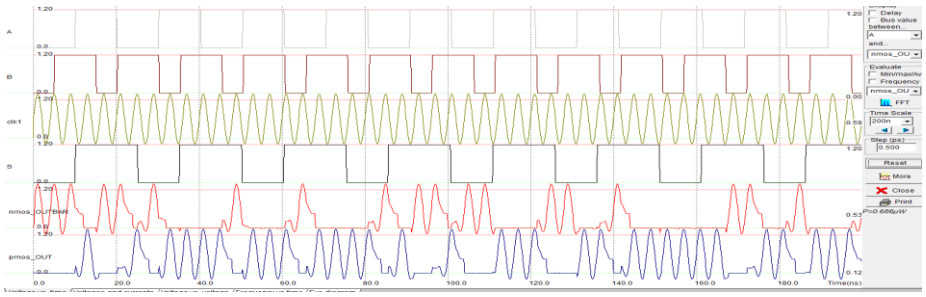

Fig. 12 Layout simulation of proposed 2:1 Multiplexer.

Layout out design of adiabatic multiplexer based 4-2 compressor is shown in Fig. 11. Layout is designed 0.12µm Technology.

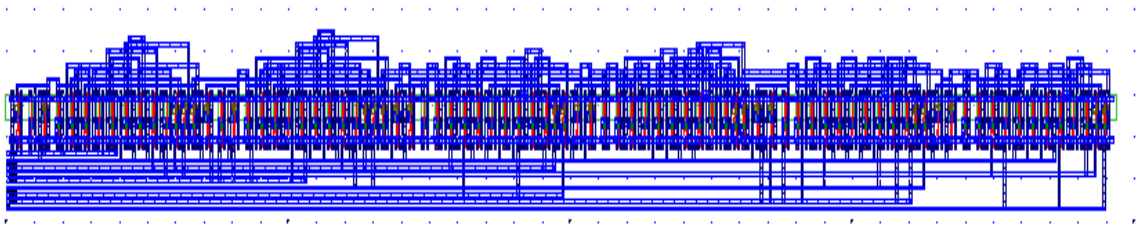

Fig. 13 Layout of adiabatic multiplexer based compressor

Layout simulation of adiabatic 4-2 compressor is carried out at 1.2 V. It is shown in Fig. 12. All results are simulated at 200 nano scale with a constant temperature of 27^0C. By using positive feedback adiabatic logic full swing is obtained in output waveform. The frequency of applied sinusoidal clock is 250 MHz.

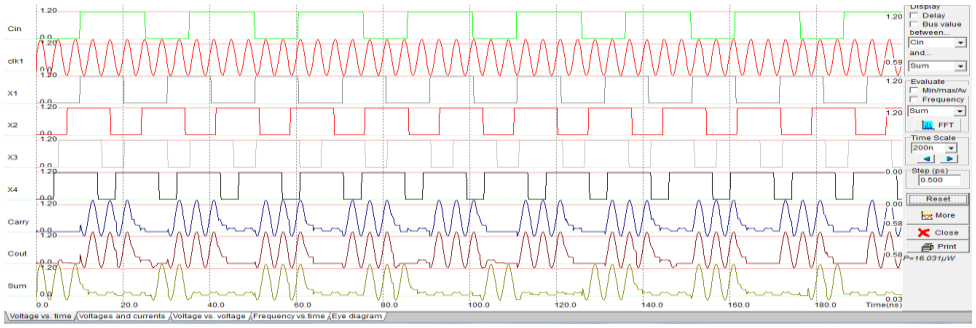

Fig. 14 Layout simulation of 4-2 adiabatic compressor.

V. RESULTS & COMPARISON

Different 2:1 multiplexers designs such as DCVSL[8], MDCVSL [9], CPL [10], EEPL [11] are simulated and compared with proposed multiplexer in terms of power consumption and maximum drian current at frequency of 66MHz. Simulated results are shown in table. It has been observed that Proposed multiplexer is power efficient among all multiplexers.

Table. 1 Comparison of different 2:1 Multiplexer

Parameters	**MDCVSL[9]**	**DCVSL[9]**	**CPL[10]**	**EEPL[10]**	**Proposed**
No. of Mosfets	2 PMOS 8 NMOS	2 PMOS 6 NMOS	2 PMOS 4 NMOS	2 PMOS 4 NMOS	2 PMOS 4 NMOS
Supply Voltage	1.2V	1.2V	1.2V	1.2V	1.2V
Frequency at V_{DD}	66 MHz	66 MHz	66MHz	66MHz	66MHz
Power dissipation (µW)	2.292	1.954	1.892	1.463	0.686
Maximum drain current(mA)	0.155	0.126	0.247	0.151	0.124
Threshold voltage	0.4V	0.4V	0.4V	0.4V	0.4V

Proposed adiabatic 4-2 compressor is simulated and compared with conventional CMOS based compressor. Table 2 shows that proposed compressor is more power efficient than conventional one.

Table. 2 Comparison of 4-2 compressor.

Compressor design	**Power dissipation (µW)**
Conventional compressor	77.338
Adiabatic compressor	16.32

Power consumption of the circuits strongly depends upon the parameter variations. The impact of parameter variation on power consumption is investigated for different logic style MUX by using

BSIM4 Mos model. Graphs shown in Fig 15, 16, 17 and 18 are obtained as the result of parametric analysis on the layout of MDCVSL, DCVSL, CPL, EEPL and proposed adiabatic MUXs.
Fig. 15 and 16 shows power consumption of different 2:1 multiplexer at various supply voltages. It can be noted from the graph that power consumption increases with supply voltage. Proposed multiplexer shows best results in terms of power consumption among all multiplexers implemented with different logic. All the simulations are carried out at a specific range of voltages to show the best results [18].

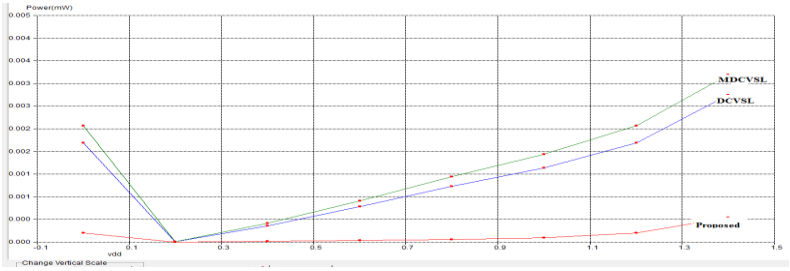

Fig. 15 Variation of power consumption with respect to supply voltage at 27^0C.

Threshold voltage for all the simulation is fixed to .4V. In both the Fig. 15 and 16 it has been shown that circuits operates efficiently only after the threshod voltage. After .4V linear curve is achieved.

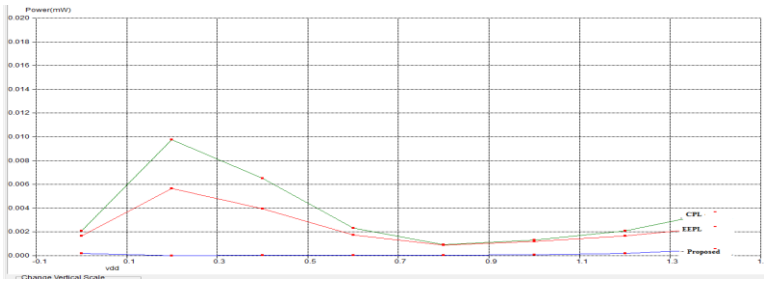

Fig. 16 Power consumption variation of different 2:1 MUX with respect to supply voltage at 27^0C.

Temperature Variation of MOS is temperature sensitive device. In this simulation three parameters are concerned with the sensitivity to temperature: Threshold voltage, mobility and slope in the sub-threshold mode [19]. Fig.17 and 18 shows graph between power consumption and temperature for different 2:1 MUX. Proposed design shows a large power saving with temperature.

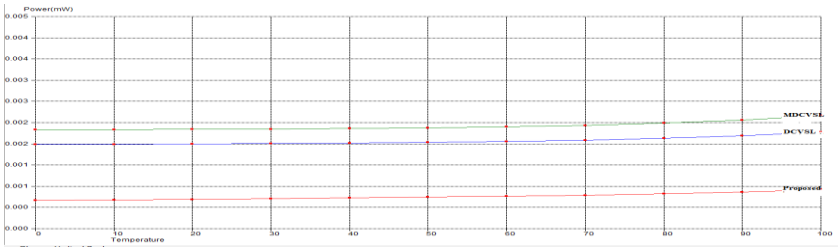

Fig. 17 Power coonsumption versus temperature of different 2:1 Multiplexer at 1.2V

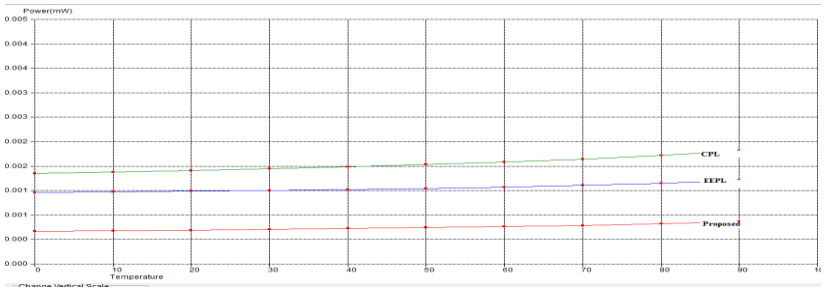

Fig. 18 Variation of power consumption with temperature for different Multiplexer at 1.2V

VI. CONCLUSION

Multiplexer through various logic style has been designed and simulated using DSCH & Microwind 3.1. These logic styles includes DVCSL, MDCVSL, CPL and EEPL multiplexer designs . Among all these logic styles EEPL MUX is more power efficient. Further EEPL multiplexer is compared with the proposed adiabatic multiplexer which is designed using PFAL logic and it has been seen that proposed MUX shows better performance in terms of power consumption. It is recorded that 53.1% improvement is obtained in terms power consumption as compare to EEPL multiplexer. Also 4-2 compressor is designed using proposed adiabatic MUX. This MUX based compressor is simulated at .12µm technology. The proposed adiabatic compressor saves 79% power than conventional CMOS based compressor design. All results are verified at different supply voltage and temperature. Proposed Multiplexer shows good performance with supply voltage temperature variations as compare to EEPL, CPL, DCVSL, MDCVSL multiplexer.

VII. FUTURE SCOPE

i. The high cost-per-weight of launching computing-related power supplies, solar panels and cooling systems into orbit imposes a demand for adiabatic power reduction in spacecraft in which these components weigh a significant fraction of total spacecraft weight.

ii. Realizing 4:1, 8:1, 16:1 multiplexers using 2:1 multiplexer with the help of adiabatic logic families.

iii. Adiabatic circuits needs non conventional power supply which causes overhead in terms of area hence overall cost is increased. So design a new adiabatic logic family which can be operated using conventional power supply.

iv. Switching speed of adiabatic circuit is slow as compare to CMOS logic. So design a new adiabatic family with better switching speed.

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