A Memristor-Based Random Modulator for Compressive Sensing Systems

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Abstract—Memristors promise to allow high levels of compaction in computing systems because these elements combine memory and switching functionality. This can be utilized to overcome some of the hardware challenges in compressive sensing architectures. In this paper, we propose a compressive sensing system architecture that uses a memristor-based random modulator. The gains of using such a memristor-based modulator mainly stem from replacing memory blocks and many of the switching components typically used in compressive sensing. We discuss some of these benefits and the design considerations that need to be addressed in memristor-based compressive sensing architectures.

I. INTRODUCTION

Since Hewlet-Packard announced the fabrication of the memristor in 2008 [1]. The memristor was first hypothesized in 1971 by Chua based on symmetry arguments to be the forth passive circuit element, in addition to the three canonical passive circuit elements (resistance, inductance, and capacitance) [2]. Chua hypothesized the existence of a fourth passive element, dubbed the memristor, that relates the magnetic flux to the charge, and is given by

\[ M(q) = \frac{d\phi}{dq}, \]

where \( \phi \) is the magnetic flux and \( q \) is the charge. The memristor, which can be thought of as a resistor with memory, relates the current and voltage as \( v = M(q) i \), and thus has the nature of a resistor. The \( i - v \) characteristics of a memristor show hysteresis, the memristor can be modeled as having two resistance values, \( R_h \) and \( R_l \), which can be altered by applying a voltage across the memristor [1], [3]–[5]. The memristor has been proposed in a wide range of applications such as non-volatile memories, neuromorphic chips, digital circuits, and analog circuits, to name a few [1], [6]. The main advantage of the memristor stems from its ability to combine memory functionality with switching capability.

In this paper, we propose an architecture for utilizing the power of the memristor in compressive sensing systems. Compressive sensing is a signal acquisition framework that allows the reconstruction of a signal from a number of samples, called measurements, much less than dictated by the famous Shannon’s sampling theorem [7]–[13]. Reducing the sampling rate while maintaining high signal fidelity enables the reduction of power consumption by analog-to-digital converters, a major source of power consumption in most mixed-signal systems. Compressive sensing systems use high rate random signals that are digital-like, which increase the noise in the system and require many components to switch at the same rate, in addition to using digital random number generators. By using a memristor-based architecture for compressive sensing systems, our goal is to achieve a compact system that shows gains over conventional compressive sensing architectures, especially in terms of compactness and area.

The rest of the paper is organized as follows. Section II presents an overview of compressive sensing. Section III introduces the proposed memristor-based compressive sensing system and discusses the proposed architecture. Section IV concludes the paper.

II. OVERVIEW OF COMPRESSIVE SAMPLING

A signal \( x \in \mathbb{R}^N \) is said to be of sparsity \( S \) if \( x \) has at most \( S \) non-zero entries. In such a case, the signal \( x \) can be reconstructed from a signal of measurements, \( y \in \mathbb{R}^M \),

\[ y = \Phi x \]

with \( M < N \) and \( \Phi \in \mathbb{R}^{M \times N} \), if the matrix \( \Phi \) satisfies the restricted isometry property (RIP) with a small restricted isometry constant defined as a constant \( \delta_S \) that satisfies

\[ (1 - \delta)||x|| \leq ||\Phi x|| \leq (1 + \delta)||x|| \]

for all signals \( x \) of sparsity \( S \) [10]. The class of matrices whose entries are drawn from a Gaussian or Bernoulli set

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of random variables satisfies, with a very high probability, the RIP with a small RIP constant \[7\]. The signal \(x\) can be reconstructed from the measurement vector \(y\) by solving the \(L1\) minimization problem

\[
x = \arg \min_{\tilde{x} \in \mathbb{R}} ||\tilde{x}||_1 \quad s.t. \quad \Phi \tilde{x} = y
\]  

(4)

An analog signal \(f(t)\) can be expanded in a basis \(\Psi\) with basis functions \(\psi_i(t)\). It is common to represent an analog signal, \(f(t)\) as a finite sum of weighted basis functions, or

\[
f(t) = \sum_{k=1}^{K} \alpha_k \psi_k(t),
\]  

(5)

where \(\psi_k(t)\) are some basis functions. For example, framing a signal \(f(t)\) using a rectangular window results in the signal \(f_{fr}(t)\), given by

\[
f_{fr}(t) = \sum_{k=1}^{\infty} \hat{F}(\frac{2\pi k}{T_{fr}}) e^{j2\pi k t},
\]  

(6)

where \(\hat{F}\) is the Fourier transform of \(f(t)\) and when the framed signal is almost bandlimited to the frequency \(F_N\), with \(N = F_NT_{fr}\), we can write

\[
f_{fr}(t) = \sum_{k=1}^{N} \hat{F}(\frac{2\pi k}{T_{fr}}) e^{j2\pi k \frac{t}{T_{fr}}}
\]  

(7)

For sparse signals, with only \(S\) non-zero Fourier coefficients, the expression (7) is similar to (5), with \(\omega_k = \frac{F_N}{T_{fr}}\). This signal model is applicable in receivers that process signals on a frame by frame basis. In many compressive sampling receivers, the discrete time measurements obtained at the output of the ADC can be related to a discrete time vector representing the analog signal, such as the vector containing the \(\alpha_i\)'s in (7) [11]. Thus, for a system where the signal has a Nyquist rate of \(F_N\), the discrete time signal representing the analog signal would have length \(N = F_NT_{fr}\), which is the number of samples obtained if the signal were to be sampled at the rate \(F_N\). The number of measurements generated by the system would be \(M = F_s T_{fr}\), where \(F_s\) is the sub-Nyquist rate at which the back end analog to digital converter runs [11].

III. A MEMRISTOR-BASED COMPRESSIVE SENSING SYSTEM

The memristor has two states: a high resistance state, where the resistance is \(R_h\), and a low-resistance state, where the resistance is \(R_l\) [14]. The most desirable property in this regard is memristor’s configurability as the state of the memristor can be decided by applying the appropriate voltage level across it; the memristor will remain in the same state as long as the voltage level does not exceed a (relatively high) threshold voltage [14]. Another crucial advantage of the memristor is that it does not suffer from leakage power [6]. Similar advantages can be achieved in compressive sensing applications. In these applications, the input signal is pre-processed in the analog domain before being digitized at a rate below its Nyquist rate [8], [11], [15]–[21]. The pre-processing stage entails mixing the signal with a set of random signals of \(\pm 1\) and then integrating or low pass filtering the mixed signal. The random signals are generated digitally, for example by means of a linear feedback shift register, and should run at a rate that is higher than the signal’s Nyquist rate. It is desirable for each measurement (or sample) to be obtained by projecting the input signal on a random signal that runs for as long a duration as possible. There have been two general approaches that handle the tradeoff between hardware complexity and power consumption on one hand and high quality measurements on the other hand.

The random demodulator favors hardware simplicity and power efficiency and uses short random sequences [11]. Fig. 1 shows a schematic of the building block in many compressive sensing systems. In systems such as the random demodulator, the measurements are sampled at a rate of \(T_{fr}/M\), where \(T_{fr}\) is the period of repetition of the (pseudo) random signal and the filter is reset after the acquisition of each measurement. \(M\) measurements are collected in a period of \(T_{fr}\) and these \(M\) measurements are used to reconstruct the input signal. Effectively, each measurement is obtained by projecting the input signal on a windowed version of the random signal. The measurements are linearly related to a discrete-time vector representing the analog input signal by \(y = \Phi \Psi \alpha\), where \(\Psi\) is an operator mapping the sparsity domain to the time domain, such as the discrete Fourier transform, and \(\Phi\) is given by

\[
\Phi = \begin{pmatrix}
\pm 1 & \cdots & \pm 1 & 0 & \cdots & 0 & \cdots & 0 & \cdots & 0 \\
0 & \cdots & 0 & \pm 1 & \cdots & \pm 1 & \cdots & 0 & \cdots & 0 \\
\vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\
0 & \cdots & 0 & 0 & \cdots & 0 & \cdots & \pm 1 & \cdots & \pm 1
\end{pmatrix}
\]  

(8)

where the number of \(\pm 1\) in each row is \(N/M\), or the ratio of the Nyquist rate to the sampling rate of the backend ADC. On the other hand, other compressive sensing systems use \(M\) compressive sensing channels similar to that in Fig.1 but sample each at a rate of \(T_{fr}\). Thus, \(M\) measurements are collected after a period of \(T_{fr}\), just like the case of the random demodulator, but the information content of each measurement
is richer in this case, because a length $N$ random sequence is used to acquire each measurement, while in the case of the random demodulator, a length $N/M$ sequence is used. The measurement matrix in such systems, given that the random signal has the values $\pm 1$, is

$$
\Phi_{\text{Full}} = \begin{pmatrix}
\pm 1 & \cdots & \pm 1 \\
\pm 1 & \cdots & \pm 1 \\
\vdots & \vdots & \vdots \\
\pm 1 & \cdots & \pm 1
\end{pmatrix}
$$

where the number of $\pm 1$ in each row is $N$. The gain in information obtained because of the use of length $N$ sequences, however, comes at the expense of hardware complexity.

The proposed memristor-based compressive sensing architecture uses the memristor as a multiplexer to route the signal between two routes, one keeping the signal intact and one passes the signal through an inverting stage. We use $N$ such components in order to implement the projection of the signal on a length $N$ random signal. Here the length $N$ of the random signal refers to the number of $+1$ and $-1$ the signal assumes during the measurement acquisition period; that is, $N = F_N/T_{\text{FR}}$, where $F_N$ is the rate of the random signal and $T_{\text{FR}}$ is the measurement acquisition time. A multiplexer alternating at the rate $F_N$ connects the output of each of these stages to an integrator. The schematic of the system is shown in Fig. 2. In order to acquire $M$ measurements, $M$ such blocks should be used. The memristor alleviates the need to use any other memory blocks as it provides the means to store the random signal values and is reconfigurable. Because of the reconfigurability of the memristor, the whole structure can be reconfigured to implement a different measurement matrix. Reconfiguration requires the application of the correct voltages on the memristors to be turned on or off, and once the configuration voltage is removed, the memristors would stay in the configured state. Additionally, the memristors are non-volatile and do not need external power sources for holding the configured state. The resistance of the memristor in the high-resistance state is high enough so that its multiplexing functionality is effective [14].

The proposed system replaces a set of $M$ mixers and the circuitry needed to generate $M$ random sequences of length $N$. As the frequency of the random signals, or the Nyquist rate, increases, the power consumed by each mixer and the jitter induced by the random signals increase. It also becomes harder to design the system at higher frequencies because of the digital nature of the random signals. The proposed system mitigates these effects because it does not implement a dynamic mixer that takes the digital-like random signals as an input. Rather, it uses only one switching element that connects the integrator to the corresponding block.

In order to study the performance of the proposed system under practical values of the high and low resistance of the proposed system, we use the values $R_l = 1k\Omega$ and $R_h = 1000k\Omega$ [14]. For simplicity, we assume that the back-end ADC has a zero input capacitance and the switch is ideal. The proposed system then can be modeled as having the effective sequence

$$
p_{\text{eff}} = p\frac{R_h/R_l}{1 + R_h/R_l} + \hat{p}\frac{1}{1 + R_h/R_l}
$$

where $p$ is the ideal random sequence and $\hat{p}$ is it complement ($\hat{p} = -p$). In order to demonstrate the reconstruction accuracy using our proposed architecture, we generate an input signal by randomly picking the positions and amplitudes of the non-zero frequency components. Fig. 3 shows a randomly picked signal, with 50 non-zero components (top subplot), that was accurately...
reconstructed using the proposed architecture for a sampling rate of \((1/10)\times\text{(Nyquist rate)}\). The reconstructed signal is shown in the bottom subplot. While achieving a more compact and jitter-tolerant design than traditional compressive sensing systems, the results show that our memristor-based compressive sensing architecture successfully reconstructs signals that are sampled significantly below their Nyquist rate. Such memristor-based architectures promise a great potential for next generation compressive sensing systems.

IV. CONCLUSION

The unique properties of the memristor make it suitable to provide solutions to problems in a wide range of applications. In this paper, we introduce compressive sensing as another area where the memristor promises to mitigate many of the limitation and challenges faced by conventional implementation platforms. Compressive sensing has been rapidly emerging as a framework that enables analog-to-digital-converters to defy Shannon’s sampling theorem and has tremendous advantages in many applications. Using memristor-based architectures for compressive sensing systems allows further gains in terms of chip area, jitter resilience, and design complexity.

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