A Low-Power IC Design for the Wireless Monitoring System of the Orthopedic Implants

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Abstract—This paper proposes an architecture of the wireless monitoring system for the real-time monitoring of the orthopedic implants. The system monitors the implant duty cycle, detects abnormal high amounts of force, and other conditions of the orthopedic implants. Data for diagnosis is communicated wirelessly by Radio Frequency (RF) signal between the embedded chip (inside body) and the remote circuit (outside body). In different working modes the system can be powered by the RF signal or stiff lead zirconate titanate (PZT) ceramics which are able to convert mechanical energy inside the orthopedic implant into electrical energy. The Radio Frequency (RF) circuits with the working frequency of 2.4GHz have been taped out with 0.18\( \mu \)m CMOS technology with 50\( \mu \)W. It can supply 400\( \mu \)W power over a distance of 20cm between the two transceivers. The power circuits have been taped out with 0.35\( \mu \)m CMOS technology. The circuits including RF circuits, Analog Digital Converter (ADC), and Micro control Unit (MCU) have been implemented in 0.18\( \mu \)m CMOS process.

I. INTRODUCTION

Total Knee Replacement (TKR) can release patients with degenerative joint disease from severe pain and immobility due to osteoarthritis. However, TKR implants will fail because of wear, loosening, misalignment, etc. As a result, revision surgery will be conducted, bringing more pain to the patients. Therefore, early diagnosis of abnormalities is critical for avoiding injury. Embedded implant sensors could provide new in-vivo diagnostic capabilities that reduce these clinical complications and lead to improved implant materials and designs [1].

All the electronic sensors need power. Battery has been the power source of most electric-driven devices. However, the limited lifetime and physical dimension have rendered traditional batteries unacceptable for some power-critical or maintenance-free real-time embedded applications such as the wireless sensor, orthopedic implants etc. In [2], an analysis on the power generation characteristics of the stiff PZT ceramics and its equivalent circuit is put forward. It is then verified by simulation and experimental results. It was found that the maximum power (about 1.2mW) is generated when the four PZTs receive uniform and maximum force from the implant. Compared to [1], smaller PZT elements are used in the work, which specifically addresses the problem of limited space available inside an implant.

In this paper, we consider a low power IC design of the wireless monitoring system of orthopedic implants. The sensors are encapsulated within the implants, and provide in-vivo diagnostic data (i.e., force, pressure, etc.) to monitor the primary responsibility of the implant.

II. SYSTEM ARCHITECTURE

The proposed system architecture shown in figure 1 consists of two parts: one embedded in the orthopedic implants, and the other outside the body, both of which are analog-digital mixed-mode circuits. Inside the embedded part, the sensors are applied to obtain in-vivo data which will be then saved in EEPROM. The embedded part can be powered by RF signal as well as the PZT elements [2]. The low power MCU is the center control unit and is in charge of power management, control of data writing process, and other logic control operations. Outside the patient’s body, there is a RF front-end module connected to a computer or a portable recording device. The two parts of the system communicate with each other by the RF signal. The data from the EEPROM in the embedded part can be stored in the recording device, which can be mounted on the leg of the patient, and will be used by the doctor afterwards for analysis and diagnosis. In the opposite direction, the control information can be wirelessly transmitted to the embedded chip when necessary.

![Fig. 1. System architecture](image-url)
converter is designed to transform the biological information into digital data to be stored in the memory.

III. CIRCUIT DESIGN

A. RF Circuits Design

Figure 2 illustrates the block diagram of the RF circuits. The “RF Limiter” circuit keeps the amplitude of the input RF signal within a limited range to avoid damage due to excessive voltage. The “Rectifier” circuit uses Schottky diodes to rectify the current, and the “Regulator” circuit provides steady voltage when the input voltage is fluctuating. The “Oscillator” circuit supplies clock for the EEPROM, and the “Bias” circuit provides the bias current for other circuits. Obviously, the “Modulator” circuit and “Demodulator” circuit modulate and demodulate the signal respectively. The “RST” circuit gives the reset signal to the entire system. Figure 3 is the reset circuit, figure 4 is the demodulator circuit, and figure 5 is the power recovery circuit.

The circuit diagram in Fig. 2 has been taped out with 0.18μm CMOS technology as shown in Fig. 6. The size of the chip is 0.5mm*1mm. It can supply 400μW power over a distance of 20cm between the two transceivers, and the working frequency is 2.4GHz. The power dissipation is about 50μW.

The test result is shown in Fig. 7(a), in which the upper is the demodulated signal which has some glitch caused by the capacitor of the testing circuit, and the lower is the clock signal extracted from the demodulated signal. The reset signal, which is used to reset the digital circuit, is shown in Fig. 7(b). Its high value is equal to the voltage values extracted from the received signal. The test result verifies that the RF circuit can work well.
B. Power Circuit Design

The output of PZT varies with the force applied on the TKR implant. In [2] it can be seen that the piezoelectric signal consists of mainly the frequencies between 1Hz and 4Hz. At 1Hz, the power is maximized (about 0.5mW); for frequencies higher than 4 Hz, the power approaches zero. Knowing the frequency characteristic of the power, the proposed power regulation circuit is shown in Fig. 8.

![Fig. 8 Schematic power circuit](image)

In Fig. 8, the power generated by PZT is first rectified by a full-wave bridge rectifier to convert the bipolar piezoelectric output to a unipolar output. Then, a capacitor is used as storage element in parallel with the load circuit. An oscillation circuit is embedded to generate clock signals for an “SC converter” (Switching Capacitor based on DC-DC Converter), which will lower the input voltage from approximately 10V to 2V. The input voltage is controlled by four programmable switches, as shown in the dashed block in Fig. 8. Therefore, the power circuit can provide four different voltages to other circuits. Finally, a Low Drop-Out (LDO) voltage regulator reduces the voltage further to a steady value around 1.5V.

The HSPICE simulation result of the LDO circuit is shown in the Fig. 9: the input voltage in the circuit is 4V and the output voltage is approximately 1.5V.

![Fig. 9. Simulation result of LDO.](image)

C. ADC design

The analog-to-digital converter (ADC) converts the analog signal from the sensors into digital signal. According to system requirement, the ADC works at a sample frequency of 400Hz and has the resolution of 8 bits. The two-step cyclic ADC is adopted.

The ADC has four analog input channels. At one time only one channel will be chosen to be converted into digital signal. The ADC has two working modes, the normal mode and the sleep mode. When the ADC is in normal mode, it converts the analog inputs into digital outputs. When the ADC is in sleep mode, all the circuits will not work and almost no power will be consumed. This is achieved by turning off the bias circuit

![Fig. 10. Die microphotograph of the power circuit.](image)
of the analog part and clock-gating the digital circuits.

The whole circuit of the ADC with the 1.5-bit correction circuit is shown in Fig. 12. The digital logical circuit consists of a shift register and an end adder.

![Diagram of the ADC](image)

**Fig. 11** The top circuit of the ADC

The converter is fabricated at 0.18µm standard CMOS process with single-poly, six-layer metal. All the simulation results were obtained using the software of Spectre as follow. The frequency of the input signal and the clock frequency were set to full scale, 25.765Hz, and 1MHz, respectively. A typical low-frequency fast Fourier transform (FFT) output spectrum is shown in Fig. 13. The spurios free dynamic range (SFDR) is approximately 61dB. The signal-to-noise-plus-distortion ratio (SNDR) of the ADC is 48dB. Then, from formula (1), the effective numbers of bits (ENOB) is about 8bits.

$$ENOB = \frac{SNDR(dB)}{6.02} - 1.76$$  

(1)

In the normal mode, the ADC core (not including I/O) consumes 14µW at the 1.8V supply with the sample frequency of 400Hz. In sleep mode, the ADC core consumes less than 100nW at 1.8V supply.

![Diagram of the ADC output spectrum for full scale input sine wave](image)

**Fig. 12** ADC output spectrum for full scale input sine wave

**IV. ASIC DESIGN**

The 0.18-µm CMOS process technology is used for the digital IC inside the human body. The layout of the chip embedded is shown in Fig. 13. It will be verified in the testing system in the next work.

![Diagram of the chip layout](image)

**Fig. 13** The layout of the circuit embedded

**V. CONCLUSION**

This paper proposes a novel architecture of the wireless monitoring system for the real-time monitoring of the orthopedic implants. The analog-digital mix-mode system monitors the implant duty cycle, detects high amounts of force, and other conditions of the orthopedic implants. In different working modes the system can be powered by the RF signal or PZT elements. The Radio Frequency (RF) circuits with the working frequency of 2.4GHz have been taped out with 0.18µm CMOS technology with 50µW. It can supply 400µW power over a distance of 20cm between the two transceivers. The SC converter can transfer the input voltage (9.5V) from the PZT elements into 2.9V which will be dealt with by LDO circuit in the future work. The total efficiency of the SC converter is 28.1% at fulltime working mode. The ADC circuit is also designed to meet the requirement of the system. The circuits including RF circuits, Analog Digital Converter (ADC) and Micro control Unit (MCU) have been implemented in 0.18µm CMOS process. The low power and small size chip make it possible to put the chip inside the implant to be checked. Future work includes some clinical experiments test in the application where PZT elements are used for power generation in a TKR implants.

**REFERENCES**


